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A Design of Wide-Bandwidth LDO Regulator with High Robustness ESD Protection Circuit

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Abstract

A low dropout (LDO) regulator with a wide-bandwidth is proposed in this paper. The regulator features a Human Body Model (HBM) 8kV-class high robustness ElectroStatic Discharge (ESD) protection circuit, and two error amplifiers (one with low gain and wide bandwidth, and the other with high gain and narrow bandwidth). The dual error amplifiers are located within the feedback loop of the LDO regulator, and they selectively amplify the signal according to its ripples. The proposed LDO regulator is more efficient in its regulation process because of its selective amplification according to frequency and bandwidth. Furthermore, the proposed regulator has the same gain as a conventional LDO at 62 dB with a 130 kHz-wide bandwidth, which is approximately 3.5 times that of a conventional LDO. The proposed device presents a fast response with improved load and line regulation characteristics. In addition, to prevent an increase in the area of the circuit, a body-driven fabrication technique was used for the error amplifier and the pass transistor. The proposed LDO regulator has an input voltage range of 2.5 V to 4.5 V, and it provides a load current of 100 mA in an output voltage range of 1.2 V to 4.1 V. In addition, to prevent damage in the Integrated Circuit (IC) as a result of static electricity, the reliability of IC was improved by embedding a self-produced 8 kV-class (Chip level) ESD protection circuit of a P-substrate-Triggered Silicon Controlled Rectifier (PTSCR) type with high robustness characteristics.

Key words: LDO, Linear, Low-dropout, Multiple error amp, Wide-bandwidth

I. INTRODUCTION

Power management circuits have recently become increasingly important as a result of the rapid propagation of battery-based mobile devices that emphasize convenience of use, such as smartphones. Nowadays, consumers are purchasing products with a wider variety of features. Therefore, researchers must develop techniques that make efficient use of limited battery power for longer periods of time. As a result, high-performance mobile systems require the use of quiescent current, lower power consumption, and fewer parts [1]-[3].

In this paper, A low-dropout regulator with two error amplifiers is proposed in this paper. The proposed regulator is effective and enables efficient power use.

One error amplifier has a small voltage gain and a wide bandwidth, and the other error amplifier has a high voltage gain and a narrow bandwidth. These two error amplifiers have opposite characteristics; therefore, they enable a more efficient power consumption by selectively operating according to the presence of high-frequency elements resulting from changes in the output voltage. The variations in the output voltage are quickly put into a normal state via selective operation according to the bandwidth features [4], [5]. To prevent damage in the IC as a result of static electricity, a self-produced 8 kV-class ESD protection circuit of a PTSCR type with high robustness characteristics was embedded [6].

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II. LOW-DROP OUT VOLTAGE REGULATOR WITH MULTIPLE ERROR AMPLIFIER AND AN ESD PROTECTION CIRCUIT

A. Proposed LDO Voltage Regulator

The structure of a basic LDO regulator is as follows. The voltage that is output from the pass transistor is fed back into the error amplifier through the voltage distributed by the feedback resistor. The error amplifier compares the feedback voltage to the reference voltage and then amplifies the

difference between them. As a result, the error amplifier and the pass transistor together form a feedback loop, and the output remains constant.

The proposed LDO voltage regulator (Fig. 1) consists of a reference voltage generator, a first error amplifier, a second error amplifier, a pass Transistor (TR), and a voltage divider. The first error amplifier receives the reference voltage (Vref) from the negative input terminal and the feedback voltage (Vfb) from the positive input terminal. The output of the first error amplifier is applied to the gate terminal of the pass transistor. The gate terminal determines the drive current that flows through the pass transistor. The second error amplifier receives the reference voltage (Vref) from the negative input terminal and the feedback voltage (Vfb) from the positive input terminal. Therefore, Vref is applied to both the negative input terminals of the first and second error amplifiers, and the feedback voltage Vfb is applied to both the positive input terminals of first and second error amplifiers. The output terminals for the two error amplifiers are both connected to the gate terminal of the pass transistor [7], [8]. To prevent an increase in the area as a result of the use of dual error amplifiers, a body-driven technique was used for the error amplifier and the pass transistor.

B. Operation of Proposed LDO Voltage Regulator

The proposed LDO regulator has two error amplifiers connected in parallel, as shown in Fig. 2. The output voltage fluctuates as a result of external conditions during the early stage of the input or during normal operation, and it has wide and fast frequency elements at the beginning of the fluctuations. At this time, the error amplifier with a wider bandwidth quickly stabilizes the fluctuations in the output voltage. Later, when fewer frequency elements are present, the error amplifier with a higher gain performs the stabilization.

Fig. 3 shows the graphs for the gain and bandwidth of the proposed error amplifier. Depending on the error amplifiers used in general regulators, the first error amplifier is characterized by a lower gain and a broader bandwidth, whereas the second is characterized by a higher gain and a narrower bandwidth.

The gain and bandwidth for the first error amplifier are denoted as A1 and BW1, respectively, and those for the second error amplifier are denoted as A2 and BW2. A2 is higher than A1, BW1 is wider BW2, and the first amplifier has a faster response than the second error amplifier. This setup implies that the first amplifier responds faster to fluctuations in Vout.

The two error amplifiers operate in a common mode during the normal operation in the following case. The Vref and the Vfb are maintained at the same voltage level by a virtual short circuit. If Vout increases, the initial values have high frequency elements. Therefore, the error amplifier with a broad bandwidth and a low voltage gain is activated, and the second error amplifier has a very low gain due to the presence of high

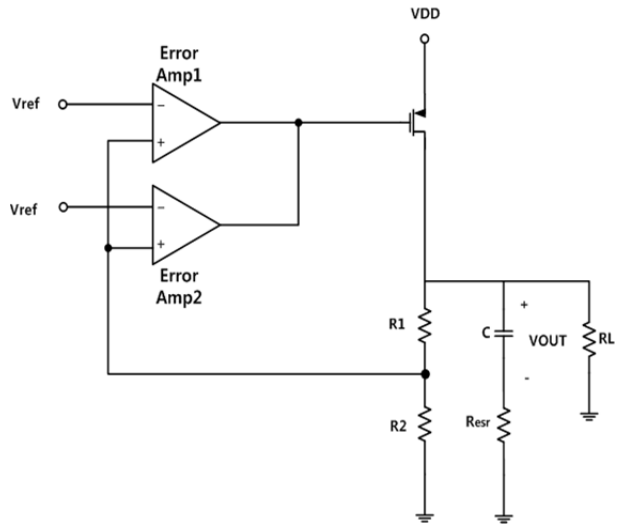

Fig. 1. Structure of proposed LDO regulator.

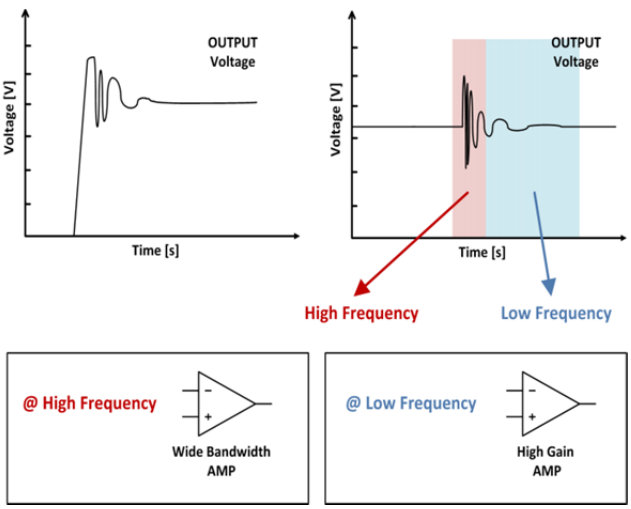

Fig. 2. Operation concept of proposed LDO regulator.

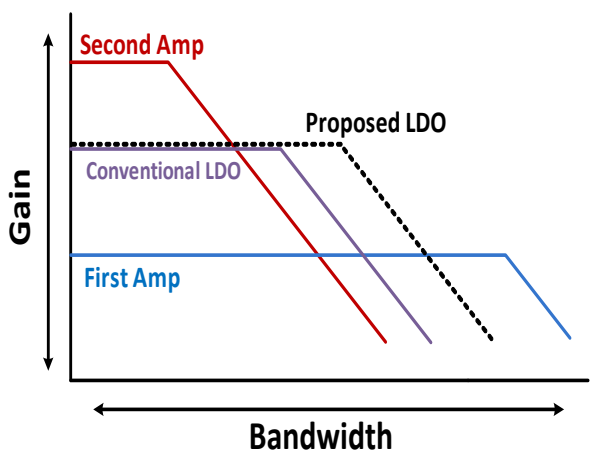

Fig. 3. Gain & Bandwidth of proposed LDO regulator.

frequency elements. Therefore, in the early stages of the fluctuations of Vout, the amplification is carried out by A1 in the first error amplifier. As a result, the drive current in the past transistor decreases, and Vout decreases to a normal state. Vout

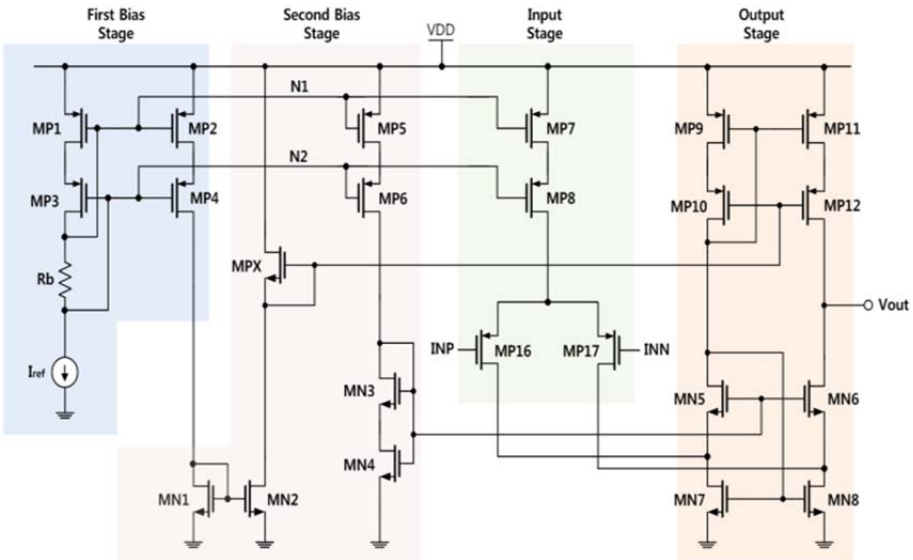

Fig. 4. Proposed first error amp.

continuously decreases and has low-frequency elements.

The gain and bandwidth for the first error amplifier are denoted as A1 and BW1, respectively, and those for the second error amplifier are denoted as A2 and BW2. A2 is higher than A1, BW1 is wider BW2, and the first amplifier has a faster response than the second error amplifier. This setup implies that the first amplifier responds faster to fluctuations in Vout.

The two error amplifiers operate in a common mode during the normal operation in the following case. The Vref and the Vfb are maintained at the same voltage level by a virtual short circuit. If Vout increases, the initial values have high frequency elements. Therefore, the error amplifier with a broad bandwidth and a low voltage gain is activated, and the second error amplifier has a very low gain due to the presence of high frequency elements. Therefore, in the early stages of the fluctuations of Vout, the amplification is carried out by A1 in the first error amplifier. As a result, the drive current in the past transistor decreases, and Vout decreases to a normal state. Vout continuously decreases and has low-frequency elements.

In the low frequency band, the second error amplifier has a higher voltage gain than the first error amplifier, so it amplifies with the voltage gain A2. Therefore, Vfb quickly follows Vref due to the operation of the second error amplifier. In other words, for early fluctuations in Vout, the first error amplifier plays a primary role in regulation, and then the second error amplifier plays a primary role in regulation with a high gain.

C. Proposed Error Amplifier

Fig. 4 shows the circuit diagram of the proposed error amplifier with a broad bandwidth and a low gain. With respect to small signals, the first error amplifier has a cascode configuration in which the common source amplifier and the common gate amplifier are connected in parallel to each other. With respect to a positive input signal (INP), the cascode configuration improves the frequency response characteristics because the common source amplifier has a low impedance output. Therefore, the first error amplifier has a broader bandwidth than the second. Particularly for INP, the structure is that of a serial connection of two-stage cascode configurations with one MP6 and MN5 cascode configuration, and another with MN8 and MN6. Furthermore, in a negative input signal (INN), the structure is that of a one-stage cascode configuration of MP17 and MN6.

Fig. 5 shows the circuit diagram for the error amplifier with a narrow bandwidth and a high gain. The second error amplifier consists of a first bias stage, a second bias stage, an input stage, an output stage, and a second output stage.

The first bias stage, second bias stage, and input stage are identical to those of the first error amplifier, and the first output stage of the second error amplifier is identical to that of the first error amplifier. The signal of the N3 node, which is the output terminal of the first output stage, is applied to the gate terminals of MP14 and MN9. In particular, MP14 has a common source amplifier configuration for small signal modeling. Therefore, the signals of the N3 node that are amplified through MP14 appear in the drain terminal and are applied to the gate terminal of MN12, which has a common

The second error amplifier has MP16 and MN5, which have a cascode configuration in which the common source and common gate amplifiers are serially connected from the perspective of INP. The amplifier has a serial three-stage common source amplifier structure, consisting of MN8, MN11, and MN12, which are connected to the cascode configuration. Furthermore, a second cascode is formed with a common source amplifier and the MN6 common gate amplifier, and MP14 and MN12 have a two-stage serial connection as common source amplifiers.

From the point of view of INN of the second error

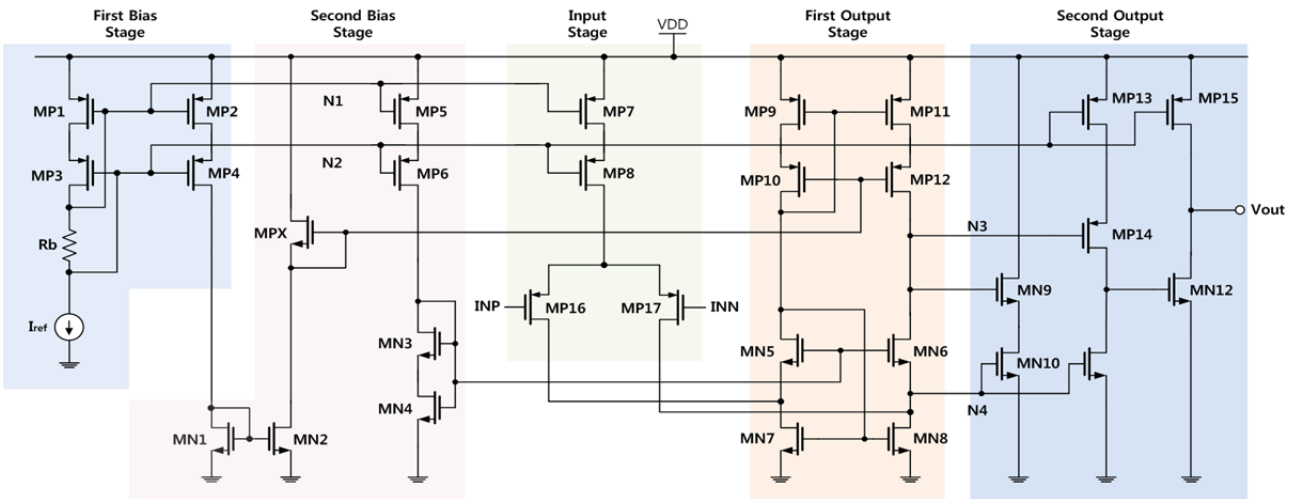

Fig. 5. Proposed second error amp.

amplifier, MP17 and MN6 form a cascode, and the MP14 and NM12 common source amplifiers are serially connected in two stages to the cascode. In the final analysis, the second error amplifier has at least two common source amplifiers that are serially connected to the cascode configuration and have a higher gain than the first error amplifier. However, the second error amplifier has lower frequency characteristics and a narrower bandwidth than the first error amplifier because of the common source amplifiers that are serially connected to the cascode configuration.

The proposed error amplifiers are connected in parallel to other and provide different voltage gains at different frequency bands. In other words, in the high frequency band, the first error amplifier plays the primary role and quickly minimizes the fluctuations of the output terminal. In the low frequency band, the second error amplifier has a higher voltage gain and regulates operation to minimize the fluctuations in the output terminal.

D. Body-Driven Technique

In this study, a forward body bias is applied to the p-channel transistor in order to lower Threshold Voltage (Vth) and to reduce the size of the transistor. A forward body biasing scheme is favorable because it reduces the size of the transistors at the same Vth. However, a strong body bias voltage activates parasitic devices, such as bipolar transistors and p-n junction diode in MOSFETs [2]. Therefore, a forward body bias voltage is limited to certain values to prevent the operation of parasitic devices and to provide stability.

An appropriate forward bias must be defined to achieve a design that prevents the operation of parasitic devices and provides a leakage current that is insensitive to power consumption. In this study, the operation of the transistor was verified and analyzed through variation in the forward body voltage to determine the forward bias voltage. An NMOSFET

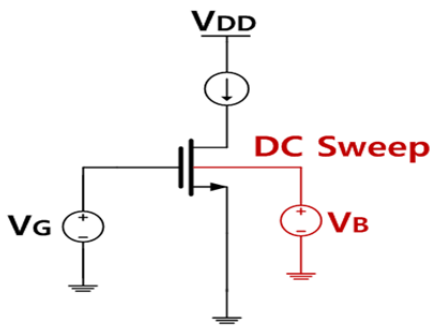

Fig. 6. Body bias technique.

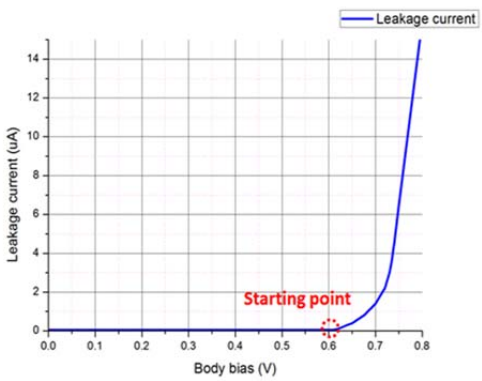

Fig. 7. IBS-VBS characteristic.

transistor was used for the simulation, as shown in Figs. 6, 7, and 8. These figures present graphs obtained via analysis of the IBS-VBS and VDS-VBS characteristic curves. The variations in the body voltage in Fig. 6 indicate the value where the leakage current and current reach maximum can be found.

In Fig. 7, the leakage current sharply increases when the body bias voltage rises to 0.6 V or higher. In Fig. 8, the threshold voltage becomes the lowest when the body bias voltage is 0.7 V. Fig. 9 shows the characteristic curve for the temperature. To prevent the activation of parasitic devices due to changes in the

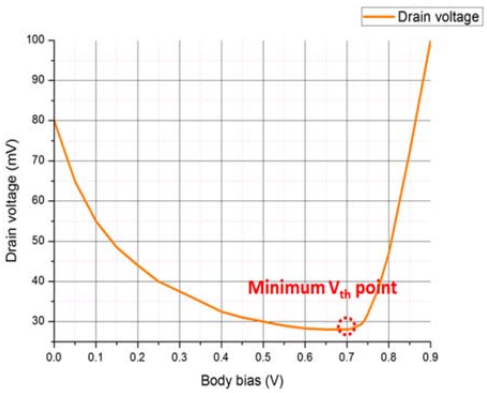

Fig. 8. VDS-VBS characteristic.

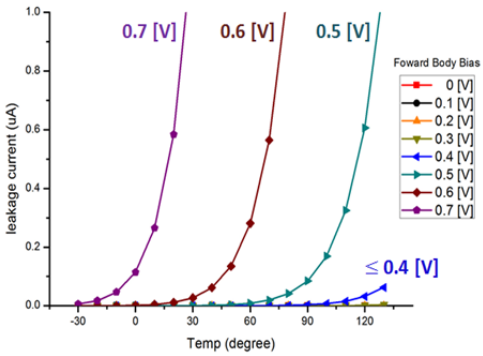

Fig. 9. The characteristic of temperature variation.

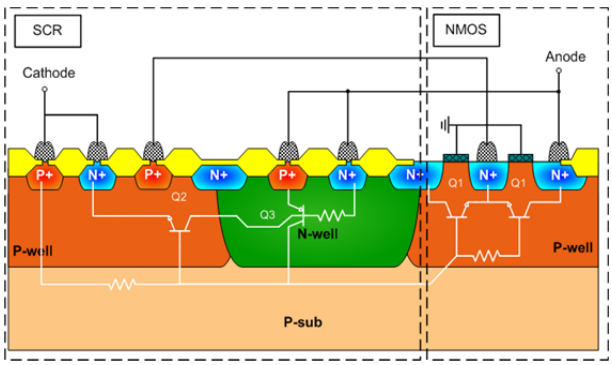

Fig. 10. PTSCR Structure.

temperature, we can check the values for the leakage current at different temperatures. In Fig. 9, when the body bias voltage decreases to 0.4 V or lower, the leakage current becomes insensitive to changes in the temperature. As a result, 0.4 V was set as the body bias voltage for the design of the proposed device.

E. PTSCR(P-Substrate-Triggered SCR)

Fig. 10 shows the structure of the PTSCR, which acts as the ESD protection circuit. This device consists of two Grounded Gate NMOS (GGNMOS) structures (2-Finger GGNMOS) connected in parallel at the right-hand side and an SCR that contains additional bridge N+ and P+ diffusion areas (P+ Tab). This structure enables the following characteristics of the proposed device.

First, the parallel arrangement of the two GGNMOS structures consists of two drain areas (bridge N+, N+ anode) that lowers the avalanche breakdown voltage with P-Well and enables a lower trigger voltage. Second, when the ESD current flows in, this device works separately between the first operation by the GGNMOS and the second operation by the Silicon Controlled Rectifier (SCR). As a result of the first operation process by the GGNMOS, this device generally has a high trigger current and a high holding current. Third, the bridge N+ and P+ diffusion areas (P+ Tab) on the discharge path of the SCR decrease the current gain of the parasitic NPN and PNP of the SCR, increasing the general holding voltage of SCR. In particular, the P+ diffusion area (P+ Tab) is connected to the source of the GGNMOS and supplies the trigger current from the GGNMOS to the SCR. The working principle of this device is that when the anode voltage increases by the ESD current from the anode, the potentials of both the N+ drain of the GGNMOS and the N-Well increase as well. When the electric field between the drain of the GGNMOS and the P-Well in opposite direction reaches the critical value, an avalanche breakdown occurs, generating an electron-hole pair. The electron current that is generated is released to the drain of the GGNMOS and the N+ anode diffusion area of the SCR. The hole current that is generated increases the potential of the P-Well. When the potential of the P-Well becomes greater than the potential of the N+ source diffusion area of the GGNMOS, the hole current flows through the N+ source diffusion area of the GGNMOS. The hole current flowing in through the source of GGNMOS begins to flow into the P-Well through the P+ tab located in the middle of the discharge path of SCR, which increases the potential for the P-Well. When the trigger current increases further, the potential of the P-Well becomes greater than that of the internal electric field of the P-Well/N+ cathode junction. The two junctions are therefore biased in the forward direction, and the parasitic NPN bipolar of the SCR begins to turn on. The activation of the parasitic NPN bipolar activates the parasitic PNP bipolar of SCR, and the SCR is activated by the latch action of the parasitic NPN/PNP bipolar. Most ESD currents are then discharged through the SCR's path [10].

III. Simulation Results

Fig. 11 shows the results of the line regulation simulation for the proposed LDO regulator as well as that of a conventional LDO regulator. The simulation was conducted by adjusting the input voltage from 3.3 V to 5 V with a 60 mA load current. The results of the simulation revealed that the proposed LDO regulator showed a 14 mV change in the output voltage, and the conventional LDO regulator showed a 30 mV change. Thus, the change in the output voltage of the proposed LDO regulator was about 50% that of a conventional LDO regulator.

Fig. 12 shows the results of the load regulation simulation for the proposed LDO regulator and those of a conventional

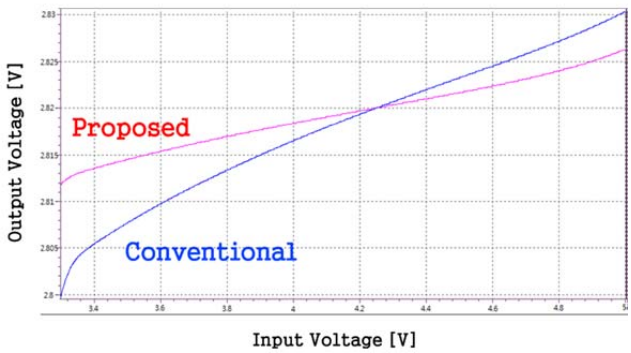

Fig. 11. Simulation results of Line Regulation.

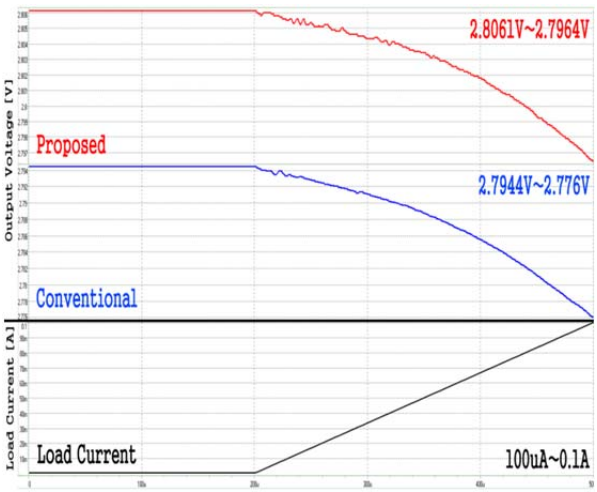

Fig. 12. Simulation results of Load Regulation.

LDO regulator. The simulation of the load regulation was conducted by adjusting the load current from 100 µA to 100 mA, with a 2.8 V output voltage. The results of the simulation indicate that the proposed LDO regulator had a 9.7 mV change in the output voltage, and the conventional LDO regulator had a 18.4 mV change. Thus, the change in the output voltage of the proposed LDO regulator was about 50% that of the conventional LDO regulator.

Fig. 13 shows the simulation of the DC gain, the bandwidth, and phase margin (PM) of the proposed LDO regulator. The DC gain of the first error amplifier is 20 dB, and the DC gain of the second error amplifier is 84 dB. The DC gain of a conventional LDO regulator is 60 dB, and its -3 dB frequency is 36 kHz. However, when the two error amplifiers proposed in this study are used, the DC gain is 62 dB, and the -3 dB frequency is 130 kHz. Thus, the proposed LDO regulator shows a higher bandwidth than the conventional one.

According to the results of the simulation, the second error amplifier has a higher DC gain and a narrower bandwidth than the first error amplifier. Moreover, the conventional LDO regulator has phase margin of 49.7°, and the proposed LDO regulator has phase margin of 69.3°. In conclusion, the two error amplifiers with different gain and bandwidth can improve the DC gain, bandwidth characteristics, and phase margin of the LDO regulator.

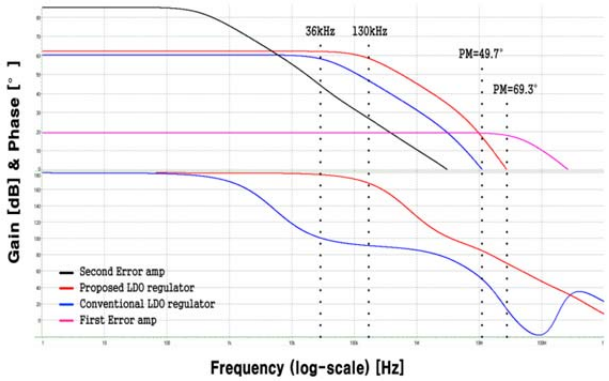

Fig. 13. Simulation results of Gain & Bandwidth & PM.

Fig. 14 shows the results of the simulation of the power consumption for the conventional LDO regulator. The power consumption was simulated by fixing the supply voltage of 3.3 V, load current of 88.9 mA, and output voltage of 2.8 V. As a result, the conventional LDO regulator showed a total power consumption of 295 mW. Because of this, the conventional LDO regulator has an efficiency of 84.4%.

Fig. 15 shows the results of the simulation of the power consumption for the proposed LDO regulator. The power consumption was simulated by fixing the supply voltage of 3.3 V, load current of 88.9 mA, and output voltage of 2.8 V. As a result, the proposed LDO regulator showed a total power consumption of 297 mW. Because of this, the proposed LDO regulator has an efficiency of 83.8%.

As a result, the conventional LDO regulator and the proposed LDO regulator rarely has difference in power consumption and efficiency. Furthermore, the proposed LDO regulator has better characteristics of line and load transient, and line and load regulation. It will be checked in measurement results.

IV. Measurement Results

Fig. 16 shows the results of the measurements of the transient load for the proposed LDO regulator and a conventional LDO regulator. The transient load was measured by varying the load current from 100 µA to 100 mA.

As a result, the conventional LDO regulator showed a change in the output voltage of 90 mV, and the proposed LDO regulator showed a change of 25 mV.

Fig. 17 shows the results of the measurement of the line transient for the proposed LDO regulator and a conventional LDO regulator. The line transient was measured by varying the supply voltage from 3 V to 3.8 V. As a result, the proposed LDO regulator showed changes in the output voltage of 5 mV, and the conventional LDO regulator showed a change of 10 mV. Thus, the change in the output voltage of the proposed LDO regulator was approximately 50% that of a conventional LDO regulator.

Fig. 18 shows the results of the measurement of the line

Fig. 14. Power consumption of conventional LDO.

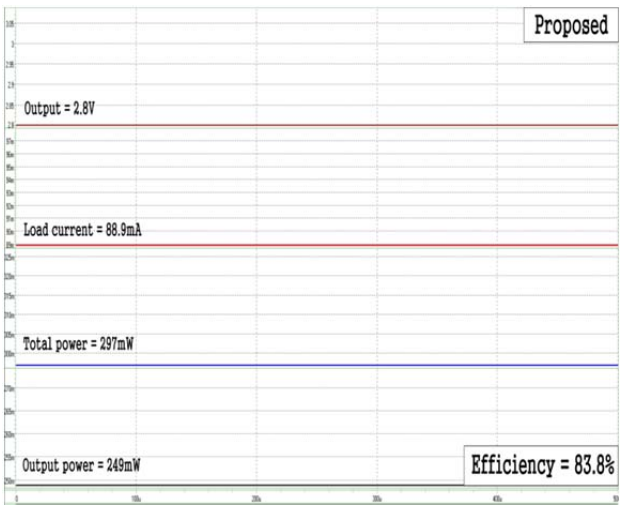

Fig. 15. Power consumption of proposed LDO.

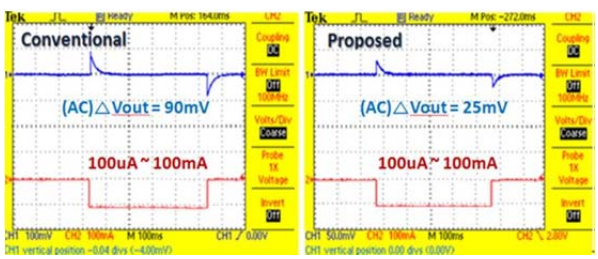

Fig. 16. Load Transient.

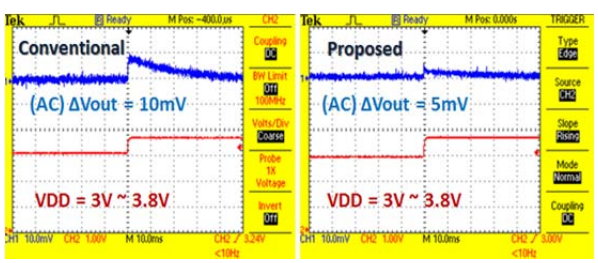

Fig. 17. Line Transient.

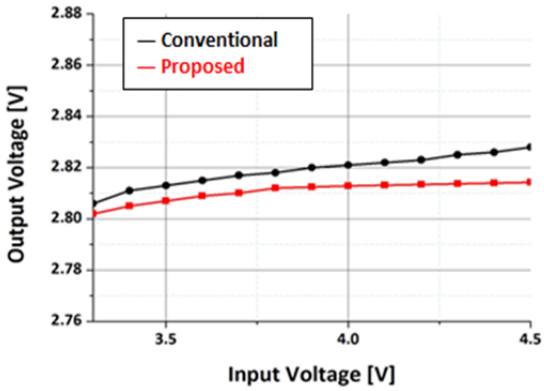

Fig. 18. Line Regulation.

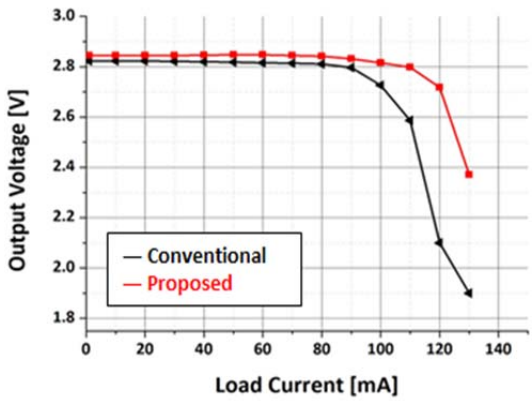

Fig. 19. Load Regulation.

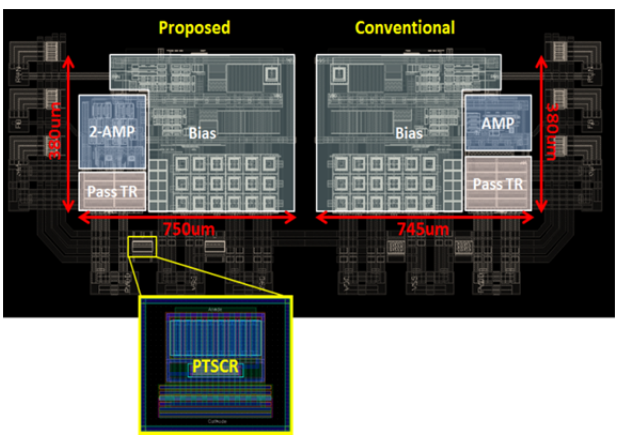

Fig. 20. Layout.

regulation for the proposed LDO regulator and a conventional LDO regulator. The line regulation was measured by varying the supply voltage from 3.3 V to 4.5 V. As a result, the proposed LDO regulator showed a change in the output voltage of 12 mV, and the conventional LDO regulator showed a change of 22 mV.

Fig. 19 shows the results of the measurement of the load regulation. The changes in the output voltage were measured by varying the load current from 100 μA to 100 mA. The conventional regulator showed stable operation until it reached a load current of 90 mA; the proposed regulator had stable operation until it reached a load current of 110 mA.

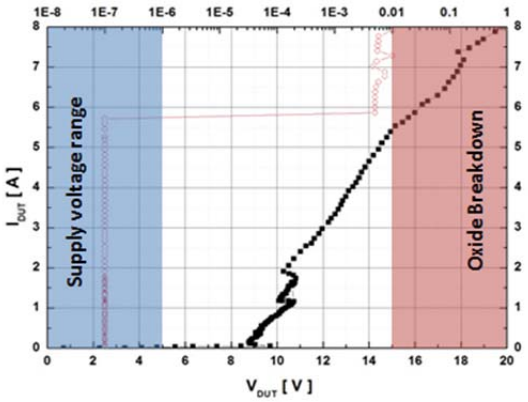

Fig. 21.Chip level TLP I-V curve.

Fig. 22. HBM Test result.

Fig. 20 shows the layouts of the proposed LDO regulator and the conventional LDO regulator. The active area of the proposed regulator is 750 μm * 380 μm, which is almost identical to that of the conventional regulator.

Fig. 21 shows the chip-level Transmission Line Pulse (TLP) I-V curve of the ESD protection circuit that was produced by embedding the proposed regulator. The PTSCR has a holding voltage of 8.3 V and a trigger voltage of 9.69 V, which are both lower than the supply voltage of the proposed LDO. Furthermore, it had a 5.4 A current drive capacity and showed an 8 kV tolerance in the HBM test on the Printed Circuit Board (PCB). Fig. 22 shows the normal operation waveforms before and after the HBM test.

V. Conclusion

An LDO regulator embedded with a high robustness ESD protection circuit was proposed in this paper. The proposed regulator shows an improvement in the regulation characteristics, and its bandwidth is 3.5 times higher than that of a conventional regulator. The proposed regulator has a 12 mV change in the output voltage when the input voltage changes from 3.3 V to 4.5 V, which was approximately 50% lower than that of a conventional regulator. Furthermore, it maintained a stable output until it reached a 110 mA load current, showing a broader range of normal operation than a conventional regulator. In addition, an 8 kV (Chip level) ESD protection circuit of a PTSCR structure was designed and embedded to improve the latch up problem of the low holding voltage of the conventional SCR structure. Therefore, the reliability of the IC improved by preventing the malfunction and breakdown of the IC as a result of ESD.

Acknowledgment

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