JPE 15-6-26

http://dx.doi.org/10.6113/JPE.2015.15.6.1664
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Series Arc Fault Detection Strategy for Single-Phase Boost PFC Rectifiers

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Abstract

This paper proposes a series arc fault detection algorithm which incorporates peak voltage and harmonic current detectors for single-phase boost power factor correction (PFC) rectifiers. The series arc fault model is also proposed to analyze the phenomenon of the arc fault and detection algorithm. For arc detection, the virtual *dq* transformation is utilized to detect the peak input voltage. In addition, multiple combinations of low- and high-pass filters are applied to extract the specific harmonic components which show the characteristics of the series arc fault conditions. The proposed model and the arc detection method are experimentally verified through a boost PFC rectifier prototype operating under the grid-tied condition with an artificial arc generator manufactured under the guidelines for the Underwriters Laboratories (UL) 1699 standard.

Key words: Arc fault detection, Power factor correction, Series arc, UL1699

I. INTRODUCTION

The installation of arc fault detectors, such as arc fault circuit interrupters (AFCIs), has been required by law or strongly recommended, because arc faults are considered to be the cause of most electrical fires [1]-[4]. Among the three different kinds of arc fault types, parallel, ground, and series [5], [6], the detection accuracy of series arc faults is lower than the others. The reason is that the shape of the input current under a series arc fault is similar to that of a normal nonlinear or light load condition. Several arc detection strategies, including the signal analysis and the hardware filtering techniques, have been proposed for commercial electric systems, photovoltaic converters, and AFCIs [3], [7]. However, series arc detection under low power conditions is still a big challenge. On the other hand, the growth of the renewable energy industry also demands AFCIs for protection [8], [9].

A power quality meter which can detect series arc-faults has been proposed in [10]. In that paper, the root-mean-square (rms) values of the voltage and current, and the total harmonic distortion (THD) were utilized to detect series arcs. However, this method cannot be directly applied to arc fault analysis in power electronic circuits. For series arc detection, the adaption of the wavelet transform approach is considered to be a recent trend [11], [12]. However, they increase the calculation load.

On the other hand, the use of a simple and accurate arc model is very important to quickly analyze the arc detection mechanism. However, it is difficult to establish a well-defined arc model because of its nonlinearity. Several arc models have been proposed in [13]-[18]. However, except for the two diode models, they are somewhat complicated and not very intuitive. In addition, the accuracy of the traditional two diode models is not very high.

To develop an arc detection apparatus or algorithm, it is important to follow the recommendations in the Underwriters Laboratories (UL) 1699 standard [19] where the functional description, the rule, and the testing method in arc fault detection are described. For series arc faults, the UL1699 states that an arc detector should be able to detect a series arc fault under an input current larger than 5A for 120V line conditions. However, this may not be directly applicable to 220V lines, because a lower current is necessary at the same power rating when compared to 120V lines.

In this paper, a series arc fault detection method is proposed for single-phase power factor correction (PFC) converters. The proposed method consists of the peak voltage and harmonic current detectors. For the peak voltage

Manuscript received Mar. 24, 2015; accepted May 17, 2015
Recommended for publication by Associate Editor Honnyong Cha.
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detector, the virtual *dq* concept is applied, and the peak voltage information is obtained directly. The harmonic current detector utilizes multiple combinations of low- and high-pass filters to detect harmonic components. Both of the algorithms are implemented in software, and can be plugged into existing PFC controllers. Consequently, no additional expense is expected. Experimental results with the proposed method demonstrate the detection capability of series arc faults with less than a 3A current, which is 1.66 times worse when compared to the UL1699 standards.

II. MODELING OF SERIES ARC FAULTS

Fig. 1 shows the PFC converter configuration with poor connectivity dealt with in this paper. Series arc faults are mainly caused by a poor or loose connection between the grid voltage source v_g and the input terminal voltage v_i. The defective connection introduces highly nonlinear impedance which changes according to the phase angle. Usually, the impedance near the zero crossing point (ZCP) of v_i is higher than that in other locations, and this leads a zero current as shown in the figure. The section where the input current is zero is called as a shoulder [6]. The voltage drop across nonlinear impedance during series arc faults is defined as the arc voltage v_{arc}. Then, the relationship among v_g, v_i, and v_{arc} is established as below.

$$v_g = v_{arc} + v_i \tag{1}$$

From (1), it is supposed that v_i decreases when v_{arc} is generated. In fact, v_{arc} contains severe harmonic components because of nonlinearity. Since the total harmonic distortion (THD) of v_g is much lower than v_{arc}, it is supposed that v_i will contain undesirable harmonic components. In Fig. 2, typical shapes v_g, v_i and v_{arc} are shown. Here, T_g is the period of the grid voltage. The section where the arc voltage is nearly flat is defined as the plateau. It can be considered as a "steady-state" for the arcing condition. As shown in this figure, v_i is distorted near the ZCP because of the arc voltage v_{arc}. If the air-gap between the two terminals increases, more distortion is generated. This naturally increases the third harmonic component in the input current. It should be noticed that this ZCP voltage distortion provides important information for arc detection. Ideally, the grid voltage v_g should not be changed. However, it is slightly affected due to the grid side impedance.

Fig. 3 shows the proposed low frequency series arc generation model. This model mainly consists of three parts, ideal diodes, passive components, and voltage sources. In this figure, R_p, R_n, L_p, and L_n constructs the impedance models for the positive and negative cycles during a series arcing condition. The diode and the voltage source V_{bias} work as clipper circuits, and mainly determine the starting point of a fault current. In the existing models [13, 18], only the dc source V_{bias} has been considered. However, as can be seen in Fig. 2, v_{arc} includes ac components, and they cannot be modeled with

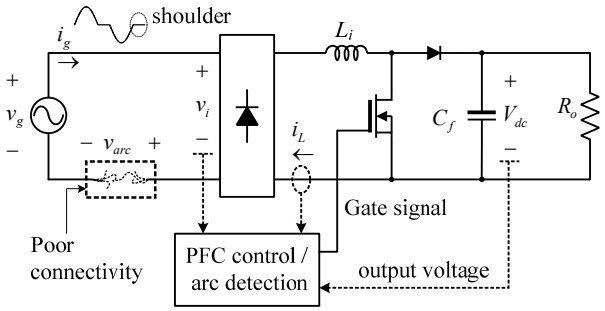


Fig. 1. PFC converter configuration under a series arc fault condition.

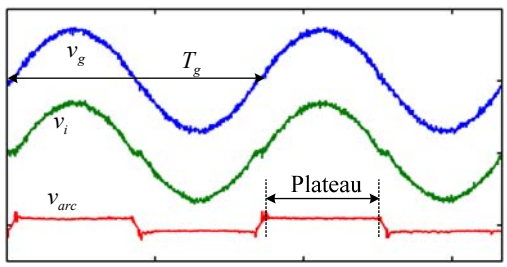


Fig. 2. Typical shapes of v_g, v_i, and v_{arc} under series arc fault conditions.

V_{bias}. In order to cover the ac component and to improve the accuracy of the arc model, the use of ac voltage v_r is proposed in this paper. By considering these components, the voltage equations can be established. For positive cycles with a series arc, the upper branch conducts, and the series arc voltage v_{arc} is written as follows:

$$v_{arc} = V_{bias} - v_r + i_p R_p + L_p \frac{di_p}{dt} \tag{2}$$

where i_p represents the input current during the arc fault condition. The voltage equation of the lower branch which conducts for negative cycles is represented as:

$$v_{arc} = -V_{bias} - v_r - i_n R_n - L_n \frac{di_n}{dt} \tag{3}$$

In (2) and (3), v_r is defined as follows:

$$v_r = K_r v_g \tag{4}$$

where f_g and K_r represent the fundamental frequency of the grid voltage and the model correction factor whose range varies from zero to unity. By adjusting K_r, the depth of the circular arc during fault conditions, which will be detailed, later can be changed. If the gap in the poor connection is assumed to be very narrow, the inductances L_p and L_n can be ignored. Then, (2) and (3) can be simplified as follows:

$$v_{arc} = V_{bias} - v_r + i_p R_p \tag{5}$$

$$v_{arc} = -V_{bias} - v_r - i_n R_n \tag{6}$$

The values of R_p, R_n, and V_{bias} are proportional to the physical air-gap at the location where the series arc fault occurs so that the two electrical conductors are separated. Usually, R_p and R_n have the same value. Equations (5) and (6) represent the generated arc voltage for the plateau where D_p or D_n is conducting. In this case, the conditions below should be valid

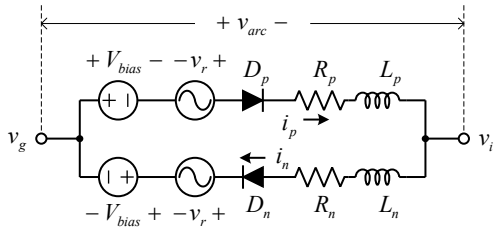


Fig. 3. Proposed low frequency series arc generation model.

for the positive and negative input voltage cycles:

$$v_g - v_i > V_{bias} - v_r \quad (v_g \geq 0) \tag{7}$$

$$v_g - v_i > -V_{bias} - v_r \quad (v_g < 0) \tag{8}$$

If (7) or (8) is not satisfied, D_p or D_n does not turn on, and the input current i_p or i_n does not flow. Then, v_i is zero, and v_{arc} can be obtained as follows from (1).

$$v_{arc} = v_g \tag{9}$$

In summary, the series arc voltage can be modeled with (5), (6), and (9) according to the voltage and current conditions.

III. PFC Controller with the Proposed Series Arc Fault Detection Method

A. PFC Control Strategy

Fig. 4 shows a PFC controller including the proposed arc detection algorithm which will be discussed in this section. The controller consists of a voltage controller $G_v(z)$, a current controller $G_c(z)$, a duty feed-forward d_{ff}, a phase-locked loop (PLL), and the proposed algorithm. Here, the voltage and the current controllers are in the form of traditional proportional-integral (PI) controllers.

The voltage controller regulates the dc-link voltage V_{dc} as a voltage reference higher than the peak input ac voltage V_{pk}. For the voltage controller, the control bandwidth should be much less than the fundamental electrical frequency of the system to avoid the well-known double frequency power ripples in single-phase power systems.

For PFC operation, the input current is controlled by the current controller. To improve the current control performance, the duty feed-forward d_{ff} which follows is added to the output of the current controller.

$$d_{ff} = -\left|\frac{v_i}{V_{dc}}\right| \tag{10}$$

By adding d_{ff}, the admittance component in the current control loop can be compensated. As a result, the excessive integration in $G_c(z)$ is prevented. The control bandwidth of $G_c(z)$ should be as high as possible. Usually, it is limited by one tenth of the sampling frequency with the single sampling technique.

A block diagram of the PLL is shown in Fig. 5 [20]. The PLL employs an all pass filter (APF) whose pole frequency is 60Hz to obtain the same shape of the input voltage with 90 degree of phase delay. With the two sinusoidal signals, the *dq*

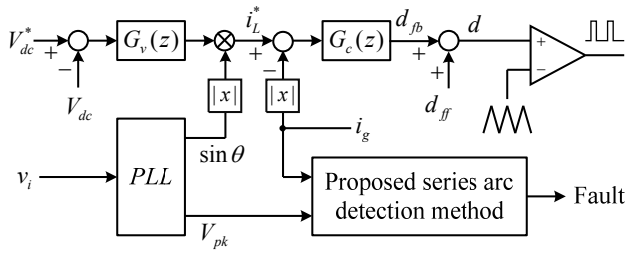


Fig. 4. PFC converter control scheme with the proposed series arc detection algorithm.

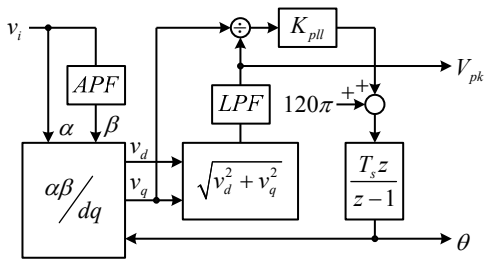


Fig. 5. The structure of the PLL.

components are obtained in the synchronous reference frame. This is the so-called virtual *dq* transformation which decomposes the input voltage into the original and orthogonal ones. The relationship between the peak voltage V_{pk} and the *dq* reference frame voltages v_d and v_q is established as follows:

$$V_{pk} = \sqrt{v_d^2 + v_q^2} \tag{11}$$

Equation (11) gives that V_{pk} can be continuously obtained whenever v_d or v_q is controlled to be zero. Here, the *q* axis value is taken to be zero. By doing so, the phase angles can be extracted simultaneously. The estimator is implemented with the proportional gain, K_{pll}. After passing the integrator, the estimated phase angle θ is obtained. This angle is again returned to the $\alpha\beta$ to *dq* transformation. In fact, this PLL offers important information for the proposed series arc detection algorithm, which will be discussed in the following subsection.

B. Proposed Series Arc Fault Detection Algorithm

Fig. 6 shows the proposed series arc fault detection algorithm. The algorithm determines whether a series arc has occurred or not using three indicators, the peak voltage magnitude, the derivative of the peak voltage variation, and the harmonic current detector including multiple LPFs and HPFs. From (1), it can be seen that the PFC input voltage v_i is decreased when a series arc fault has occurred so that the arc voltage v_{arc} is established. Accordingly, V_{pk} is also reduced with an increasing v_{arc}. For this reason, V_{pk} is an important indicator which divulges whether a series arc fault has occurred. The detection of V_{pk} is easily achieved by monitoring the virtual *d* axis voltage v_d and its low-pass-filtered component in the PLL as shown in Fig. 5. Here, V_{pk} is compared with the minimum allowed peak voltage V_{pkL}. If V_{pk} is less than V_{pkL}, indicator S_1 becomes true. In practice, the power grid can undergo the under-voltage (UV) condition. To minimize misreading during

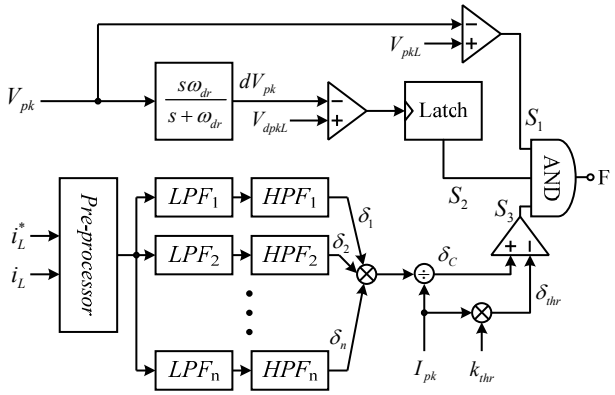


Fig. 6. Proposed series arc fault detection algorithm.

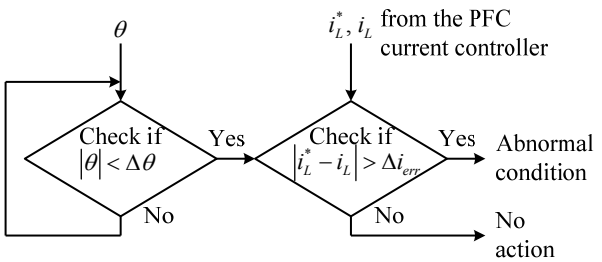


Fig. 7. The flowchart of the pre-processing step.

the normal UV condition, V_{pkL} is determined by averaging 600 cycles of V_{pk}, and taking 85 to 95 percent of the averaged V_{pk} in the software, when no arc fault is detected.

The other criterion to detect a series arc is the derivative of V_{pk}. Again, equation (1) is utilized. The series arc induces the voltage drop, and it can be detected using the derivative filter as follows:

$$G_{dV} = \frac{s\omega_{dr}}{s+\omega_{dr}} \tag{12}$$

where ω_{dr} is the pole frequency. In fact, G_{dV} is equal to a 1st order HPF. Since the output of G_{dV} is returned to zero at the steady-state, the latching of the output signal is necessary in the plateau region. In this paper, the latching is implemented in the software.

The last stage is evaluating the harmonic components in the input current. This consists of two steps, the pre-processing and using multiple combinations of LPFs and HPFs. The pre-processor, shown in Fig. 7, checks the level of the input current error i_{err} between the current reference i_L^* and the input current i_L near the ZCPs. Once this error is over a certain value Δi_{err}, the pre-processor regards it as an abnormal situation. By using the pre-processor, the series arc detection accuracy under light load conditions, where the input current already has some harmonics, can be improved.

Once the pre-processor detects an abnormal situation, certain frequency components of $\underline{i_L}$ are extracted by using the LPFs and HPFs. In Fig. 8, several filtering branches are paralleled. In the figure, the subscript n represents the number of paralleled branches. Each branch is composed of one LPF and one HPF, and their cut-off frequencies are different. Either 1st or 2nd order

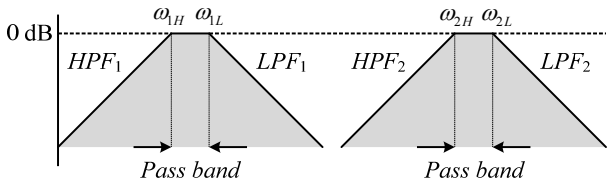


Fig. 8. Configuration of the harmonic frequency passbands.

TABLE I
THE RELATIONSHIP BETWEEN THE AIR-GAP DISTANCE AND THE ARC VOLTAGE

g_{arc} (mm)	v_g	v_i	v_{arc}
2.5	200.1	188	16.43
2.6	200.3	187.9	16.42
2.7	200.2	187.9	16.41
2.8	200.1	187.4	16.77
2.9	200.1	186.9	17.41
3.0	200.3	187.2	17.42
3.1	199.9	186.5	18
3.2	199.9	185.7	18.58
3.3	200.2	186	18.96
3.4	200	185.7	19.32
3.5	200.2	185.3	19.38
3.6	201.5	9.3	202.5

filters can be employed. The cut-off frequencies of the filters, LPF_n and HPF_n, are selected as follows:

$$\begin{aligned} \omega_{nL} &= \omega_n + \Delta\omega_n \\ \omega_{nH} &= \omega_n - \Delta\omega_n \end{aligned} \tag{13}$$

where ω_n, $\Delta\omega_n$, ω_{nL}, and ω_{nH} represent the passband frequency, half of the passband width, and the cut-off frequencies of the LPF and the HPF in the branch, respectively. The candidates for ω_n are the harmonic frequencies of the fundamental electrical frequency. The passband width affects the accuracy of the filtering effect. A wider passband shows better performance than a lower one, but the potential aliasing effect should be avoided. One simple rule to selecting the passband width is sharing the cut-off frequency of a LPF with that of a HPF in the next branch. By doing so, the aliasing problem can be solved, and the iteration cycle of the software can be considerably reduced. Once the outputs of each branch are obtained, they are multiplied by each other as follows:

$$\delta_c = \delta_1 \times \delta_2 \times \cdots \times \delta_n / I_{pk} \tag{14}$$

where δ_n and I_{pk} are the filtered output of the n-th branch and the peak magnitude of the input current to normalize δ_c for different load conditions. This multiplication process is used to maximize the detection capability of the series arcs because the multiple harmonic components are conjugated under the series arc condition. Next, the obtained δ_c is compared with the harmonic threshold δ_{thr}, which is determined by I_{pk} and the correction factor k_{thr}. In practice, it may be necessary for δ_{thr} to be tuned by considering the signal-to-noise ratio of the sampled current information. Finally, the proposed algorithm judges the incidence of a series arc when the values of all of the indicators S_1, S_2 and S_3 become simultaneously true.

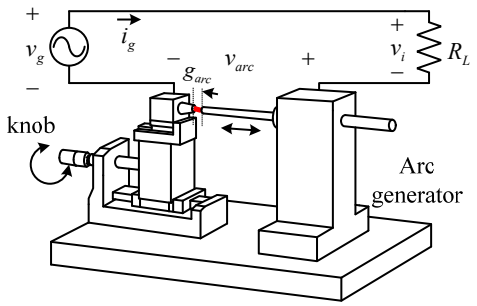


Fig. 9. Test configuration for arcing voltage.

TABLE II
PARAMETERS FOR THE BOOST RECTIFIER

System Parameter	Values
nominal grid voltage	$220V_{rms}$
load resistance R_o	242Ω
dc-link capacitance C_f	680μF
boost inductor L_i	4mH
Switching frequency f_s	20kHz
algorithm iteration frequency f_a	20kHz

IV. PRELIMINARY TEST AND SIMULATION

To examine how the air-gap in the series arc path affects the arc voltage, a preliminary test was performed. Fig. 9 illustrates the configuration for the test. An arc generator which follows the guidelines outlined in UL1699 is placed between the source and the load. The length of the air-gap g_{arc} between the two terminal points can be adjusted by turning the knob. At the beginning, g_{arc} is 0mm, and v_g is directly applied to R_L whose resistance is 70Ω so that the 3A input current condition can be met at the steady-state. After that, the knob is turned, and g_{arc} is increased. Once g_{arc} is set by the reference distance, the rms values of v_g, v_i, and v_{arc} are measured.

Table I summarizes the test results. In the results, v_i gets lower as the air-gap increases because of the increasing v_{arc}. This means that a lower voltage is transferred to the load side when a series arc fault occurs. The grid voltage rarely changes because of the lower impedance. For the 3.5mm condition, v_{arc} is almost 10 percent of the input voltage. When g_{arc} is 3.6mm, the closed current path is no longer established, and the circuit is open. Fig. 10 shows the relationship between g_{arc}, v_i, and v_{arc}. It is obvious that a longer air-gap induces a higher v_{arc} and a lower v_i.

For the simulation, a simulation model of the circuit in Fig. 1 has been built in PSIM software. For the arc voltage, the proposed model is implemented. Table II shows the parameters of the boost PFC rectifier. In the preliminary test results, the minimum v_{arc} is 16.43V when g_{arc} is 2.5mm. This voltage corresponds roughly to 8.21 percent of the input voltage. By considering this, V_{bias} in the proposed arc model is selected as 18V which is 8.21 percent of the nominal grid voltage in the

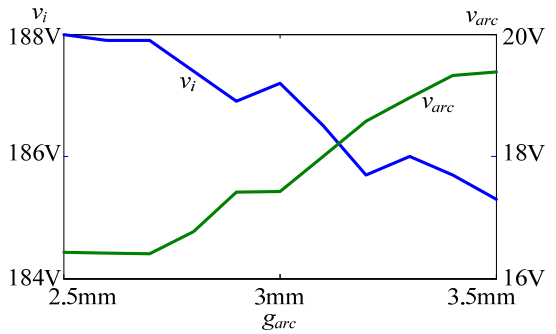


Fig. 10. The relationship among g_{arc}, v_i, and v_{arc}.

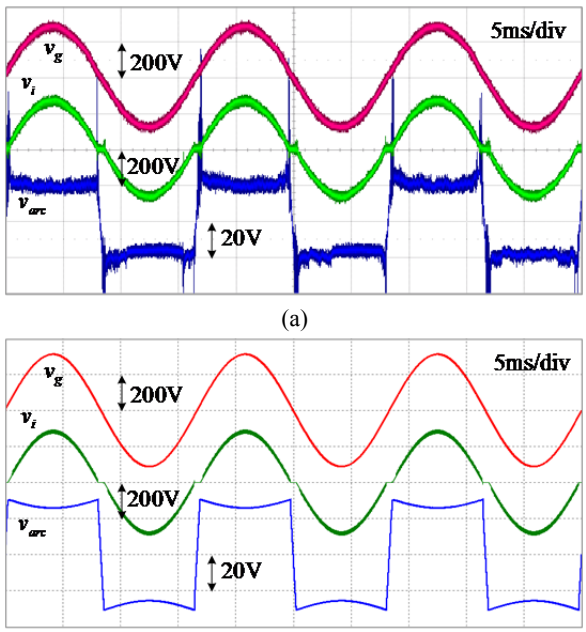
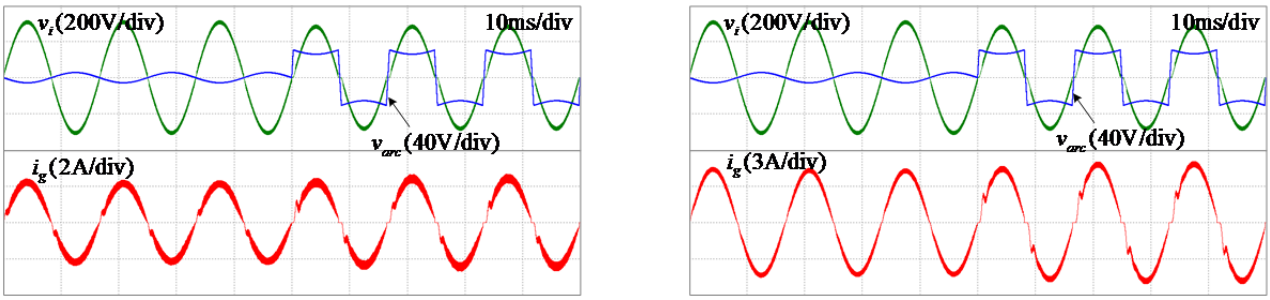


Fig. 11. Measured and simulated voltages. (a) Measured v_g, v_i, and v_{arc}. (b) Simulated v_g, v_i, and v_{arc}.

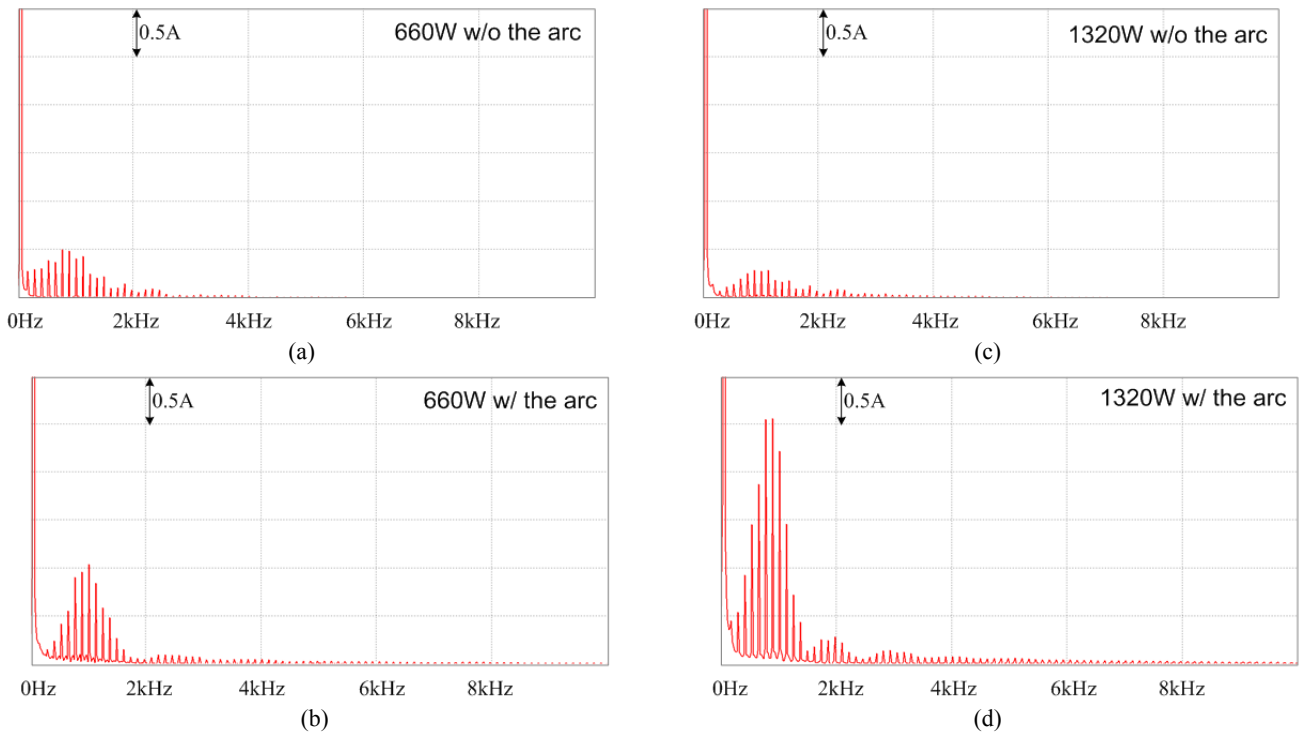
rms. The measured and the simulated values for v_g, v_i, and v_{arc} are compared in Fig. 11. As can be seen in this figure, the proposed arc voltage model reflects the practical phenomenon of the arc condition. The converter input voltage v_i has distortions near the ZCPs as expected. The repetitive spike of the real v_{arc} is caused by nonlinear parasitics which are not considered in the simulation model. However, this does not affect the arc detection capability of the proposed algorithm where high frequency transients are not considered.

Fig. 12 shows the simulated values of v_i, v_{arc}, and i_g for 660W and 1320W load conditions. Here, the series arc occurs at t = 0.05s. For both the 660W and 1320W cases, the magnitude of v_i is slightly reduced, and i_g is distorted when the series arc is applied. It should be noticed that more current distortion is observed in the higher current condition. The frequency component analyses for the input current are illustrated in Fig. 13. Figs. 13(*a*) and (*b*) compare the harmonic contents in i_g for the 660W load condition, where i_g is 3A. Compared to the harmonic contents in Fig. 13(*a*), the 13th, 15th



(a) (b)

Fig. 12. Simulated voltages and currents with PFC operation and arcing conditions. (a) 660W. (b) 1320W.



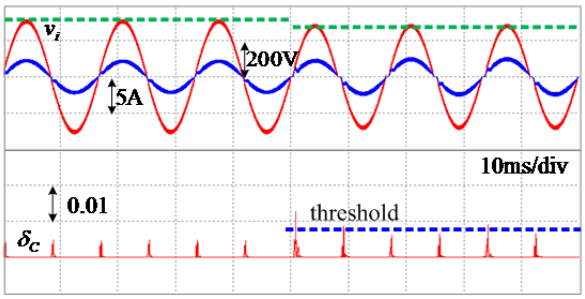
(a) (c)

(b) (d)

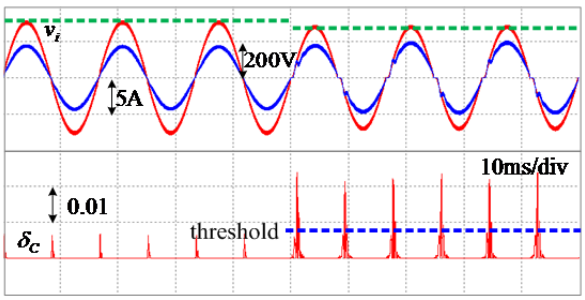
Fig. 13. Frequency components in different load and arc conditions. (a) 660W without the arc. (b) 660W with the arc. (c) 1320W without the arc. (d) 1320W with the arc.

and 17th harmonics have been markedly increased in Fig. 13(*b*), where the series arc has been simulated. Similarly, the harmonic contents are compared in Figs. 13(*c*) and (*d*) for the 1320W load condition. In Fig. 13(*c*), lower harmonic components turn up when compared to Fig. 13(*a*) case. This is due to the fact that a higher current is usually favorable for obtaining a lower THD in boost PFC rectifiers. When the series arc is simulated for the 1320W load condition, the 17th and 19th harmonics are noticeably increased as shown in Fig. 13(*d*). Additionally, an increased amplitude boost near 2kHz and 3kHz also occurs. This information is given to the fundamental criteria to determine the filtering frequency in the proposed algorithm presented in the previous section. First, the magnitude of the mid frequency ranges from the 13th to 19th harmonics is increased. Second, a larger increase of the harmonics is indicated in the higher load current condition. This means that arc detection is easier under heavy load conditions. Third, the large current error near the ZCPs cannot be avoided. This is due to the fact that the input voltage is distorted so that its magnitude is zero in the regions. Since fewer current errors are detected in other regions, this can be worked as an important indicator for arc detection. This supports the role of the pre-processor in the proposed method.

With the above analysis, the simulation results of the proposed arc detection algorithm are shown in Fig. 14. In Fig. 14(*a*), the load condition is assumed as 660W. At t=0.05s, the series arc is generated, and v_i decreases as previously analyzed. Simultaneously, the current distortion near the ZCPs starts. After that, the magnitude of the series arc indicator δ_C increases so that the series arc can be detected. Fig. 14(*b*) shows the simulation results for the 1320W load condition. In this case, the input current distortion is more severe than in the previous condition, and δ_C is much larger than before. Consequently, it is supposed that the series arc detection performance is better.



(a)



(b)

Fig. 14. Simulation result of the proposed method. (a) 660W. (b) 1320W.

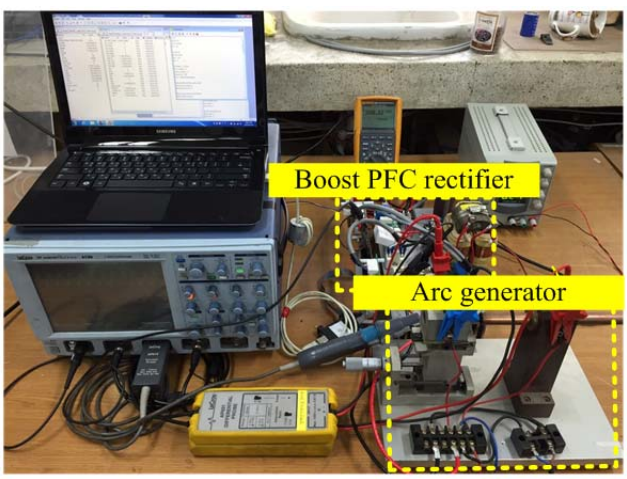
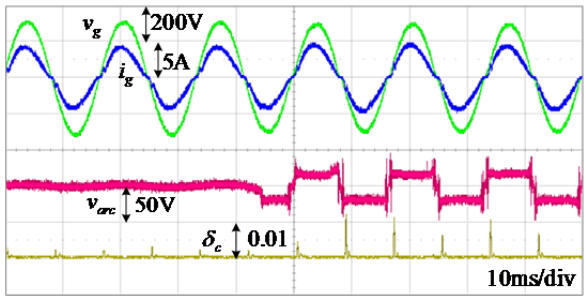


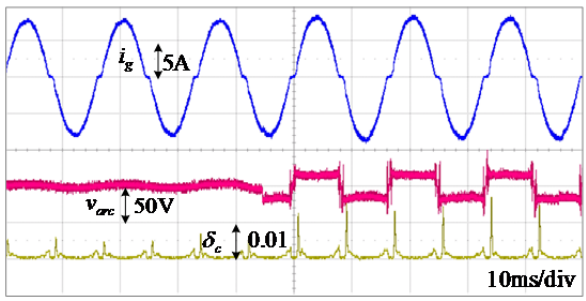
Fig. 15. Experimental configuration.

V. Experimental Results

In order to verify the effectiveness of the series arc detection algorithm, a 2kW PFC boost rectifier prototype whose parameters are the same as the ones in Table II has been built and tested. For the algorithm implementation, a Texas Instruments' 32 bit digital signal controller (TMS320F28335) has been employed. The control board equips a 4-channel digital to analog converter (DAC) to monitor the internal variables in real time. The power stage uses Semikron's IGBT modules. The arc generator was built under the guidance of the UL1699 standard. The length of air-gap can be easily changed by adjusting the knob so that the depth of the series arc can be managed. The entire experimental setup, including the PFC boost rectifier and the arc generator, is shown in Fig. 15.

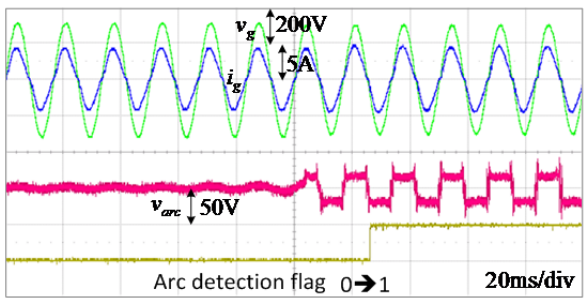


(a)

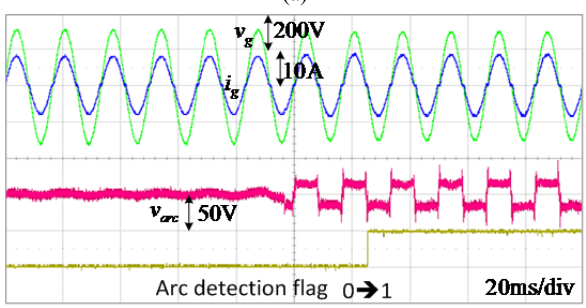


(b)

Fig. 16. Experimental results of the proposed algorithm. (a) 660W. (b) 1320W.



(a)



(b)

Fig. 17. Series arc fault detection performance. (a) 660W. (b) 1320W.

Fig. 16 shows the experimental results of the proposed algorithm under 660W and 1320 load conditions. In the test, the series arc was created by the arc generator at 0.045s. Consequently, the arc voltage turns up as in the figure. Although the current distortion after the series arc is barely distinguishable, δ_c clearly indicates the series arc fault signals in both cases. It should be noticed that the average value of δ_c in the 1320W condition is higher than that in the 660W condition. This means that arc detection in the higher load

condition is easier than in the lower load condition. However, the potential for misreading can also be increased. That is why the normalizing process in Fig. 6 is necessary in the proposed method.

The arc detection performances under the 660W and 1320W load conditions are shown in Fig. 17. In both cases, the series arc can be detected in 0.025s. This almost corresponds to one and a half cycles of the fundamental period. According to the UL1699 standard [19], at least four sequential cycles are necessary before arc detection devices can judge if true arc faults have occurred. Since the proposed method can detect a series arc in one and half cycles, it can be easily modified to meet the UL1699 standard.

VI. CONCLUSION

A series arc fault detection algorithm for single-phase boost rectifiers has been proposed in this paper. The method mainly utilizes the peak voltage variation and harmonic contents in the phase current. The virtual *dq* transformation is adapted to detect the peak voltage, and multiple combinations of LPFs and the HPFs are introduced for the series arc detection. Additionally, a series arc fault model has been proposed to simply model the phenomenon of series arc faults. To verify the proposed algorithm, simulations and the experiments using a boost PFC rectifier were performed. Both the simulation and experimental results agree very well with the analyses. The proposed method was also tested under the UL1699 standard for series arc detection, and this shows the detection capability of series arc faults of less than 3A current which is a 1.66 times worse condition when compared to the standard.

ACKNOWLEDGMENT

This work was supported by the Power Generation & Electricity Delivery of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korea government Ministry of Knowledge Economy (No. 20131020400960).

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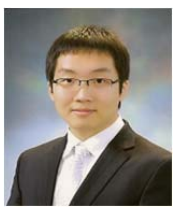

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