

Harmonic Elimination and Reactive Power Compensation with a Novel Control Algorithm based Active Power Filter

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Abstract

This paper presents a power system harmonic elimination using the mixed adaptive linear neural network and variable step-size leaky least mean square (ADALINE-VSSLLMS) control algorithm based active power filter (APF). The weight vector of ADALINE along with the variable step-size parameter and leakage coefficient of the VSSLLMS algorithm are automatically adjusted to eliminate harmonics from the distorted load current. For all iteration, the VSSLLMS algorithm selects a new rate of convergence for searching and runs the computations. The adopted shunt-hybrid APF (SHAPF) consists of an APF and a series of 7th tuned passive filter connected to each phase. The performance of the proposed ADALINE-VSSLLMS control algorithm employed for SHAPF is analyzed through a simulation in a MATLAB/Simulink environment. Experimental results of a real-time prototype validate the efficacy of the proposed control algorithm.

Key words: Adaptive linear neural network, Digital control, Harmonic elimination, Shunt-hybrid active power filter, Variable step-size leaky least mean square

I. INTRODUCTION

Current harmonics have become a major issue in distribution network because of the wide power electronic device applications in the industry. To overcome the current harmonic related problems, passive filters are connected in different configurations that represent a low cost solution [1], [2]. However, this mechanism has few drawbacks, such as resonance, size, instability, and inability to compensate for the changing harmonic current contents, which deject their implementation. To resolve these issues, an active filtering approach called active power filter (APF) was introduced as an advanced technique for harmonics elimination and reactive power compensation [3]-[7]. Nonetheless, the main disadvantage in using this approach is that the cost of power electronic inverters is high, especially for high power ratings. Moreover, APF is difficult to implement in high-voltage applications. Another harmonic mitigation solution called

shunt-hybrid APF (SHAPF) topology was investigated and introduced [8]-[10]. SHAPF is formed by the connection of an APF with one or more passive filters in a series. This type of configuration significantly reduces the rating. Passive filters absorb the harmonics injected by the nonlinear load and suppress the switching ripples generated from APF, which in turn enhances the filtering performance of the passive filter.

The generation of references in the form of voltage or current is the essential aspect of active filter control. The control strategies in frequency-domain include the fast Fourier method [11], the Kalman filter [12], and the wavelet transform. The frequency-domain approach requires large memory, slow response, and additional computational power. Moreover, this method may provide imprecise results during transient conditions. Time-domain approaches, such as d-q and p-q transformations, are based on the measurements and transformation of three-phase quantities [7]-[10]. However, these three- to two-phase transformations fail to work properly under unbalanced conditions [3], [13]. A recent study proposed a fast adaptive linear neural network (ADALINE) based time-domain approach for extracting the fundamentals from the distorted current [3]-[6].

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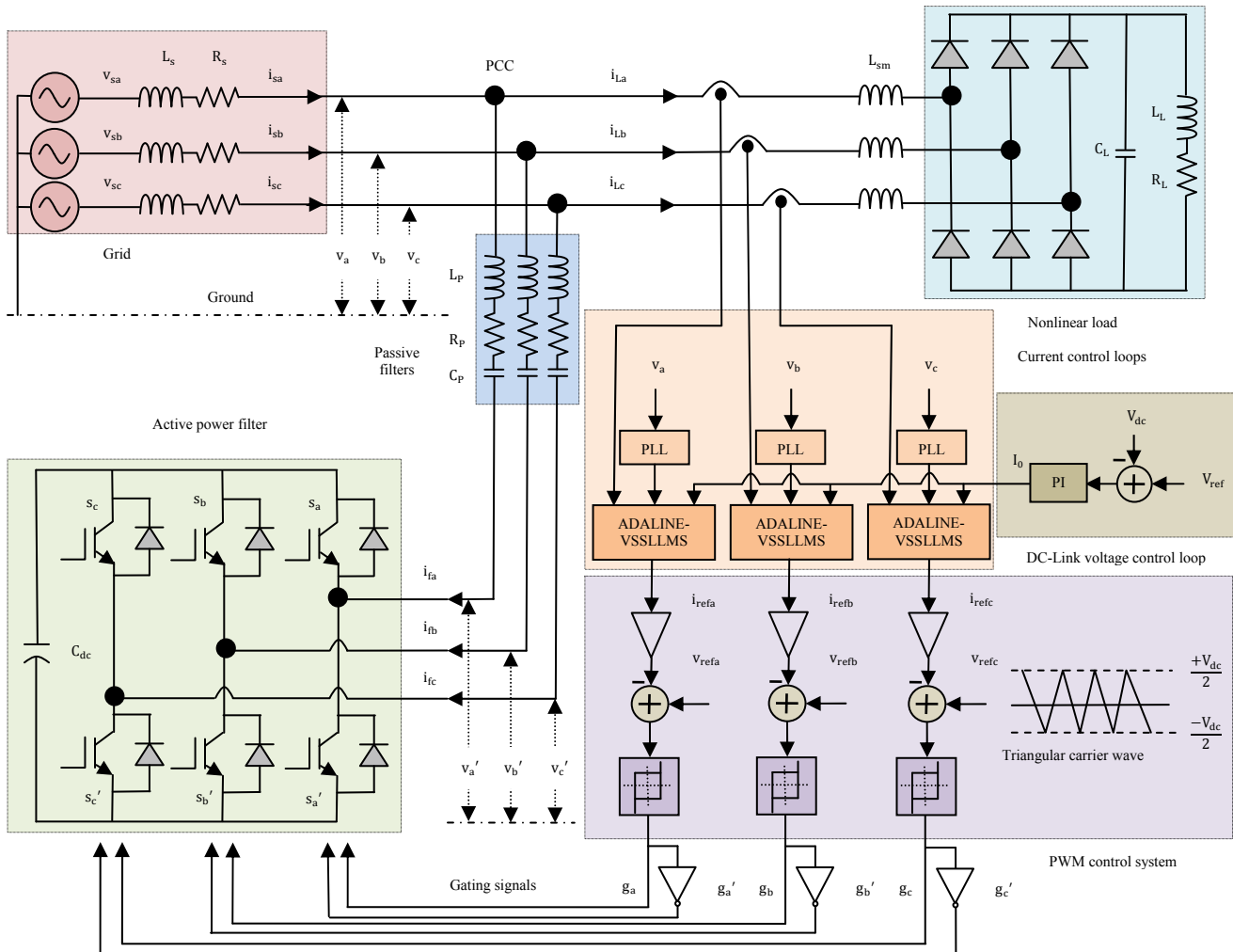


Fig. 1. Structure of the three-phase SHAPF.

The weights of ADALINE are generally updated using the least mean square (LMS) recursive algorithm [14]-[16].

This algorithm is commonly used in signal processing and control system application because of its simplicity and robustness. The rate of convergence of LMS algorithm directly depends on the fixed step-size parameter [17]. During steady state operations, a large step-size leads to a large offset and fast convergence rate, whereas a small step-size results in a slow convergence rate and small offset. These drawbacks can be addressed by implementing a time varying step-size. In the variable step-size LMS (VSSLMS) algorithm, step-size is dynamically adjusted during convergence [17], [18].

The eigenvalue decomposition of the autocorrelation matrix sometimes produces a zero eigenvalue, which causes the LMS adaptive filter to have undamped modes. These modes make the system unstable and should therefore be pushed to zero. In this event, a leakage factor is introduced in the autocorrelation matrix [19]-[21]. Implementing a leaky adjustment technique makes the convergence rate faster than the conventional LMS algorithm in case of a high input

eigenvalue spread.

In this study, a new design of SHAPF that employs mixed ADALINE-VSSLLMS algorithm is proposed. Three ADALINES in each phase are used to extract the harmonics and reactive components from the sensed load currents. A pulse width modulation control technique is used to generate gating pulses for the insulated gate bipolar transistors (IGBTs). Extensive simulations are conducted to emphasize the efficacy of the investigative results and the admirable performance of the proposed ADALINE-VSSLLMS control algorithm. Finally, the results are verified by implementing the proposed control algorithm in real-time using a SPARTAN-3A DSP processor.

The rest of the paper is organized into six sections. Following the Introduction, Section II describes the complete structure of SHAPF. Section III presents the mathematical equations of the proposed control algorithm. Section IV discusses the simulation results of SHAPF under different load conditions. Section V explains the development of a laboratory prototype model and the corresponding experimental results. Finally, Section VI describes the

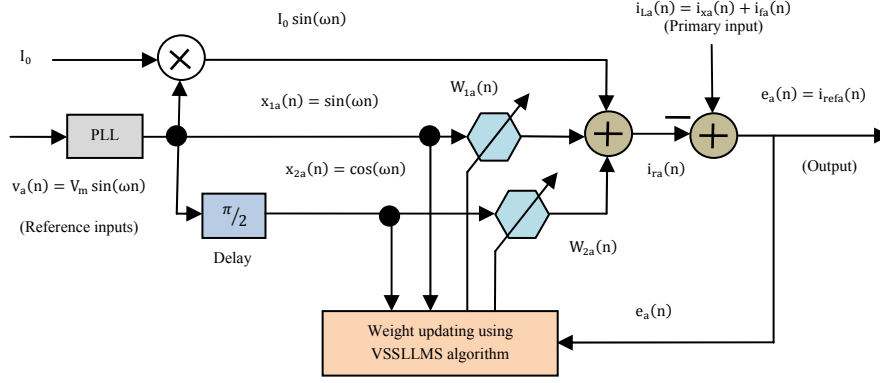


Fig. 2. Block diagram of ADALINE-VSSLLMS based reference signal generation in phase-a.

conclusion of the study.

II. SYSTEM DESCRIPTION

Fig. 1 shows the configuration of SHAPF. The low-rated APF and 7th tuned passive filters are connected directly to the AC-mains without using a coupling transformer. The 7th tuned passive filter provides a lower impedance path for the 11th and 13th harmonic frequencies as compared to 5th tuned passive filter, thereby resulting in a satisfactory filtering performance. Moreover, designing the 5th tuned passive filter is heavy, bulky, and expensive than the 7th tuned because of its large capacitance C_p value.

APF is a three-phase voltage source inverter consisting of six switches and a DC-link capacitor (C_{dc}). A PI controller is employed to charge the DC-link capacitor to the desired voltage level. The nonlinear load comprises a diode bridge rectifier followed by a capacitor with an inductive load (R_L, L_L). The SHAPF, which employs the proposed control technique, is designed to detect its harmonics and reactive components and inject a filter current identical with the load harmonic current. The three-phase source voltages measured at the point of common coupling are (v_a, v_b , and v_c). The three-phase source currents, three-phase load currents, and three-phase SHAPF currents are denoted as (i_{sa}, i_{sb} and i_{sc}), (i_{La}, i_{Lb} and i_{Lc}), and (i_{fa}, i_{fb} and i_{fc}), respectively.

III. MIXED ADALINE-VSSLLMS BASED HARMONIC AND REACTIVE COMPONENT ELIMINATION

The load current $i_{La}(t)$, including the harmonics, can be described using a Fourier series as follows:

$$i_{La}(t) = \sum_{n=1}^N I_n \sin(n\omega t + \phi_n) = i_{DC,a}(t) + i_{AC,a}(t) \quad (1)$$

where $i_{DC,a}(t)$ is the fundamental or DC current component, and $i_{AC,a}(t)$ is the sum of all harmonics or AC current components of the load current. If the reactive component is simultaneously compensated by APF, then $i_{DC,a}(t)$ can be further divided into two terms shown below.

$$i_{DC,a}(t) = I_1 \cos \phi_1 \sin \omega t + I_1 \sin \phi_1 \cdot \cos \omega t$$

$$= i_{xa}(t) + i_{ya}(t) \quad (2)$$

where $i_{xa}(t)$ and $i_{ya}(t)$ are the active and reactive components of the fundamental load current, respectively. Combining Eqs. (1) and (2) yields the following expression:

$$i_{La}(t) = i_{xa}(t) + i_{ya}(t) + i_{AC,a}(t) = i_{xa}(t) + i_{fa}(t) \quad (3)$$

The compensating current component $i_{fa}(t)$ can be derived as

$$i_{fa}(t) = i_{La}(t) - i_{xa}(t) = i_{La}(t) - [w_{1a}, w_{2a}]v_a(t) \quad (4)$$

where $W = [w_{1a}, w_{2a}]$ is the weight vector of ADALINE.

Fig. 2 shows the block diagram of the ADALINE-VSSLLMS control algorithm for reference signal generation. This algorithm is composed of two neurons whose weights $w_{1a}(n)$ and $w_{2a}(n)$ are updated online by the VSSLLMS algorithm. The input of each neuron is fed by the sinusoidal $x_{1a}(n)$ and cosine $x_{2a}(n)$ reference inputs collected from the source voltage $v_a(n)$ by the phase locked loop circuit. The difference between the primary nonlinear load current $i_{La}(n)$ and the estimated components $i_{ra}(n)$ induces an error signal $e_a(n)$. The weights of ADALINE are updated based on the VSSLLMS algorithm [19]-[21].

$$\begin{aligned} w_{1a}(n+1) &= (1 - 2\Delta(n)\gamma_{1a}(n))w_{1a}(n) + \Delta(n)e_a(n)x_{1a}(n) \\ w_{2a}(n+1) &= (1 - 2\Delta(n)\gamma_{2a}(n))w_{2a}(n) + \Delta(n)e_a(n)x_{2a}(n) \end{aligned} \quad (5)$$

where $\Delta(n)$ is the variable step-size parameter, and $\gamma(k)$ is the variable leakage factor. When $\gamma(k) = 0$, it behaves as a conventional LMS algorithm. The leakage factor is set to be large enough at the transient state to expedite the rate of convergence, but is reduced at the steady state. The variable step-size can be calculated as [17], [18]

$$\begin{aligned} \Delta(n+1) &= \alpha\Delta(n) + \gamma_{1a}(n)R(n)^2 \\ \Delta(n+1) &= \alpha\Delta(n) + \gamma_{2a}(n)R(n)^2 \end{aligned} \quad (6)$$

where α and γ are constant values controlling the convergence time, and $R(n)$ is the autocorrelation of $e_a(n)$ and $e_a(n-1)$. This autocorrelation can be expressed as follows:

$$R(n) = \beta R(n-1) + (1 - \beta)e_a(n)e_a(n-1) \quad (7)$$

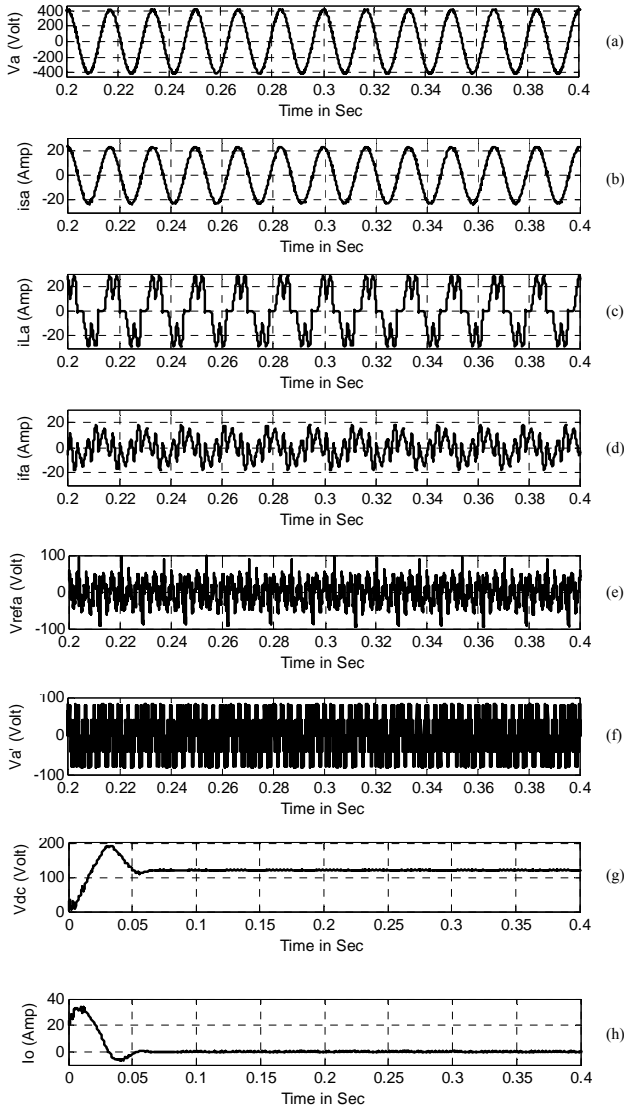


Fig. 3. Steady state waveforms of SHAPF; (a) source voltage v_a , (b) source current i_{sa} , (c) load current i_{La} , (d) SHAPF current i_{fa} , (e) reference voltage v_{refa} , (f) output of inverter voltage v_a' , (g) DC-link capacitor voltage v_{dc} , and (h) DC-current I_0 .

where β is an exponential weighting parameter. The variable leakage factor $\gamma(k)$ can be adjusted with the below equations.

$$\begin{aligned} \gamma_{1a}(n+1) &= \gamma_{1a}(n) - 2\rho\Delta(n)e_a(n)x_{1a}(n)^T w_{1a}(n-1) \\ \gamma_{2a}(n+1) &= \gamma_{2a}(n) - 2\rho\Delta(n)e_a(n)x_{2a}(n)^T w_{2a}(n-1) \end{aligned} \quad (8)$$

ADALINE-VSSLLMS aims to minimize the error and determine an optimal weight vector. Hence, $i_{ra}(n)$ approximates $i_{xa}(n)$. The residual error can be obtained as

$$e_a(n) = i_{fa}(n) + [i_{xa}(n) - i_{ra}(n)] \quad (9)$$

The cost function $J(n)$ is defined as follows:

$$J(n) = E\{e_a^2(n)\} = E[i_{fa}^2(n)] + E[i_{xa}(n) - i_{ra}(n)]^2 + 2E[i_{fa}(n)i_{xa}(n) - i_{fa}(n)i_{ra}(n)] \quad (10)$$

where $E\{\cdot\}$ is the statistical expectation operator, and

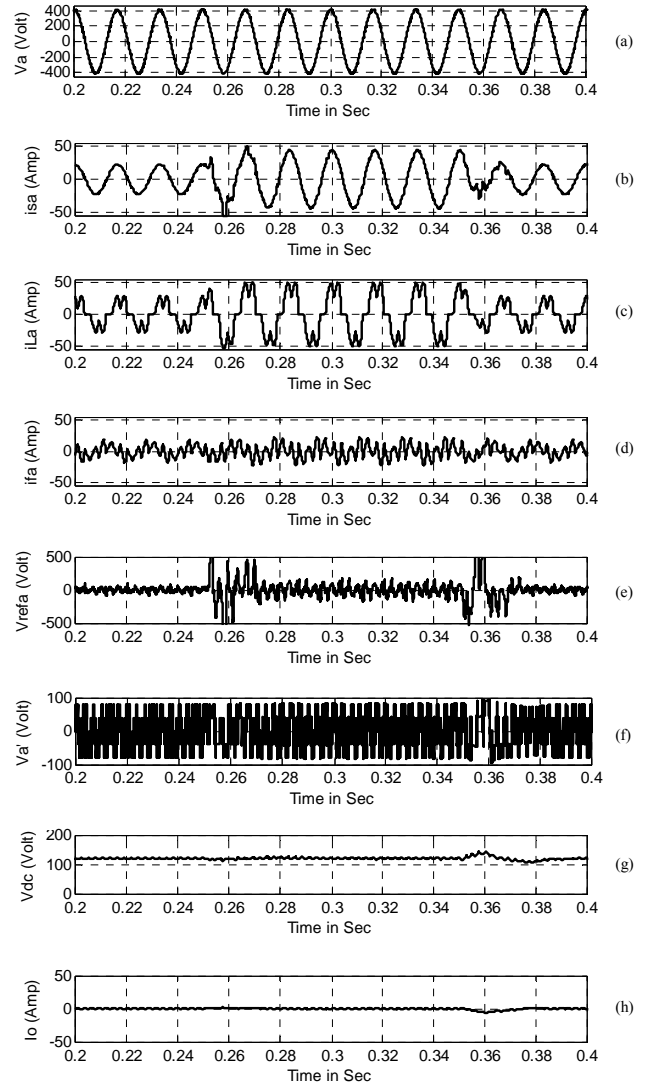


Fig. 4. Dynamic response under sudden load variations; (a) source voltage v_a , (b) source current i_{sa} , (c) load current i_{La} , (d) SHAPF current i_{fa} , (e) reference voltage v_{refa} , (f) output of inverter voltage v_a' , (g) DC-link capacitor voltage v_{dc} , and (h) DC-current I_0 .

$i_{fa}(n)$ is uncorrelated with $i_{xa}(n)$ and $i_{ra}(n)$ because of the orthogonality of trigonometric functions. When $i_{xa}(n) = i_{ra}(n)$, the following expression is obtained:

$$J(n)_{\min} = E[e_a^2(n)]_{\min} = E[i_{fa}^2(n)] \quad (11)$$

The preceding equation is the best mean square estimation of $i_{xa}(n)$. When this condition is achieved, the references are estimated successfully [4].

IV. SIMULATION STUDIES

The newly developed ADALINE-VSSLLMS control algorithm for harmonics elimination is designed, modeled, and simulated in a MATLAB/Simulink environment. The device parameters employed in the simulation studies are given in the Appendix, and the initial parameters are $\Delta =$

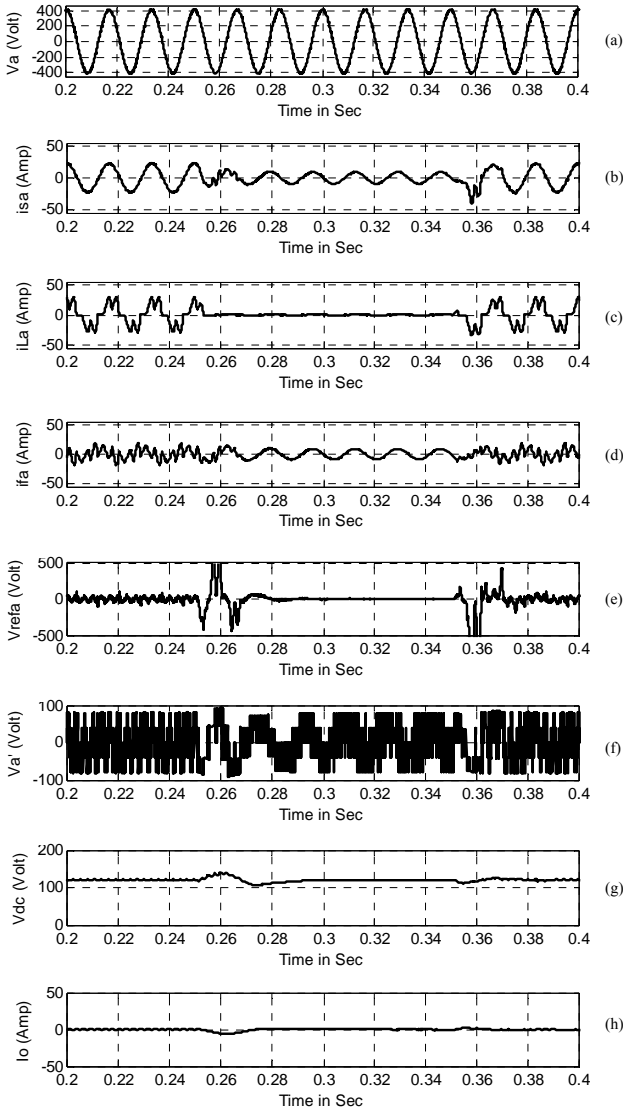


Fig. 5. Dynamic response under on- and off-load switching conditions; (a) source voltage v_a , (b) source current i_{sa} , (c) load current i_{La} , (d) SHAPF current i_{fa} , (e) reference voltage v_{refa} , (f) output of inverter voltage v_a' , (g) DC-link capacitor voltage v_{dc} , and (h) DC-current i_0 .

0.001, $\gamma = 0.01$, and $W = 0.018$.

The steady state response of SHAPF is presented in Fig. 3. The source voltage v_a , sinusoidal source current i_{sa} , nonlinear load current i_{La} , SHAPF current i_{fa} , reference voltage v_{refa} , output of inverter voltage v_a' , DC-link capacitor voltage v_{dc} , and reference current i_0 are depicted in Figs. 3(a) to (h), respectively. These figures illustrate that the source waveforms are of pure sinusoids and are in phase. The voltage across the capacitor is well balanced with an average value of 130 V. The maximum and minimum values of v_{dc} are 127 and 132 V, respectively. The magnitude of the reference current i_0 is zero.

Figs. 4(a) to (h) depict the dynamic response when a sudden step change of load occurs. The load resistance

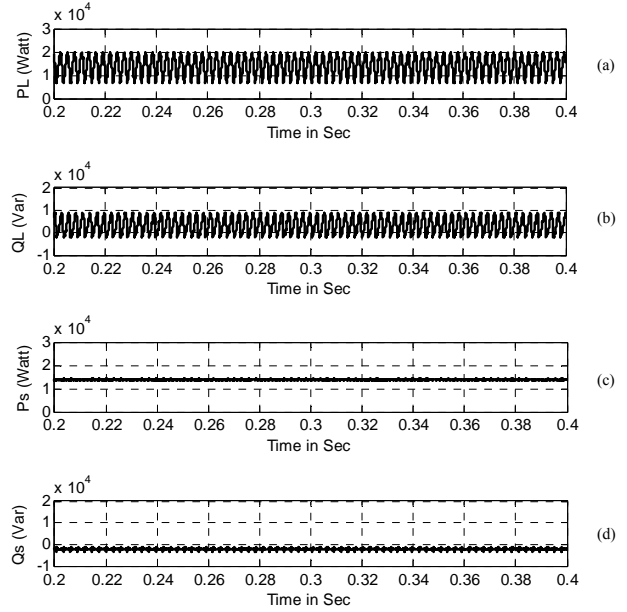


Fig. 6. Simulated waveforms; (a) instantaneous active power P_L on load side, (b) instantaneous reactive power Q_L on load side, (c) instantaneous active power P_s on source side, and (d) instantaneous reactive power Q_s on source side.

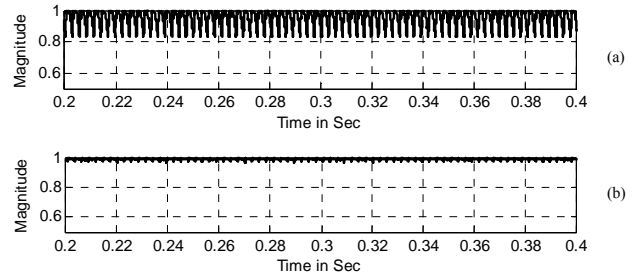


Fig. 7. Simulated waveforms of the system power factor; (a) before compensation, (b) after compensation.

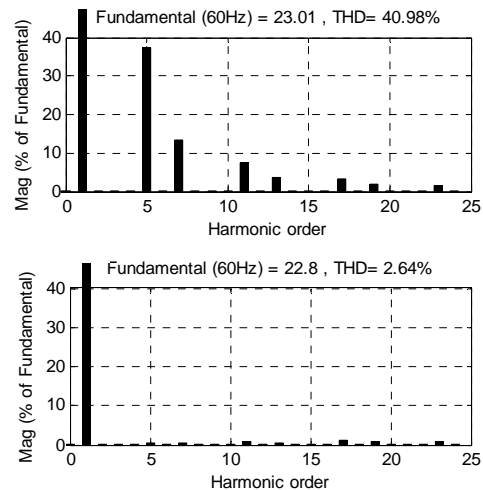


Fig. 8. Total harmonic distortion; (a) load current, (b) source current.

changes from 32Ω to 16Ω and from 16Ω to 32Ω at 0.25 and 0.35 S, respectively. The Fig. 4 evidently demonstrates that i_{sa} and v_{dc} exhibit a fast transient response, achieving a stable operation using the ADALINE-VSSLLMS control algorithm.

Figs. 5(a) to (h) show the dynamic response of SHAPF, which adopts the proposed controller, under on- and off-load switching conditions. A three-level variation is conducted on i_{La} (100% to 0%, steady at 0%, 0% to 100%). The SHAPF exhibits a fast response of one-time period to settle down to a new value. When i_{La} is set to zero, i_{sa} takes 0.016 S to maintain the equal i_{fa} . The DC-link capacitor charges to an over-shoot voltage of 140 V (7.69%) and to an under-shoot voltage of 125 V (3.84%) at the on- and off-load conditions, respectively.

Fig. 6 demonstrates the active and reactive powers on the load and source sides of the distorted power system. With SHAPF, the instantaneous active power is 1.48×10^4 W, and the reactive power is zero. The simulated waveforms of the system power factor are depicted in Fig. 7. The power factor is upgraded from 0.81 to 0.98 when SHAPF is connected.

The harmonic distortions of i_{La} and i_{sa} with the application of SHAPF are depicted in Figs. 8(a) to (b), respectively. During the steady state operation, the harmonic levels of i_{La} and i_{sa} are 2.64% and 40.98%, respectively. These values are well below the restrictions imposed by the IEEE standard 519-1992.

Table I presents the performance comparison of the individual harmonic amplitude (peak value) using the conventional ADALINE-LMS and the proposed ADALINE-VSSLLMS algorithm. The harmonic component elimination that employs the ADALINE-VSSLLMS algorithm exhibits better precision than that, which uses the conventional approach. Moreover, the computational time needed for the proposed algorithm is lesser than that for the conventional one.

V. REAL-TIME FPGA IMPLEMENTATION

To evaluate the performance of the proposed ADALINE-VSSLLMS control algorithm applied for SHAPF, a prototype model is developed using a SPARTAN-3A XC3SD1800A DSP processor and is certified in the laboratory as shown in Fig. 9. The experimental setup is composed of an SKKD 101/16 diode bridge rectifier fed inductive load that acts as a nonlinear load. A balanced three-phase supply is fed to the load through an auto-transformer and IGBT module PM25RSB120, which acts as a voltage source inverter. In this experimental setup, the source inductor, filter inductor, filter capacitor, and DC-link capacitor are set as 120 μ H, 1500 μ H, 137 μ F, and 2200 μ F respectively. The load resistance and inductance values are 100 Ω and 36 mH, respectively. The switching

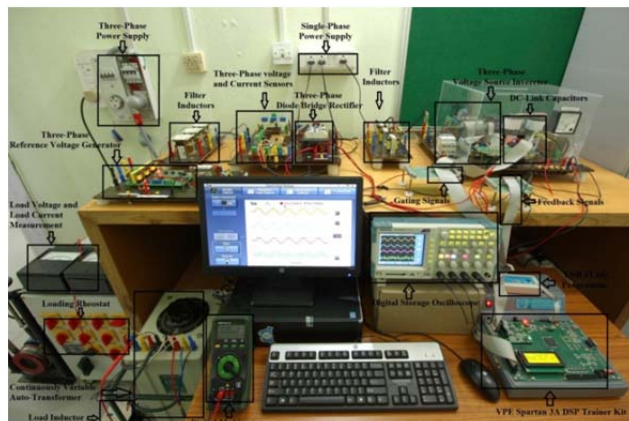


Fig. 9. Photograph of FPGA based experimental setup for implementing the proposed algorithm.

TABLE I
PERFORMANCE COMPARISON

Order of Harmonic	Load Current	Source Current using ADALINE-LMS	Source Current using ADALINE-VSSLLMS
5 th	8.64 A	0.21 A	0.11 A
7 th	3.12 A	0.19 A	0.13 A
11 th	1.72 A	0.26 A	0.21 A
13 th	0.83 A	0.19 A	0.15 A
17 th	0.75 A	0.28 A	0.24 A
19 th	0.47 A	0.27 A	0.18 A
23 th	0.38 A	0.31 A	0.21 A
25 th	0.32 A	0.21 A	0.16 A

frequency for the IGBT inverter is 10 KHz. LEM LV25-P and LEM LTS25-NP sensors are used to track the load currents and DC-link capacitor voltage, respectively. A signal conditioning circuit is designed to amplify and provide the necessary offset required by the analog to the digital converter circuit used. Table II describes the device utilization summary of the SPARTAN-3A XC3SD1800A DSP processor.

Figs. 10(a) to (f) show the steady state waveforms of the three-phase source voltages, three-phase load currents, three-phase source currents, three-phase compensated currents, switching signals, and DC-link capacitor voltage, respectively. Fig. 10(f) indicates that the DC-link capacitor voltage is regulated with regard to its reference value, and the output current of PI controller is set as zero. These conditions satisfy the essential requirements of SHAPF. The reactive power and harmonic components of the load currents are almost compensated by the generated SHAPF currents depending on the feedback signal fed to the control circuit. Therefore, the source current waveforms are almost pure sinusoidal with an input power factor of 0.96.

Figs. 11(a) to (c) demonstrate the experimental waveforms under the steady and dynamic states of load. The waveforms

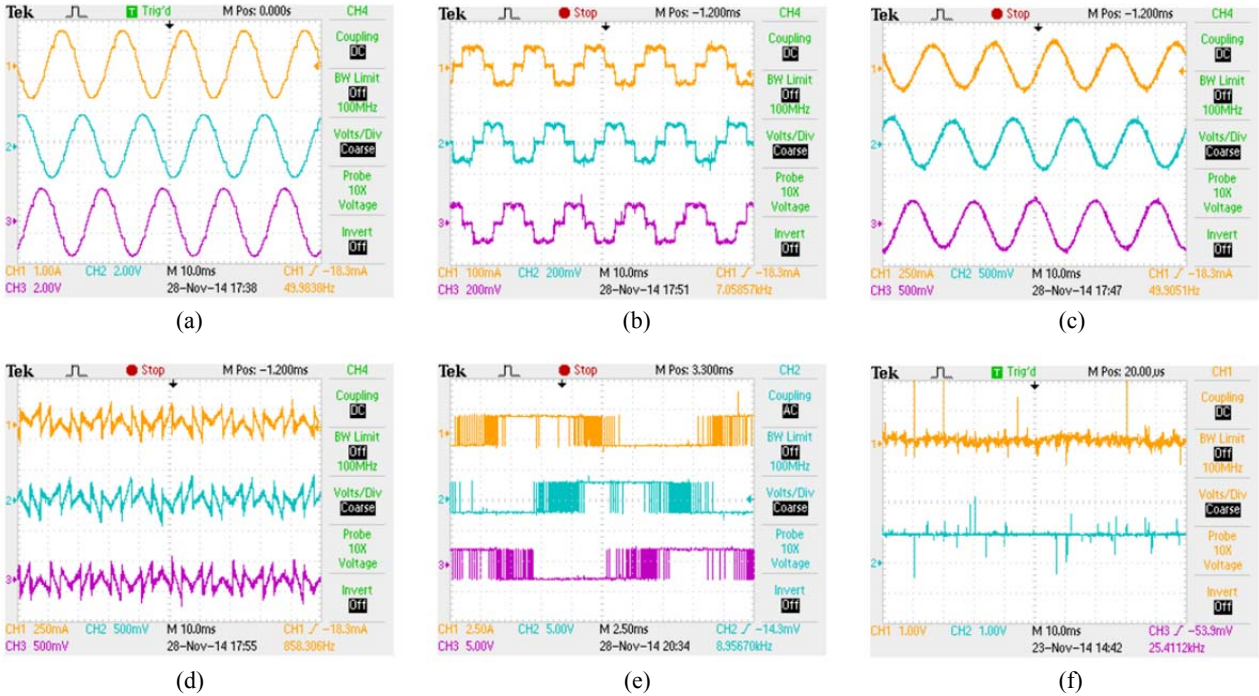


Fig. 10. Experimental results of SHAPF under the steady state condition; (a) source voltages (v_a, v_b, v_c), (b) load currents (i_{La}, i_{Lb}, i_{Lc}), (c) source currents (i_{sa}, i_{sb}, i_{sc}), (d) compensating currents (i_{fa}, i_{fb}, i_{fc}), (e) gating signals (g_a, g_b, g_c), and (f) DC current (I_0) and DC-link capacitor voltage (V_{dc}).

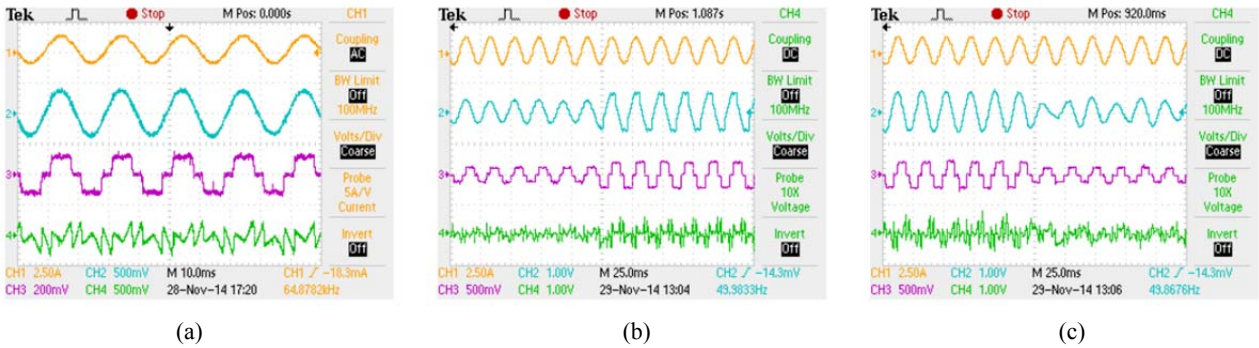


Fig. 11. Experimental waveforms of source voltage, source current, load current, and filter current (all values in phase-a); (a) steady state response of load, (b) and (c) dynamic response of SHAPF under sudden load variations

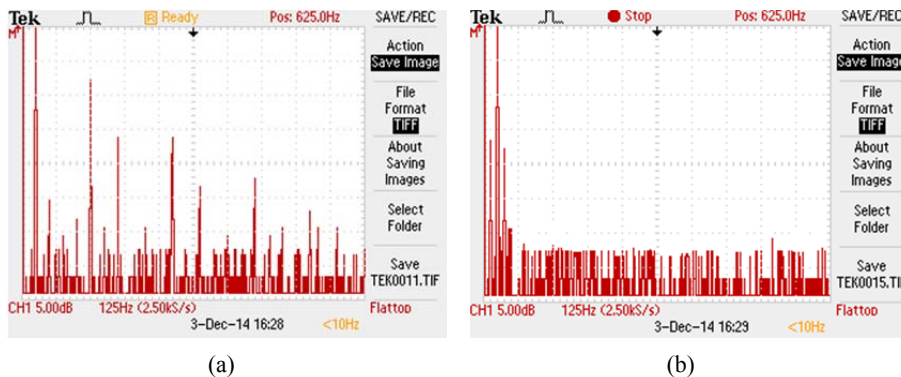


Fig. 12. Harmonic spectra; (a) load current, (b) source current.

TABLE II
DEVICE UTILIZATION SUMMARY

Logic Utilization	Used	Available	Utilization
No. of slice flip flop	1440	33280	4%
No. of four input LUTs	3950	33280	11%
No. of occupied slices	2460	16640	14%
No. of bonded IOBs	59	519	11%
No. of BUFGMUXs	3	24	12%
No. of DSP48As	25	84	29%
Average fan-out of non-clock nets	2.43		

in each figure, from top to bottom, represent the source voltage v_a , source current i_{sa} , load current i_{La} , and filter current i_{fa} , respectively. Fig. 11(b) shows the waveforms of SHAPF under the sudden changes of load from 2 KW to 1 KW, and Fig. 11(c) depicts the load changes from 1 KW to 2 KW. It has been observed that i_{sa} exhibits a fast transient response to settle down to a new value within a half-time period. The figures illustrate that both i_{sa} and V_a are maintained with pure sinusoidal and same phase by employing the proposed control technique.

The harmonic spectra of i_{La} and i_{sa} are presented in Figs. 12(a) to (b), respectively. These figures indicate that the amplitude of the individual harmonics is reduced significantly by employing SHAPF based on the ADALINE-VSSLLMS control algorithm.

VI. CONCLUSION

A novel mixed ADALINE-VSSLLMS control algorithm is presented for reference signal generation. The SHAPF based on proposed control algorithm has ability to compensate reactive power and eliminate harmonic components from the load currents. Both simulation and experimental results are analyzed to validate the efficacy of the proposed control algorithm. The findings reveal that the novel ADALINE-VSSLLMS approach is accurate, has fast convergence, and is stable at the dynamic changes of load in the power system. Given these advantages, the proposed control strategy can be a good solution for SHAPF, which requires adaptive characteristics and integrated functionalities.

APPENDIX

$V_s(\text{Peak}) = 420 \text{ V}$, $f = 60 \text{ Hz}$, $L_s = 0.1 \text{ mH}$, $R_s = 0.03 \Omega$, $C_L = 1500 \mu\text{F}$, $R_L = 36 \Omega$, $L_{sm} = 1.2 \text{ mH}$, $C_p = 57.6 \mu\text{F}$, $L_p = 2.5 \text{ mH}$, $R_p = 0.1 \Omega$, $C_{dc} = 1200 \mu\text{F}$, $V_{dcref} = 130 \text{ V}$, $K_p = 0.22 \Omega^{-1}$, $K_I = 22 \Omega^{-1}\text{S}^{-1}$.

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