JPE 15-6-21

http://dx.doi.org/10.6113/JPE.2015.15.6.1609
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Bidirectional Dual Buck-Boost Voltage Balancer with Direct Coupling Based on a Burst-Mode Control Scheme for Low-Voltage Bipolar-Type DC Microgrids

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Abstract

DC microgrids are considered as prospective systems because of their easy connection of distributed energy resources (DERs) and electric vehicles (EVs), reduction of conversion loss between dc output sources and loads, lack of reactive power issues, etc. These features make them very suitable for future industrial and commercial buildings' power systems. In addition, the bipolar-type dc system structure is more popular, because it provides two voltage levels for different power converters and loads. To keep voltage balanced in such a dc system, a bidirectional dual buck-boost voltage balancer with direct coupling is introduced based on P-cell and N-cell concepts. This results in greatly enhanced system reliability thanks to no shoot-through problems and lower switching losses with the help of power MOSFETs. In order to increase system efficiency and reliability, a novel burst-mode control strategy is proposed for the dual buck-boost voltage balancer. The basic operating principle, the current relations, and a small-signal model of the voltage balancer are analyzed under the burst-mode control scheme in detail. Finally, simulation experiments are performed and a laboratory unit with a 5kW unbalanced ability is constructed to verify the viability of the bidirectional dual buck-boost voltage balancer under the proposed burst-mode control scheme in low-voltage bipolar-type dc microgrids.

Key words: Bipolar-type DC microgrid, Burst-mode control, Dual buck-boost voltage balancer, N-cell, P-cell

I. INTRODUCTION

DC microgrids [1]-[14], compared with conventional ac microgrids, have attracted a lot of attention in the pursuit of effective solutions to meet modern energy distribution challenges. They can provide a better connection for dc output type sources such as photovoltaic (PV) systems, fuel cells, and energy storage devices (Li-ion batteries and super-capacitors, etc.). Moreover, system efficiency becomes higher for the lower conversion losses of the inverters between sources and loads, when loads are directly supplied with dc power. Other advantages are as follows: (1) no frequency stability or reactive power issues; (2) no skin effect or ac losses; (3) no downtime related to voltage sags or blackouts. Thus, they are very suitable for future industrial and commercial buildings' power systems, and for making our daily life efficient and secure.

Generally, there are two types of dc microgrids [1], [4]: unipolar-type and bipolar-type. The first type has only one voltage level in a two-wire dc distribution system. This makes it impossible to supply some types of loads at half voltage. The other type has two voltage levels in a three-wire system. This can provide a grounded neutral line, which is favorable for the security of people in domestic and office places. Additionally, bipolar-type systems have higher reliability due to the possibility of using a power supply under one line failure. This can also decrease power loss for reducing current levels and increasing power transmission capability.

As shown in Fig. 1, a low-voltage bipolar-type dc microgrid [1], [11] consists of a bidirectional rectifier, a voltage balancer, distributed energy sources (DERs) and dc/ac loads, where dc

Manuscript received Jan. 7, 2015; accepted Jun. 25, 2015
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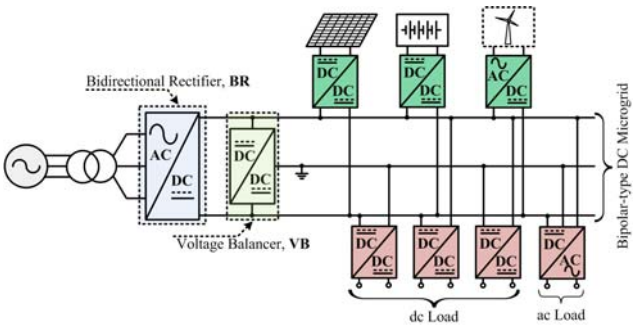


Fig. 1. Low-voltage bipolar-type dc microgrid structure.

power is transmitted through a three-wire system. The bidirectional rectifier can construct a unipolar-type system, and then a voltage balancer with the voltage balancing function is introduced to build a three-wire bipolar-type system. The voltage balancer can make the power supply flexible and reliable with two voltage levels for different loads in a bipolar-type dc microgrid. Compared with the unipolar-type dc grid, a voltage balancer is needed and additional loss can be produced in a bipolar-type dc grid.

This paper will focus on the research of a voltage balancer. The conventional topologies of bridge-type converters can suffer from a shoot-through risk, which is a major drawback to the reliability of this type of voltage balancer [4]. In addition, MOSFETs with lower switching loss and conducting loss cannot be used directly in conventional bridge converters due to the poorer characteristic of the MOSFET body-diode. Thus, a bidirectional dual buck-boost voltage balancer based on the P-cell and N-cell concepts is adopted in this paper [15]-[18]. Compared with the traditional bridge-type converter, it exhibits the following distinct merits [19]-[24]: (1) there is no shoot-through issue due to the fact that there are no active power switches connected in series in each phase leg; (2) the reverse recovery dissipation of the power switch is greatly reduced because there is no freewheeling current flowing through the body diode of the power switches which improves the reliability; (3) using MOSFETs combined with optimized diodes permits a higher switching frequency to reduce weight and volume. However, the bidirectional dual buck-boost voltage balancer has the disadvantage that two separate inductors are needed resulting in increased volume and weight. However, this can be mitigated by using the directly coupled inductor technique.

Generally, a voltage balancer is always working under constant-voltage mode control, resulting in additional power loss, such as converters' switching loss and conduction loss, especially under voltage balanced conditions. To increase system efficiency and reliability, a novel burst-mode control strategy is proposed for the dual buck-boost voltage balancer.

In this paper, a bidirectional dual buck-boost voltage balancer based on the P-cell and N-cell concepts is introduced in Section II, where a direct coupling inductor combined with a common inductor is presented to optimize the two separate

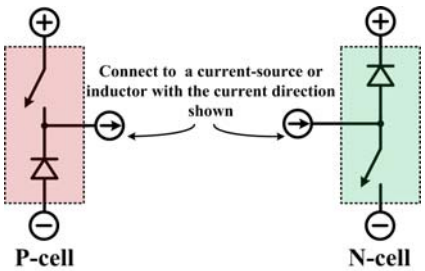


Fig. 2. Two basic switching cells: P-cell and N-cell.

inductors. The basic operation principle based on the continuous conduction mode (CCM) is also presented and analyzed in this section. In Section III, a novel burst-mode control strategy is proposed, where the operating principle and the current relations of the inductors, the capacitors and the unbalanced loads are analyzed in detail. In Section IV, an average small-signal model of the voltage balancer under the CCM condition is given to design the control system parameters. In Section V, a 10kW simulation experiment is carried out to validate the feasibility of the proposed burst-mode control strategy for the voltage balancer. In Section VI, a laboratory unit with a 5kW unbalanced ability is constructed to verify the viability of the proposed burst-mode control strategy for the dual buck-boost voltage balancer in low-voltage bipolar-type dc microgrids. Finally, some concluding remarks are drawn in Section VII.

II. Bidirectional Dual Buck-Boost Voltage Balancer with Direct Coupling

The concept of a "low-voltage bipolar-type dc microgrid" with a higher power supply quality is shown in Fig. 1, where medium voltage is converted into dc voltage in a range from 360V to 400V through a step-down transformer and an active-front-end rectifier. The three-wire dc distribution consisting of a positive line, a neutral line and a negative line is constructed by the voltage balancer, which provides two different voltage levels for customers. The load-side dc-dc/dc-ac converters can be connected between the positive line and the negative line, the positive line and the neutral line, the negative line and the neutral line separately. Since the latter two connections may cause power and voltage imbalances between the positive-neutral and the negative-neutral lines, it is essential to adopt dc voltage balance control. The voltage balancer is placed near the bidirectional rectifier to balance the positive and negative voltage, which can also be placed near the load side.

A. Bidirectional Dual Buck-Boost Voltage Balancer Based on P-cell and N-cell

Power electronics circuits can be constructed with two basic switching cells defined as P-cell and N-cell [16] [17], as shown in Fig. 2. Each cell consists of one switching device (a MOSFET, IGBT or any other switching device) and one diode

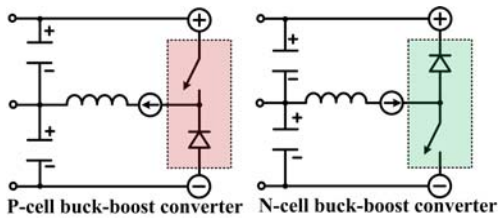


Fig. 3. Buck-boost converters based on basic switching cells.

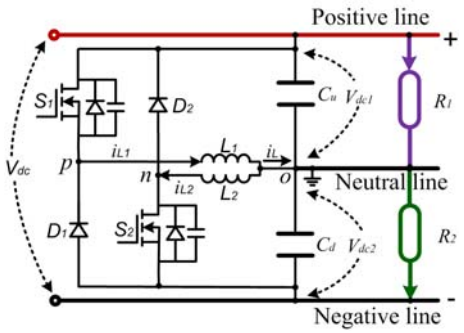


Fig. 4. Bidirectional dual Buck-boost voltage balancer.

constituting three terminals: (+) which is connected to the positive of a voltage-source or capacitor, (-) which is connected to the negative of a voltage-source or capacitor, and a common terminal which is shown as (→) or (←). For the P-cell, this common terminal is connected to the negative terminal of a current source or inductor. For the N-cell, the common terminal is connected to the positive of a current source or inductor.

Fig. 3 shows the buck-boost converters based on the basic switch cells. It can be seen that the P-cell buck-boost converter can only transfer power from upside to downside, and the N-cell buck-boost converter from downside to upside. Thus, by combing the former two converters, a bidirectional dual buck-boost converter can be obtained forming a voltage balancer, as shown in Fig. 4. The voltage balancer consists of the P-cell leg (S_1, D_1), the N-cell leg (S_2, D_2), separate inductors (L_1, L_2), and two split dc bus capacitors (C_u, C_d). MOSFETs are used as power switches here, and their body diodes never work. Thus, both the power switches and the power diodes can get an optimized design independently. This permits a higher switching frequency to reduce the weight and volume.

As shown in Fig. 4, V_{dc1}, V_{dc2} and V_{dc} stand for the positive-neutral, negative-neutral and positive-negative voltages, respectively. In the following analysis, it is assumed that V_{dc} is kept constant with the regulation by the bidirectional rectifier.

B. Mathematical Model in the Rotor Reference Frame

To overcome the drawback of the bidirectional dual buck-boost converter, where two separate inductors are needed resulting in more volume and weight, the directly coupled inductor technique combined with a common inductor is adopted, as shown in Fig. 5. The equivalent inductance L_{pn} is

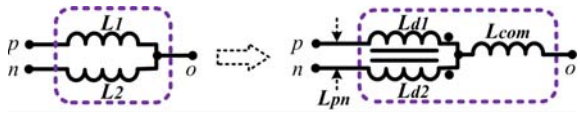


Fig. 5. The directly coupled inductor technique combined with the common inductor.

four times each phase inductance (L_{d1}, L_{d2}) using the direct coupling technique. The inductor L_{pn} between S_1 and S_2, and the stray inductance L_S of the interconnections will limit the current i_{pn} if there is any overlap in the switching of the P-cell and N-cell devices.

It is assumed that the overlap time is limited to below some value Δi_{limit}. Then, L_{pn} has the following relation:

$$\Delta i_{pn} = \frac{V_{dc}}{L_{pn} + L_S}\Delta t_{pn} < \Delta i_{\lim it} \Rightarrow L_{pn} > \frac{V_{dc}}{\Delta i_{\lim it}}\Delta t_{pn} - L_S \quad (1)$$

Depending on the system requirements, the directly coupled inductor can be optimized using Eq. (1).

Based on the current ripple analysis, the total inductance value ($L_{d1} + L_{com}$) can be obtained as:

$$L_{d1} + L_{com} = \frac{V_{dc1}}{2\Delta I_{LD} f_s} \quad (2)$$

where, f_s is the switching frequency and $V_{dc1} = V_{dc2}$. From Eq. (1), L_{d1} (L_{d2}) can be derived, and L_{com} can also be calculated under the condition that $\Delta I_{LD} \leq 20\% I_{L0}$ (I_{L0}-nominal operating current).

C. Basic Operation Principle under the CCM Condition

To simplify the analysis of the operation principle, some assumptions are made as follows: (1) all of the power MOSFETs and diodes are ideal devices with no consideration of the switching time or conduction voltage drop; (2) all of the inductors and capacitors are ideal with $L_{d1} = L_{d2}$ and $C_u = C_d = C$; (3) the output dc voltages (V_{dc1}, V_{dc2}) are constant during each switching process.

The reference direction of i_L is from the p terminal to the common terminal o. It can be seen that i_{L1} is as a positive current while i_{L2} as a negative current. Fig. 6 shows the four basic operation modes under the CCM condition.

1) Mode 1: When R_1 is bigger than R_2, the voltage V_{dc1} of the capacitor C_u will increase combined with a decrease of the voltage V_{dc2} of the capacitor C_d. At this moment, S_1 is turned on and the positive inductor current i_{L1} increases linearly. In this mode, the P-cell leg starts to transfer additional power to R_2 through L_1, as shown in Fig. 2(a).

2) Mode 2: When S_1 is turned off, i_{L1} continues to run through the freewheeling diode D_1, as shown in Fig. 2(b). The process is not be terminated until S_1 is turned on again.

3) Mode 3 and Mode 4: Conversely, when R_1 is smaller than R_2, S_2 is turned on and the negative current i_{L2} increases linearly. At this time, the N-cell leg starts to transfer the redundant power to R_1 through L_2, as shown in Fig. 2(c). Fig.

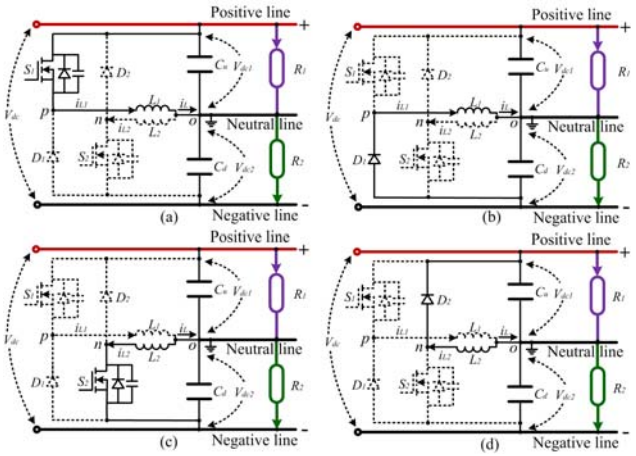


Fig. 6. Basic operation modes: (a) Positive current $i_L = i_{L1}$, S_1 turned on; (b) Positive current $i_L = i_{L1}$, D_1 free-wheeling; (c) Negative current $i_L = -i_{L2}$, S_2 turned on; (d) Negative current $i_L = -i_{L2}$, D_2 free-wheeling.

2(d) shows that i_{L2} continues to run through the freewheeling diode D_1 when S_2 is turned off.

III. The Novel Burst-Mode Control Scheme for a Bidirectional Dual Buck-Boost Voltage Balancer

Burst mode control has been widely used in PWM converters to achieve lower standby losses [25], [26]. It is an operation mode using the cycle-skipping technique to reduce the switching loss in a switching regulator and to increase the operating efficiency at low power levels. During a burst cycle, each burst of switching can be started at the lowest output voltage value (which occurs just at the start of a burst) and stopped at the maximum voltage value (which occurs at the end of a burst), and this process is repeated. This operation mode can result in high efficiency at low power levels, because the MOSFETs converters can operate at a designed power level close to the optimum efficiency point during a switching period.

Based on the idea of burst mode, a novel adaptive burst mode control scheme is proposed for the bidirectional dual buck-boost voltage balancer in low-voltage bipolar-type dc microgrids. Fig. 7 shows a simplified system control block diagram of this scheme. In the proposed adaptive burst mode control, there are three basic operation modes: P-cell mode (PCM), natural-balance-mode (NBM), and N-cell mode (NCM). The basic operational waveforms are shown in Fig. 8.

D. Three Operation Modes of the Proposed Burst Mode Control

1) P-cell mode (PCM): When R_1 is bigger than R_2, V_{dc1} increases and V_{dc2} decreases while V_{dc} is kept constant at the same time. After V_{dc2} touches the voltage lower limit V_{lower}, the P-cell leg switch S_1 works under the current mode control

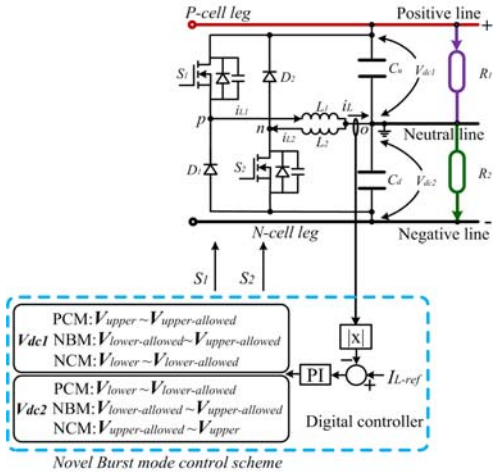


Fig. 7. Simplified control block diagram of burst mode control based on the bidirectional dual buck-boost voltage balancer.

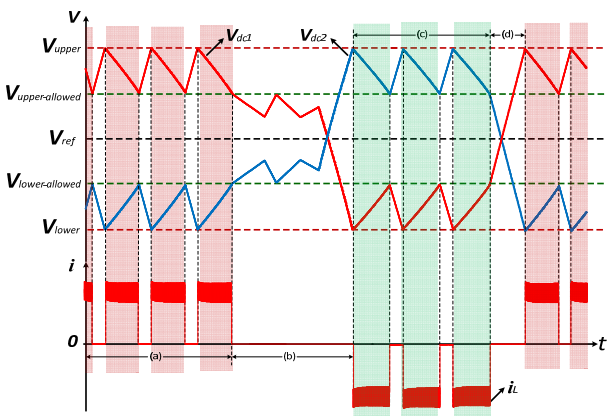


Fig. 8. The basic operational waveforms of three operation modes in the bidirectional dual buck-boost voltage balancer.

with the preset $i_{L\text{-}ref}$. Then, V_{dc2} begins to increase to the allowed voltage lower limit $V_{\text{lower-allowed}}$ during a burst-mode switching period, in which the voltage difference should satisfy the condition of $V_{upper\text{-}allowed} - V_{lower\text{-}allowed} < V_{dc1} - V_{dc2} < V_{upper} - V_{lower}$. After that, S_1 does not work until V_{dc2} reaches V_{lower} again. Operating in the P-cell mode, the positive inductor current i_L transfers the redundant power from the upside to the downside, as shown in Fig. 8(a).

2) Natural-balance mode (NBM): As shown in Fig. 8(b), when V_{dc1} and V_{dc2} are naturally maintained between the allowed voltage lower limit $V_{lower\text{-}allowed}$ and upper limit $V_{upper\text{-}allowed}$ without control, the voltage balancer does not work and i_L is zero at this time.

3) N-cell mode (NCM): When R_1 is smaller than R_2, V_{dc1} decreases and V_{dc2} increases while V_{dc} is kept constant at the same time. After V_{dc2} touches the voltage upper limit V_{upper}, the N-cell leg switch S_2 works under the current mode control with the preset $i_{L\text{-}ref}$. Then, V_{dc2} begins to decrease to the allowed voltage upper limit $V_{upper\text{-}allowed}$ during a burst mode switching period, in which the voltage difference should satisfy the condition of $V_{upper\text{-}allowed} - V_{lower\text{-}allowed} < V_{dc2} - V_{dc1} < V_{upper} - V_{lower}$. After that, S_2 does not work until V_{dc2} reaches

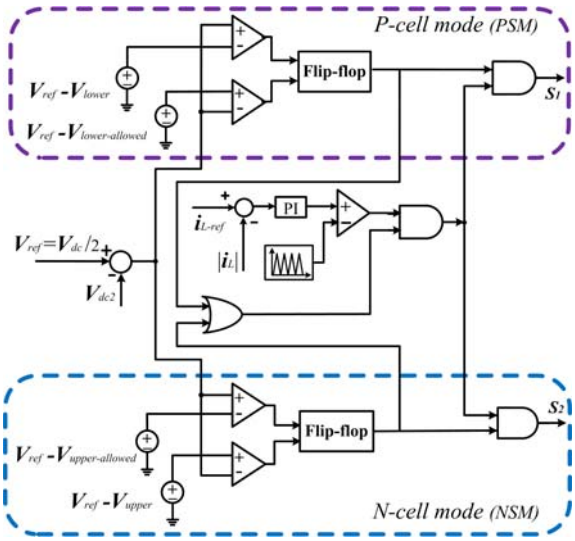


Fig. 9. Realization of the proposed burst mode control scheme.

V_{upper} again. Operating in the N-cell mode, the negative i_L transfers redundant power from the downside to the upside as shown in Fig. 8(c).

Because V_{dc1} and V_{dc2} should not higher than V_{upper} or less than V_{lower}, the switches (S_1, S_2) will work only when the dc voltage values (V_{dc1}, V_{dc2}) do not meet predetermined values. Then, a positive or negative intermittent i_L will exist to transfer the corresponding power between the two poles making the voltages balanced. Thus, the switching loss of the balancer will be effectively reduced and its efficiency will be improved. In addition, the switches of the P-cell leg and N-cell leg are controlled separately. This can avoid the power switches shoot-through problem in traditional bridge topological structures. In this case, high frequency MOSFETs switches can be used to reduce the system volume.

E. Realization of the Proposed Burst Mode Control Scheme

The realization of the proposed burst mode control scheme is presented in Fig. 9. V_{ref} is equal to half of the total dc voltage value V_{dc}. If R_1 is bigger than R_2, V_{dc1} increases combined with the decrease of V_{dc2}. When V_{dc2} is less than V_{lower}, the following is true V_{ref} - V_{dc2} > V_{ref} - V_{lower} and V_{ref} - V_{dc2} > V_{ref} - $V_{lower\text{-}allowed}$. At this time, the outputs of the two comparators in the P-cell mode are 1 and 0, respectively, and the outputs of the flip-flop and the OR gate are 1. The PWM current control regulates i_L tracking the reference current $i_{L\text{-}ref}$, with the outputs of the comparator and the OR gate sent to the AND gate together. When the output of the AND gate connected with the comparator is 1, a trigger signal will be sent to switch S_1 which will be turned on with a positive i_L. Operating in the P-cell mode, the P-cell leg will transfer redundant power from the upside to the downside, and then V_{dc2} will increase. When V_{dc2} goes up to the value of $V_{lower\text{-}allowed}$, there will be V_{ref} - V_{dc2} < V_{ref} - V_{lower} and V_{ref} - V_{dc2} < V_{ref} - $V_{lower\text{-}allowed}$. At this time, the outputs of the two comparators are 0 and 1, respectively. The output of the flip-flop is zero and the trigger signal of S_1 disappears. Then, S_1 is turned off and the voltage balancer stops working. As the operating procedures of S_2 are the same as those of S_1, the analysis process of S_2 is not given out.

F. Main Current Relationships of the Bidirectional Dual Buck-Boost Voltage Balancer

If R_1 is bigger than R_2, V_{dc1} goes up and V_{dc2} decreases at the same time. Since V_{dc} is kept constant through regulation by the bidirectional rectifier, the ripple voltage ΔV_{dc1} of V_{dc1} is also equal to the negative ripple voltage $-\Delta V_{dc2}$ of V_{dc2}.

$$\Delta V_{dc1} = \frac{1}{C_u}\int_{t_0}^{t_1} i_{C_u}\,dt = -\frac{1}{C_d}\int_{t_0}^{t_1} i_{C_d}\,dt = -\Delta V_{dc2} \tag{3}$$

If the two capacitors, C_u and C_d, are equal, $i_{C_u} = i_{C_d}$.

Since $i_L = i_{C_d} + i_{R2} - i_{C_u} - i_{R1}$, the following can be obtained:

$$i_L + i_{R1} = i_{R2} \tag{4}$$

If $(i_L + V_{dc1}/R_1) \times R_2 > V_{ref}$ is satisfied, either the voltage balancer will work normally to balance V_{dc1} and V_{dc2}, or the balancer will fail to work properly to balance V_{dc1} and V_{dc2}. On the premise of the balancer working normally, the balancer does not work all the time if $(i_L + V_{upper\text{-}allowed}/R_1) \times R_2 > V_{lower\text{-}allowed}$ is satisfied, and an intermittent inductor current i_L will exist. However, the balancer will always at work with a sustained i_L if $(i_L + V_{upper\text{-}allowed}/R_1) \times R_2 = V_{lower\text{-}allowed}$ is satisfied. When R_1 is infinity in extreme cases, R_2 should not be less than $V_{ref}/i_{L\text{-}ref}$, or the balancer will not work.

IV. The Average Small-Signal Model for the Bidirectional Dual Buck-Boost Voltage Balancer

In order to select the control system parameters, an average small-signal model of the voltage balancer under CCM is derived. The duty cycles of S_1 and S_2 are defined as d_1 $\left(d_1 = D_1 + \hat{d}_1\right)$ and d_2 $\left(d_2 = D_2 + \hat{d}_2\right)$, respectively, where D_1, D_2, $\hat{d}_1$ and $\hat{d}_2$ are the stable duty ratios and the perturbations of d_1 and d_2. Moreover, the voltage v_{dc2} and the inductance current i_{L1} are defined as $v_{dc2} = V_{dc2} + \hat{v}_{dc2}$ and $i_{L1} = I_{L1} + \hat{i}_{L1}$, where V_{dc2}, I_{L1}, $\hat{v}_{dc2}$ and $\hat{i}_{L1}$ are the stable voltage values, the current values and the perturbations of v_{dc2} and i_{L1}.

From Fig. 6, it is possible to obtain (5) and (6) when the P-cell bridge leg operates under CCM.

(1) S_1 turning on

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_{dc} - v_{dc2} \\ C_d \dfrac{dv_{dc2}}{dt} = i_{L1} + C_u \dfrac{d(V_{dc} - v_{dc2})}{dt} + \dfrac{V_{dc} - v_{dc2}}{R_1} - \dfrac{v_{dc2}}{R_2} \end{cases} \tag{5}$$

(2) S_1 turning off

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = -v_{dc2} \\ C_d \dfrac{dv_{dc2}}{dt} = i_{L1} + C_u \dfrac{d(V_{dc} - v_{dc2})}{dt} + \dfrac{V_{dc} - v_{dc2}}{R_1} - \dfrac{v_{dc2}}{R_2} \end{cases} \tag{6}$$

According to the methods of building the average model, it can be derived from (5) and (6):

$$\begin{cases} \dfrac{d\hat{i}_{L1}}{dt} = \dfrac{V_{dc}}{L_1}\hat{d}_1 - \dfrac{1}{L_1}\hat{v}_{dc2} \\ \dfrac{d\hat{v}_{dc2}}{dt} = \dfrac{1}{C_u + C_d}\hat{i}_{L1} - \dfrac{R_1 + R_2}{R_1 R_2 (C_u + C_d)}\hat{v}_{dc2} \end{cases} \tag{7}$$

Thus, the transfer function of the inductance current i_{L1} versus the duty cycle d_1 is represented by:

$$G_1(S) = \frac{\hat{i}_{L1}}{\hat{d}_1} = \frac{(2CR_1R_2s + R_1 + R_2)V_{dc}}{2L_1CR_1R_2s^2 + L_1(R_1 + R_2)s + R_1R_2} \tag{8}$$

From Fig. 8, (9) and (10) can be obtained when the N-cell bridge leg operates under CCM.

(1) S_2 turning on

$$\begin{cases} L_2 \dfrac{di_{L2}}{dt} = v_{dc2} \\ C_d \dfrac{dv_{dc2}}{dt} = -i_{L2} + C_u \dfrac{d(V_{dc} - v_{dc2})}{dt} + \dfrac{V_{dc} - v_{dc2}}{R_1} - \dfrac{v_{dc2}}{R_2} \end{cases} \tag{9}$$

(2) S_2 turning off

$$\begin{cases} L_2 \dfrac{di_{L2}}{dt} = -(V_{dc} - v_{dc2}) \\ C_d \dfrac{dv_{dc2}}{dt} = -i_{L2} + C_u \dfrac{d(V_{dc} - v_{dc2})}{dt} + \dfrac{V_{dc} - v_{dc2}}{R_1} - \dfrac{v_{dc2}}{R_2} \end{cases} \tag{10}$$

According to the methods of building the average model, (9) and (10) are rewritten by:

$$\begin{cases} \dfrac{d\hat{i}_{L2}}{dt} = \dfrac{V_{dc}}{L_2}\hat{d}_2 + \dfrac{1}{L_2}\hat{v}_{dc2} \\ \dfrac{d\hat{v}_{dc2}}{dt} = -\dfrac{1}{C_d + C_u}\hat{i}_{L2} - \dfrac{R_1 + R_2}{R_1 R_2 (C_d + C_u)}\hat{v}_{dc2} \end{cases} \tag{11}$$

Thus, the transfer function of the inductance current i_{L2} versus the duty cycle d_2 is represented by:

$$G_1(S) = \frac{\hat{i}_{L2}}{\hat{d}_2} = \frac{(2CR_1R_2s + R_1 + R_2)V_{dc}}{2L_2CR_1R_2s^2 + L_2(R_1 + R_2)s + R_1R_2} \tag{12}$$

Comparing (8) with (12), the open-loop transfer functions of the P-cell and N-cell bridge legs are the same. Using the following equation $G_2(s) = G_1(s)/[1 + G_1(s)]$, the closed-loop transfer functions $G_2(s)$ can also be achieved. The control system diagram of the voltage balancer can be illustrated by Fig. 10.

V. Simulation Results for the Bidirectional Dual Buck-Boost Voltage Balancer

To validate the aforementioned analysis, computer simulations of the output voltages and inductance currents are carried out in PISM software. The total power of the voltage balancer is 10kW and the switching frequency is 30 kHz. The other main simulation parameters are listed as follows: V_{dc} = 400V, V_{ref} = 200V, L_1 = L_2= 0.2mH, $i_{L\text{-}ref}$ = 50A, C_u = C_d = 10mF, V_{upper} = 202.2V, V_{lower} = 197.8V, $V_{upper\text{-}allowed}$ = 201.8V,

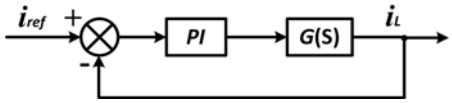
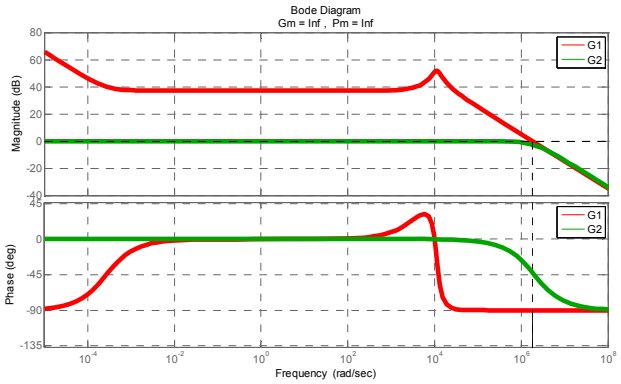
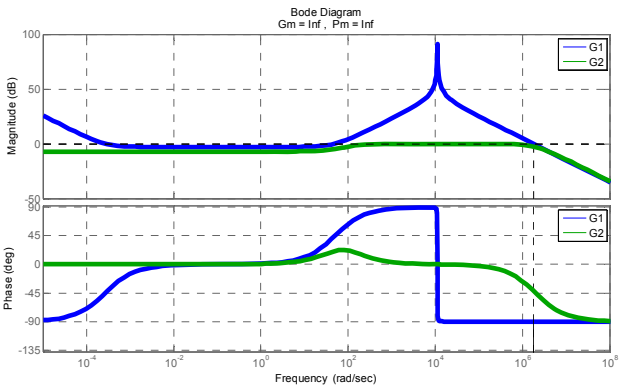


Fig. 10. Control system based on the current mode control.



(a)



(b)

Fig. 11. Bode diagram of the open-loop and closed-loop system transfer function: (a) R_1 = 5Ω, R_2 = 50MΩ; (b) R_1 = 500Ω, R_2 = 50MΩ.

and $V_{lower\text{-}allowed}$ = 198.2V. R_{dc1} and R_{dc2} will be given according to the simulation requirements in the following.

G. Analysis of the Control System Parameters

The PI parameters of the control system in Fig. 10 are K_p = 3.7 and K_i = 0.001. With the above simulation parameters, a Bode diagram of the control system is shown in Fig.1 1, where G_1 and G_2 represent the open-loop and closed-loop transfer functions, respectively. When the unbalanced loads are R_1 = 5Ω and R_2 = 50MΩ, that is to say, R_2 is infinite relative to R_1, the open-loop transfer function G_1(s) and the closed-loop transfer function G_2(s) are described in (13) and (14), respectively. In this case, a Bode diagram of the control system is shown in Fig. 11(a). When the unbalanced loads are R_1 = 500Ω and R_2 = 50MΩ, the open-loop transfer function G_1(s) and the closed-loop transfer function G_2(s) are described in (15) and (16), respectively. In this case, a Bode diagram of the control system is shown in Fig. 11(b). By analyzing the amplitude-frequency characteristic and phase-frequency response curves in the Bode diagram, where G_m = inf and P_m

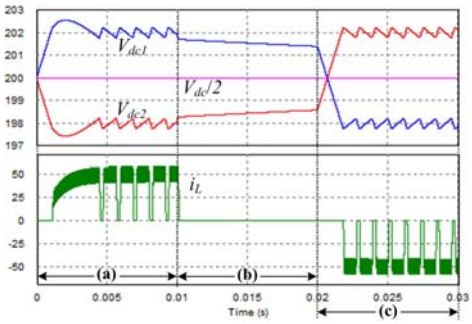


Fig. 12. Simulation results of the voltage and current relationships: (a) P-cell mode; (b) Natural-balance mode; (c) N-cell mode.

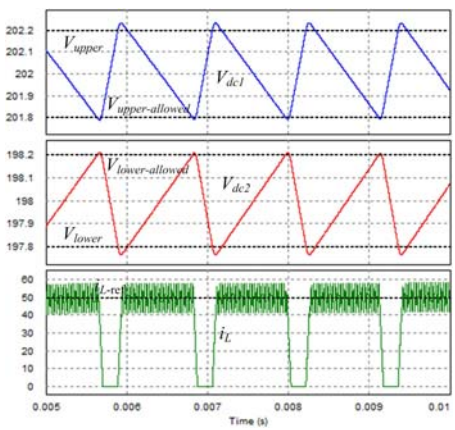


Fig. 13. Detailed simulation results of the voltage and current relationships in P-cell mode.

= inf indicate that the gain margin and phase margin are infinite, it can be seen that the given control system is stable.

$$G_1(S)=\frac{\hat{i}_L}{\hat{d}}=\frac{3.594\times10^3 s^2+1.797\times10^7 s+4858}{2\times10^{-3}s^3+10s^2+2.5\times10^5 s} \tag{13}$$

$$G_2(S)=\frac{\hat{i}_L}{\hat{d}} =\frac{8s^3+8.008\times10^4 s^2+1.2\times10^9 s+5.001\times10^{12}}{4\times10^{-6}s^4+8.04s^3+8.111\times10^4 s^2+1.205\times10^9 s+5.063\times10^{12}} \tag{14}$$

$$G_1(S)=\frac{\hat{i}_L}{\hat{d}}=\frac{3.594\times10^5 s^2+1.815\times10^7 s+4906}{0.2s^3+10.1s^2+2.5\times10^7 s} \tag{15}$$

$$G_2(S)=\frac{\hat{i}_L}{\hat{d}} =\frac{8\times10^4 s^3+8.08\times10^6 s^2+1\times10^{13} s+5.05\times10^{14}}{0.04s^4+8\times10^4 s^3+1.808\times10^7 s^2+1\times10^{13} s+1.13\times10^{15}} \tag{16}$$

H. Simulation Results

The simulation waveforms of the output voltages (V_{dc1}, V_{dc2}) and inductor current i_L are given in Fig. 12. As in the above analysis, the simulations are carried out in three different operation modes.

P-cell mode: When R_1 is bigger than R_2 (R_1 = 50MΩ, R_2= 5Ω), V_{dc1} will be higher than V_{dc2}. The P-cell leg switch S_1 works under the current control mode with a preset $i_{L\text{-}ref}$ of 50A and it generates an intermittent positive current i_L to transfer the redundant power from the upside to the downside. With a decrease of V_{dc1} and an increase of V_{dc2}, both V_{dc1} and V_{dc2} come back to allowable values during a burst mode switching period. Then, the voltage balancer stops working and the inductor current i_L disappears. Waveforms of the voltages and inductor current are shown in Fig. 12(a). To get a clear view of the voltages and current, Fig. 12(a) is partially enlarged, as shown in Fig. 13.

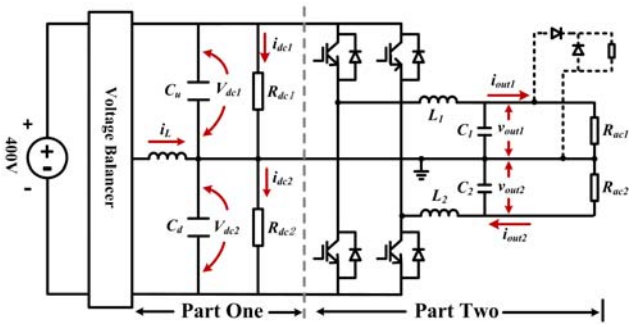


Fig. 14. The experiment system structure.

Natural-balance mode: When R_1 is equal to R_2 (R_1 = R_2 = 5Ω), V_{dc1} and V_{dc2} automatically tend to become balanced without control, and ultimately they are kept equal as in Fig. 12(b). Because V_{dc1} and V_{dc2} naturally keep between $V_{lower\text{-}allowed}$ and $V_{upper\text{-}allowed}$, the balancer does not work and the inductor current maintains a constant of zero in this case.

N-cell mode: When R_1 is smaller than R_2 (R_1 = 5Ω, R_2 = 50MΩ), V_{dc1} is lower than V_{dc2}. Thus, the curve of V_{dc1} has a downward trend when comparing with Fig. 12(a) and Fig. 12(b). Similarly, the N-cell leg switch S_2 works under the current control mode with a preset $i_{L\text{-}ref}$ of 50A and it generates a negative intermittent current i_L to transfer redundant power from the downside to the upside. With an increase of V_{dc1} and a decrease of V_{dc2}, both V_{dc1} and V_{dc2} come back to allowable values, and the voltage balancer stops working and the inductor current disappears. The waveforms of the voltages and current are shown in Fig. 12(c).

VI. Experimental Results

To demonstrate the viability of the proposed voltage balancer and the novel burst-mode control scheme, a 5-kW experiment system, shown in Fig. 14, was designed and tested. The whole system includes a 400V ac input, voltage balancer, dual-outputs full bridge inverter and loads which can be divided into dc loads and ac loads. Additionally, the ac loads include an ac resistive load and a half-bridge-rectifier ac load (such as a residential heater) which will lead to an unbalance between V_{dc1} and V_{dc2}. Thus, the experiment consists of two parts: the first part is a dc load test which is emulated by two pure resistors; and the second part is an ac load test including the balanced resistive load and unbalanced load of the half-bridge resistive heater. The simulation parameters are listed as follows: C_u = C_d = 10mF, L_1 = L_2 = 0.2mH, C_1 = C_2 = 40uF, R_{ac1} = R_{ac2} = 25Ω, and $i_{L\text{-}ref}$ = 30A. A directly coupled inductor is used in the voltage balancer to reduce its volume and weight, and L_{d1} = L_{d2} = 50uH, L_{com} =

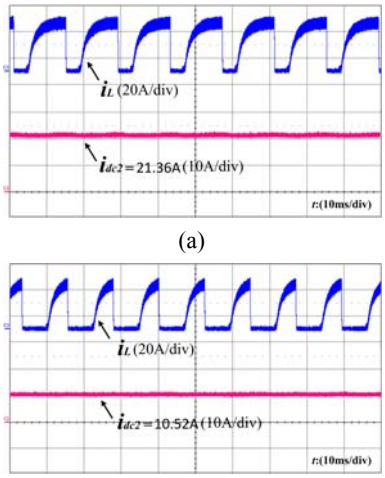


Fig. 15. The experimental waveforms of the inductor current and load current. (a) $R_{dc1} = \infty$, $R_{dc2} = 9\Omega$; (b) $R_{dc1} = \infty$, $R_{dc2} = 18\Omega$.

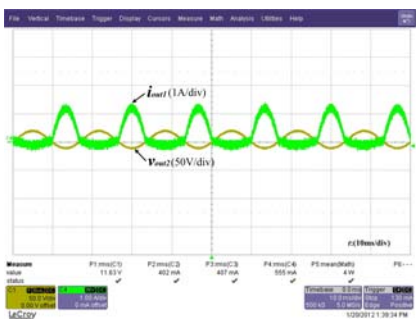


Fig. 16. The experimental waveforms without the voltage balancer when connected to unbalanced ac load.

150uH. The resistance of the half-bridge-rectifier load is 11Ω. R_{dc1} and R_{dc2} will be given according to the experimental requirements in the following.

I. Experimental Results Analysis of the dc Load

The first experiment is conducted with unbalanced dc loads so that $R_{dc1} = \infty$ and $R_{dc2} = 9\Omega$, 18Ω. The steady-state experimental waveforms of the inductor current i_L and load current i_{dc2}, which is the current through R_{dc2}, are shown in Fig. 15. As shown in Fig. 15, the switch duty cycle is reduced with the increase of R_{dc2}, and the duration of i_L becomes shorter. Even in this extreme condition, the novel burst-mode control scheme and voltage balancer work well to provide an appropriate voltage for R_{dc2}.

J. Experimental Results Analysis of the ac Load

The second experiment is conducted with unbalanced ac loads which are simulated by a half-bridge-rectifier load and a resistive load. For security reasons, a small V_{dc} is applied to observe the system performance when the voltage balancer is first disconnected. Fig. 16 shows the experimental waveforms of the ac voltage v_{out2} and the half-bridge-rectifier load current i_{out1}. It can be seen that the half-bridge-rectifier load leads to a serious asymmetric output ac voltage v_{out2} without

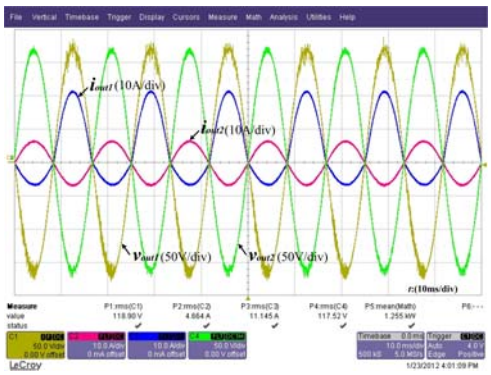


Fig. 17. The experimental waveforms of the voltage and current with the voltage balancer when connected the unbalanced ac load.

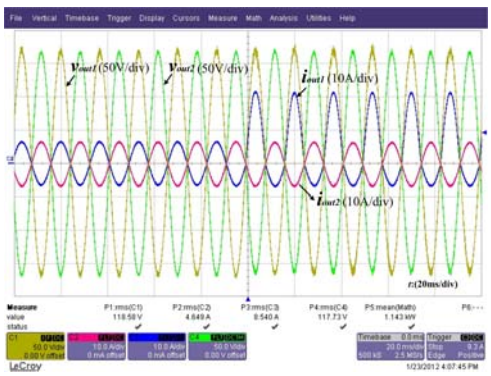


Fig. 18. The experimental transition waveforms of the ac voltage and current from balanced load to unbalanced load.

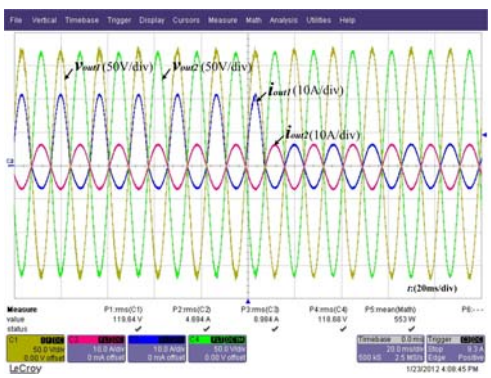


Fig. 19. The experimental transition waveforms of the ac voltage and current from unbalanced load to balanced load.

the balancer.

Fig. 17 shows the steady-state output ac voltages (v_{out1}, v_{out2}), and the half-bridge heater current i_{out1} when the voltage balancer is connected. It can be seen that the dual-output voltages have almost the same RMS values, v_{out1} = 118.90V and v_{out2} = 117.52V, though the current of the half-bridge heater is obviously unsymmetrical.

Fig. 18 and 19 show the experimental transition waveforms of the dual-output ac voltages, and the load currents between the balanced and unbalanced loads. No impact voltages or currents appear in the system with a smooth transition, and the output voltages are balanced and almost the same before

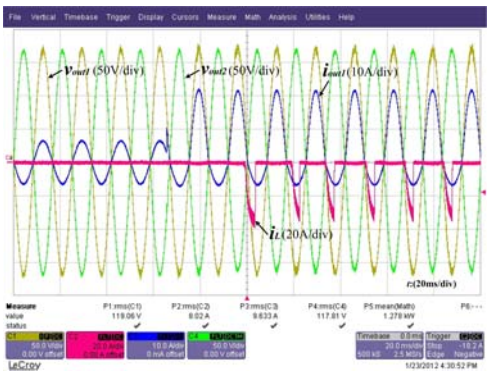


Fig. 20. The experimental waveforms of voltage and current with the voltage balancer from balanced load to unbalanced load.

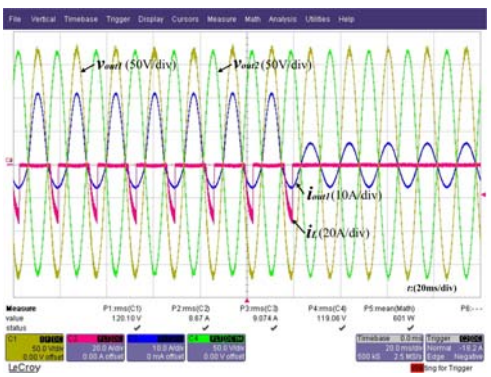


Fig. 21. The experimental waveforms with voltage balancer from unbalanced load to balanced load.

and after the loads change.

Fig. 20 and 21 show the experimental waveforms of the dual-outputs ac voltages (v_{out1}, v_{out2}), the inductor current i_L and the half-bridge heater current i_{out1}. The inductor current is zero when the ac loads are balanced. However, it becomes an intermittent negative current to balance the two voltages when the ac loads are unbalanced. Similarly, there are no impact voltages or currents in the system, and the output voltages are kept balanced before and after the loads change with a smooth transition.

According to the above experimental results, the output ac voltages (v_{out1}, v_{out2}) have almost the same values with the control of the voltage balancer, whether balanced loads or unbalanced loads are connected. Thus, the bidirectional dual buck-boost voltage balancer with the burst-mode control scheme is shown to be correct.

VII. CONCLUSION

In this paper, a bidirectional dual buck-boost voltage balancer and a burst-mode control scheme are proposed for low-voltage bipolar-type DC microgrids. The structure of the voltage balancer will enhance the system reliability thanks to the fact that it does not have any shoot-through problems. Under the proposed novel burst-mode control scheme, the balancer works and generates an intermittent inductor current with lower power losses to balance the two output DC voltages when the two voltages do not satisfy predetermined values. At last, simulation and experimental results have verified that the bidirectional dual buck-boost voltage balancer based on the burst-mode control scheme has a good ability to balance the output voltages with balanced or unbalanced DC/AC loads. Moreover, the system has a smooth transition with no impact voltages or currents when the loads change.

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