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An Improved Asymmetric Half-Bridge Converter for Switched Reluctance Motor in Low-Speed Operation with Current Regulated Mode

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Abstract

This study presents a novel method for reducing the switching losses of an asymmetric half-bridge converter for a three-phase, 12/8 switched reluctance motor operated in low speed. In particular, this study aims to reduce the switching-off losses of chopping switches in the converter when operated in the current regulated mode (chopping mode). The proposed method uses the mixed parallel operation of IGBT (chopping switch) and MOSFET (auxiliary switch). MOSFET is precisely controlled to momentarily conduct prior to the turn-off interval of the IGBT. Consequently, the voltage across the switches is clamped to approximately zero, substantially decreasing the turn-off switching losses. The analytical expressions of power losses are extensively elaborated. Compared with the conventional asymmetric half-bridge converter, the modified converter can effectively minimize the switching losses. Therefore, the efficiency of the converter is eventually improved. Computer simulation and experimental results confirm the effectiveness of the proposed technique.

Key words: Asymmetric half-bridge converter, Parallel IGBT/MOSFET, Switched reluctance motor, Switching loss

I. INTRODUCTION

Switched reluctance motors (SRMs) have simple and rigid structures compared with other conventional electrical machines. However, controlling SRMs is relatively complicated because their phase inductance and torque are functions of both rotor position and current [1]. Therefore, with the knowledge of angular positions, one should precisely control the phase currents of SRM drives with an efficient power electronic converter. High switching frequency is used to control the current of SRM with fast dynamic and accuracy. When the machine is operated below base speed, phase currents can be regulated. In this low-speed zone, the back electromotive force is lower than the DC-link voltage; hence, the current-chopping mode control can be utilized [2]. Nevertheless, the associated turn-off switching loss of the conventional hard-switched converter for SRM is a major problem in terms of efficiency.

Many scholars have attempted to reduce the switching losses. The proposed soft-switched converter for three-phase SRMs in [3] involves four switching devices, in which one is specifically assigned for the resonant part. A modified soft-switched circuit in [4] utilizes only three active switches, but requires additional bridge diodes and a resonant tank. Another modified converter employs several thyristors for the motor windings and the resonant circuit plus an extra coupled transformer [5]. The introduced soft-switched circuit in [6] has some relocation of its resonant part compared with that in [3]. Although high torque and improved efficiency are claimed to be achieved in [3] and [6], the voltage and current stresses of the switching devices could still be observed in these resonant-based converters. In addition, these techniques are considered more suitable for the high-speed single-pulse mode control than the low-speed current-chopping mode control.

An individual auxiliary resonant branch is paralleled to each load of a two-quadrant soft-switching converter [7]. The simulation results show that the snubber capacitors cause zero voltage switching (ZVS) during turn-off, and the resonant circuit incurs the close-to ZVS during turn-on. The latter part is unnecessary because the zero current switching (ZCS) during

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turn-on occurs naturally for inductive loads. A common auxiliary resonant circuit is used in a modified three-phase asymmetric half-bridge converter [8]. The MOSFET-based converter complicatedly utilizes two auxiliary switches (i.e., one for charging and another for discharging the resonant capacitor). ZVS during turn-on and ZCS during turn-off can be observed in the chopping switches. Nonetheless, the commutating switches in [7] and [8] have significant voltage stresses.

In [9], a simplified method for determining the optimum snubber capacitors for the chopping switches of a standard asymmetric half-bridge converter for three-phase SRMs is proposed. The snubber sizing in [10] is based on the fall time of the turning-off IGBT. In these previous studies, efficiency improvement is observed; yet, such technique has inherent current spike during turn-on. Furthermore, the turn-off losses of IGBT still proportionally increase with the switching frequency.

The methods for achieving soft-switched converters by the mixed parallel operation of IGBT and MOSFET pairs are explained in [11] to [18]. In these works, both devices are turned on simultaneously. However, at the end of conduction interval, the IGBT is turned off, whereas the MOSFET is still conducting. MOSFET is soon turned off after a short delay time [11]-[15]. Even though the switching loss of IGBT can be minimized, the conduction loss of MOSFET should be included. In [16], MOSFET is precisely controlled to momentarily conduct twice (i.e., the first time when the IGBT is turned on and the second time prior to the turn-off interval of the IGBT). Nevertheless, the control of hybrid switch is relatively complex and not convincing, especially when applied to inductive load (e.g., SRM). The turn-on ZCS naturally reduces the switching loss of IGBT; hence, the first MOSFET conduction is redundant. Contrarily, MOSFET in [17] is programmed to conduct only once (i.e., when the IGBT is turned off). However, the switching loss in this case is not optimally minimized because the commutation between IGBT and MOSFET is not a continuous transfer. In [18], the turn-on and turn-off time of MOSFET and IGBT are optimized, respectively, to minimize the overall losses of the hybrid switch. Extensive optimization is required when the duty cycle and/or switching frequency of the MOSFET/IGBT hybrid switch are changed. Further improving the hybrid IGBT/MOSFET power switch is difficult.

Considering the conditions cited in the preceding paragraphs, this study proposes an improved asymmetric half-bridge converter, which can efficiently operate SRM in low-speed zone with the current regulated mode. The rest of the paper is organized into five sections. Following the Introduction, Section II analyzes the operating principles of the standard asymmetric half-bridge converter. Section III presents the proposed converter based on the parallel operation of IGBT/MOSFET. Moreover, this section thoroughly explains

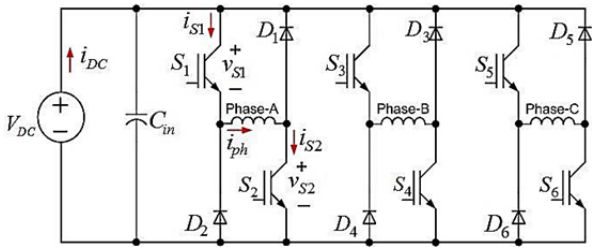
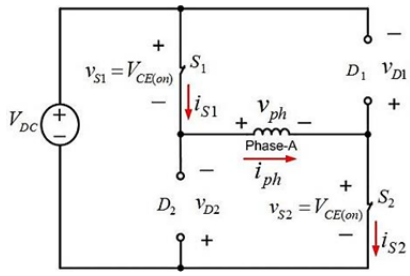
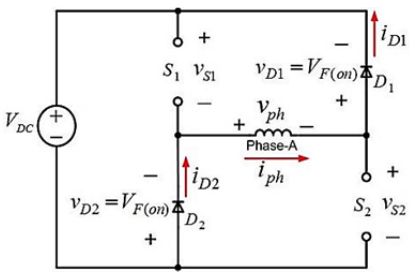


Fig. 1. Standard asymmetric half-bridge converter.



(a) Magnetization mode.



(b) Demagnetization mode.

Fig. 2. Conduction modes of the hard chopping scheme.

the topology of the hybrid switch and its control. The power losses are analyzed through the developed mathematical expressions. Sections IV and V discuss the computer simulation and experimental verification of the developed systems, respectively. These sections also compare the efficiency of the standard and proposed converters. Finally, Section VI provides the drawn conclusions.

II. THE STANDARD CONVERTER

A. Asymmetric Half-bridge Converter

Asymmetric half-bridge converter provides the most control flexibility and fault tolerance for SRM drives. Each phase of this standard converter consists of two controllable switches and two diodes as shown in Fig. 1. The converter uses the same DC-link voltage for magnetization and demagnetization through the switches and diodes, respectively. Phase current can be regulated with the magnetization and demagnetization mode of the hard chopping scheme.

Considering one phase of the three-phase asymmetric half-bridge converter (Fig. 1), the two operating modes of the hard chopping scheme are illustrated in Fig. 2. In the magnetization mode (Fig. 2(a)), the chopping switches S_1 and

S_2 are on, whereas the diodes D_1 and D_2 are off. In this case, the phase current increases. By contrast, in the demagnetization mode (Fig. 2(b)), the chopping switches S_1 and S_2 are off, whereas the diodes D_1 and D_2 are on. Correspondingly, the phase current in this case is decreased.

The voltages and currents of the phase winding and controllable switches in each conduction mode can be identified based on the mathematical expressions given below.

1) Magnetization mode: Considering Fig. 2(a), phase voltage can be expressed as

$$v_{ph} = V_{DC} - 2V_{CE(on)} \approx V_{DC} \tag{1}$$

The voltages across the chopping switches can be determined with the following formula:

$$v_{S1} = v_{S2} = V_{CE(on)} \approx 0 \tag{2}$$

The phase current is expressed as

$$i_{ph} \approx I_{ref} \tag{3}$$

The currents through the chopping switches can be determined as follows:

$$i_{S1} = i_{S2} \approx I_{ref} \tag{4}$$

2) Demagnetization mode: Considering Fig. 2(b), phase voltage can be depicted as

$$v_{ph} = -V_{DC} - 2V_{F(on)} \approx -V_{DC} \tag{5}$$

The voltages across the chopping switches can be determined as follows:

$$v_{S1} = v_{S2} = V_{DC} + V_{F(on)} \approx V_{DC} \tag{6}$$

The phase currents can be expressed as below.

$$i_{ph} = i_{D1} = i_{D2} \approx I_{ref} \tag{7}$$

The currents through the chopping switches can be identified with the below equation.

$$i_{S1} = i_{S2} \approx 0 \tag{8}$$

where V_{DC}, $V_{CE(on)}$, and $V_{F(on)}$ are the DC-link voltage, IGBT forward voltage, and diode forward voltage, respectively, and I_{ref}, i_{D1}, and i_{D2} are the reference current and the currents through diode D_1 and D_2, respectively.

In one period of the phase current pulse (T_P) of SRM, several switching periods (T_s) exist inside (Fig. 3). The waveforms of the phase current, phase voltage, chopping switch voltage, and chopping switch current corresponding to the hard chopping scheme are clearly illustrated in Fig. 3.

B. Analysis of Power Losses in the Standard Converter

As depicted in Fig. 3, the hard-chopped asymmetric half-bridge converter has two related frequencies (i.e., the current-pulse (magnetic) frequency (f_p) and the switching frequency (f_s)).

The phase current-pulse frequency or magnetic frequency induces eddy current and hysteresis. Such frequency solely affects the core losses and is directly proportional to rotor speed and the number of rotor teeth. This frequency can be obtained with the below formula.

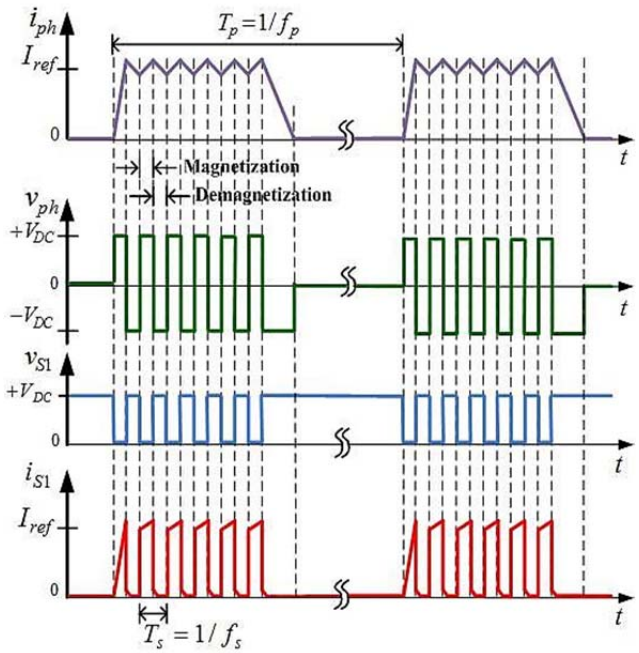


Fig. 3. Waveforms associated with the hard chopping scheme.

$$f_p = \frac{1}{T_p} = \frac{N_r n}{60} \tag{9}$$

where T_p, N_r , and n are the current-pulse period, the number of rotor poles, and the SRM speed (in rpm), respectively. This speed-dependent frequency does not significantly contribute to the converter losses.

The switching frequency refers to the frequency of the chopping switch current when the phase current is regulated with the pulse-width modulation (PWM) technique. The selected switching frequency is always constant (i.e., it does not change with rotor speed). The power losses of the switching devices in the converter only involve this frequency type. A high switching frequency results in a high switching loss. This frequency can be identified as follows:

$$f_s = \frac{1}{T_s} \tag{10}$$

where T_s denotes the switching period.

One switching period (T_s) in Fig. 3 is enlarged to analyze the power losses of the chopping switch (IGBT) in the standard converter. Fig. 4 illustrates the corresponding voltage and current waveforms of the chopping switch. I_{ref} is the average value of the chopping switch current i_{S1} during the on-state interval ($t_{on} \rightarrow t_f$).

Four consecutive intervals exist in one switching period. These intervals are presented below.

Interval 1 ($t_{on} \rightarrow t_f$): Once the gate drive signal is applied, the IGBT turns on and carries the reference current. Its voltage suddenly decreases to the level of IGBT's forward voltage.

Interval 2 ($t_f \rightarrow t_t$): During this fall time, the gate signal is removed; hence, the IGBT turns off. The current falls linearly from the initial level to A times of the reference current.

Contrarily, the IGBT voltage suddenly increases to the level of DC-link voltage along with the diode's forward voltage.

Interval 3 ($t_t \rightarrow t_x$): During this tail time, the IGBT voltage remains unchanged from the previous level. The IGBT current gradually decreases in a linear function to zero at t_x.

Interval 4 ($t_x \rightarrow t_{on}+T$): The IGBT is in a complete off-state, which lasts until the end of the switching period.

The corresponding instantaneous current of IGBT in one switching period can be expressed as

$$i_{S1}(t)=\begin{cases} I_{ref}, & t_{on} \le t \le t_f \\ I_{ref}\left[1-(1-A)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right], & t_f \le t \le t_t \\ AI_{ref}\left[1-\left(\dfrac{t-t_t}{t_x-t_t}\right)\right], & t_t \le t \le t_x \\ 0, & t_x \le t \le t_{on}+T_s \end{cases} \quad (11)$$

where A is the constant of the current transition (approximately 0.05).

The IGBT instantaneous voltage is given by the below formula.

$$v_{S1}(t)=\begin{cases} V_{CE(on)}, & t_{on} \le t < t_f \\ V_{DC}+V_{F(on)}, & t_f \le t < t_{on}+T_s \end{cases} \quad (12)$$

Consequently, the IGBT instantaneous power losses can be obtained with the following expression:

$$p_{S1}(t)=\begin{cases} V_{CE(on)}I_{ref}, & t_{on} \le t < t_f \\ \left[V_{DC}+V_{F(on)}\right]I_{ref}\left[1-(1-A)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right], & t_f \le t \le t_t \\ \left[V_{DC}+V_{F(on)}\right]AI_{ref}\left[1-\left(\dfrac{t-t_t}{t_x-t_t}\right)\right], & t_t \le t \le t_x \\ 0, & t_x \le t < t_{on}+T_s \end{cases} \quad (13)$$

The average power losses of IGBT can be calculated as

$$P_{S1}=\frac{1}{T_s}\int_{t_{on}}^{t_{on}+T_s} p_{S1}(t)dt \quad (14)$$

A major overlap between the voltage and current of IGBT during the turn-off interval (Fig. 4) induces significant switching losses. This event leads to poor converter efficiency. Thus, the practical techniques for mitigating such problem are extremely crucial.

III. The Proposed Converter

A. Modified Converter with Parallel IGBT/MOSFET

The proposed concept of modifying the standard converter is to parallel IGBT with MOSFET to form the IGBT/MOSFET pair (Fig. 5). MOSFET is controlled to momentarily conduct the current once IGBT is turned off. The fast switching MOSFET assists the IGBT to effectively commutate the phase current during the turn-off interval of the IGBT. When the MOSFET is in the on-state, the shared voltage across the IGBT and MOSFET is clamped to the forward drop level. The

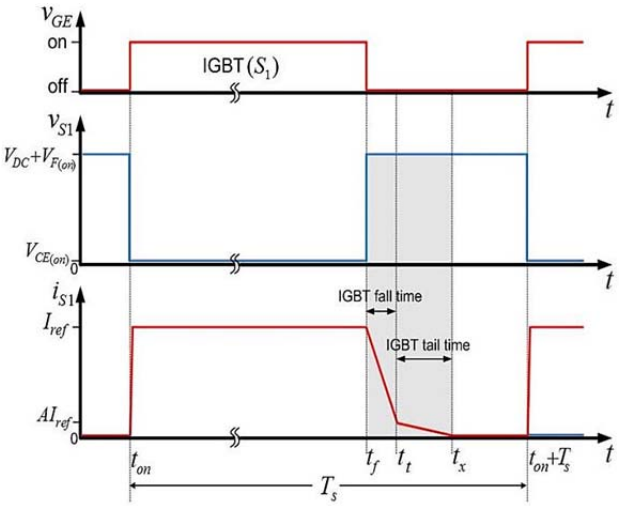


Fig. 4. Voltage and current switching waveforms of IGBT (S_1) in the standard converter.

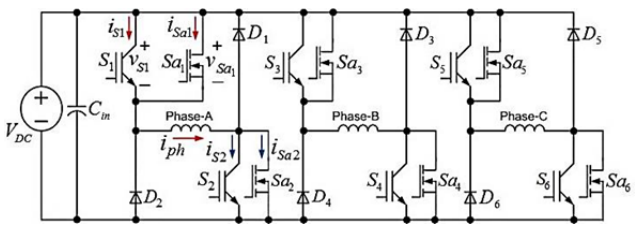


Fig. 5. Modified converter using a mixed parallel IGBT/MOSFET.

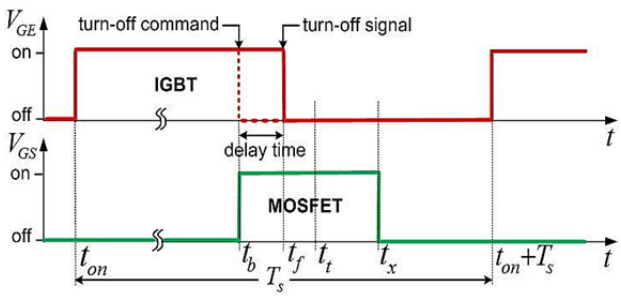


Fig. 6. Gate drive waveforms of the IGBT/MOSFET.

reduced voltage/current overlap of IGBT leads to a significant decreased switching-off loss.

The suitable gate drive signals of both IGBT and MOSFET should be generated to achieve the mixed parallel operation of their pair. MOSFET should be turned on before the IGBT is turned off with an optimal delay time. MOSFET is later turned off after the IGBT is turned off as shown in Fig. 6. To realize such gate drive waveforms, the IGBT and MOSFET of each phase are controlled according to the conditions described below.

1) IGBT gate drive: When the falling edge of the IGBT's turn-off command is detected, the falling-edge delay circuit will delay the actual turn-off signal with a predetermined delay time (Fig. 7). The algorithm does not affect the leading-edge turn-on signal of the IGBT.

2) MOSFET gate drive: Once the MOSFET gate signal generator detects the falling edge of the IGBT's turn-off

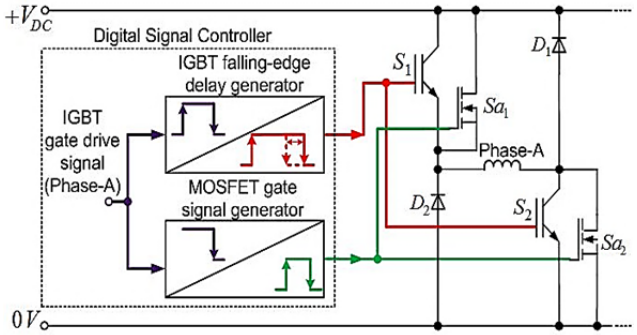


Fig. 7. Gate drive signal of the IGBT/MOSFET pairs of phase-A.

command, the corresponding MOSFET gate drive signal is immediately developed (Fig. 7). This signal lasts for the duration equal to the sum of delay time ($t_b \rightarrow t_f$), the IGBT's fall time ($t_f \rightarrow t_t$), and the IGBT's tail time ($t_t \rightarrow t_x$) (Fig. 6). Thus, the gate signals of IGBT and MOSFET overlap for the duration of delay time.

As illustrated in Fig. 7, the proposed algorithm can be easily implemented in the main digital signal controller without the need for any extra hardware. This software solution technique is effective and less complicated.

The proposed soft-switching method is applied whenever the phase current is chopped, and it functions independently of the rotor position and rotor speed. The algorithm is integrated into the current regulation with the PWM technique.

B. Analysis of Power Losses in the Proposed Converter

Given the switching characteristics of IGBT (S_1) and MOSFET (S_{a1}) in phase-A of the proposed converter in Fig. 5, the corresponding voltage and current waveforms are clearly shown in Fig. 8.

When the IGBTs carry current ($t_{on} \rightarrow t_x$), the phase current is equal to the sum of the corresponding IGBT/MOSFET pair's currents, which are equal to the reference current expressed as

$$i_{ph} = i_{S1} + i_{Sa1} = i_{S2} + i_{Sa2} = I_{ref} \tag{15}$$

Therefore, the relationships of the current transition constants (i.e., *A*, *B*, *C*, and *D* illustrated in Fig. 8) can be written as follows:

$$A + B = 1 \tag{16}$$

$$C + D = 1 \tag{17}$$

where *A* and *B* are the current transition constants of the IGBT/MOSFET pairs at the beginning of IGBT's tail time ($t_t \rightarrow t_x$), and *C* and *D* are the current transition constants of the IGBT/MOSFET pairs during the overlap time ($t_b \rightarrow t_f$).

Table I summarizes the values of the current transition constants used in this study.

In the proposed technique, seven intervals exist in one switching period of each IGBT/MOSFET pair (Fig. 8). These intervals are explained in the succeeding paragraphs.

Interval 1 ($t_{on} \rightarrow t_b$): The IGBT gate drive signal is applied; hence, the main switch conducts the reference current. Its voltage is at the level of IGBT's forward drop.

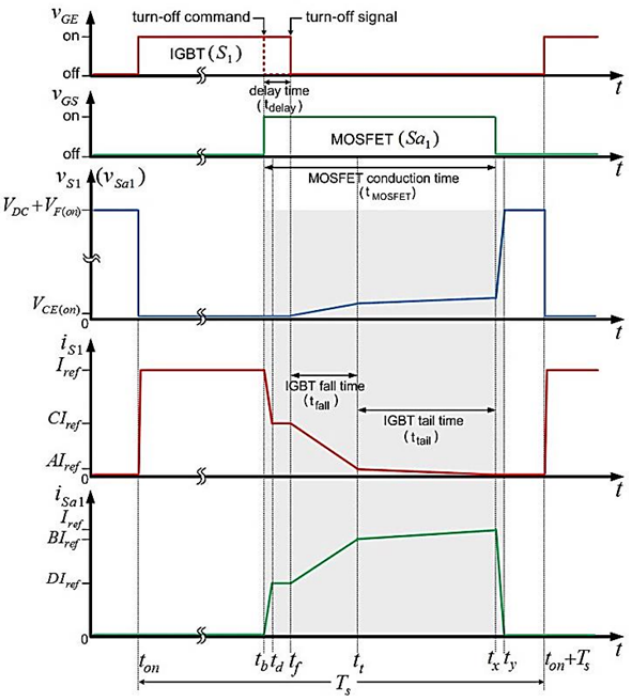


Fig. 8. Voltage and current switching waveforms of IGBT (S_1) and MOSFET (S_{a1}) in the proposed converter.

Interval 2 ($t_b \rightarrow t_d$): The MOSFET gate drive is activated, whereas the IGBT turn-off signal is delayed. Therefore, the current of the former switch increases linearly, whereas that of the latter switch decreases linearly. The voltage across the IGBT/MOSFET pair remains at the IGBT's forward voltage.

Interval 3 ($t_d \rightarrow t_f$): IGBT and MOSFET share the phase current proportionally. The currents of IGBT and MOSFET are at the level of *C* and *D* times of the reference current, respectively. The voltage of the IGBT/MOSFET pair is still at the level of IGBT's forward drop.

Interval 4 ($t_f \rightarrow t_t$): The actual IGBT turn-off signal is applied; thus, the current of IGBT is reduced linearly. By contrast, the current of MOSFET grows in a linear function. At the end of this interval, the currents of IGBT and MOSFET reach *A* and *B* times of the reference current, respectively. The voltage of the switch pair is influenced by MOSFET's on-state drain to source resistance, resulting in a linearly increased voltage.

Interval 5 ($t_t \rightarrow t_x$): During this IGBT's tail time, the IGBT current gradually decreases in a linear function to zero at the end of this interval. At the same time, the current of MOSFET progressively increases to the level of the reference current. The voltage across the IGBT/MOSFET pair is governed by the voltage model of MOSFET.

Interval 6 ($t_x \rightarrow t_y$): The MOSFET gate drive is removed; hence, the MOSFET quickly turns off. The switch pair voltage rapidly increases to the level of DC-link voltage along with the diode's forward voltage.

TABLE I
CURRENT TRANSITION CONSTANTS OF IGBT/MOSFET

Constant	Value
A	0.05 (Typical)
B	0.95 (Typical)
C	0.50 (Optimal)
D	0.50 (Optimal)

Interval 7 ($t_y \rightarrow t_o+T$): Both switches are in the complete off-state, which lasts until the end of the switching period.

The corresponding instantaneous current of IGBT in one switching period is expressed as

$$i_{S1}(t)=\begin{cases} I_{ref}, & t_{on}\le t\le t_b \\ I_{ref}\left[1-(1-C)\left(\dfrac{t-t_b}{t_d-t_b}\right)\right], & t_b\le t\le t_d \\ CI_{ref}, & t_d\le t\le t_f \\ I_{ref}\left[C+(A-C)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right], & t_f\le t\le t_t \\ AI_{ref}\left[1-\left(\dfrac{t-t_t}{t_x-t_t}\right)\right], & t_t\le t\le t_x \\ 0, & t_x\le t\le t_y \\ 0, & t_y\le t\le t_{on}+T_s \end{cases} \quad (18)$$

and the associated instantaneous current of MOSFET is denoted as

$$i_{Sa1}(t)=\begin{cases} 0, & t_{on}\le t\le t_b \\ DI_{ref}\left(\dfrac{t-t_b}{t_d-t_b}\right), & t_b\le t\le t_d \\ DI_{ref}, & t_d\le t\le t_f \\ I_{ref}\left[D+(B-D)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right], & t_f\le t\le t_t \\ I_{ref}\left[B+(1-B)\left(\dfrac{t-t_t}{t_x-t_t}\right)\right], & t_t\le t\le t_x \\ I_{ref}\left[1-\left(\dfrac{t-t_x}{t_y-t_x}\right)\right], & t_x\le t\le t_y \\ 0, & t_y\le t\le t_{on}+T_s \end{cases} \quad (19)$$

Correspondingly, the instantaneous voltage across the IGBT/MOSFET pair can be given by the below formula.

$$v_{S1}(t)=\begin{cases} V_{CE(on)}, & t_{on}\le t\le t_b \\ V_{CE(on)}, & t_b\le t\le t_d \\ V_{CE(on)}=DI_{ref}R_{DS(on)}, & t_d\le t\le t_f \\ I_{ref}\left[D+(B-D)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right]R_{DS(on)}, & t_f\le t\le t_t \\ I_{ref}\left[B+(1-B)\left(\dfrac{t-t_t}{t_x-t_t}\right)\right]R_{DS(on)}, & t_t\le t\le t_x \\ I_{ref}\left[1-\left(\dfrac{t-t_x}{t_y-t_x}\right)\right]R_{DS(on)}, & t_x\le t\le t_y \\ V_{DC}+V_{F(on)}, & t_y\le t<t_{on}+T_s \end{cases} \quad (20)$$

The instantaneous power loss of IGBT in one switching period can be obtained with the following equation:

$$p_{S1}(t)=\begin{cases} V_{CE(on)}I_{ref}, & t_{on}\le t\le t_b \\ DI_{ref}^2R_{DS(on)}\left[1-(1-C)\left(\dfrac{t-t_b}{t_d-t_b}\right)\right]\left(\dfrac{t-t_b}{t_d-t_b}\right), & t_b\le t\le t_d \\ CDI_{ref}^2R_{DS(on)}, & t_d\le t\le t_f \\ \left\{\begin{array}{l} I_{ref}^2R_{DS(on)}\left[C+(A-C)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right] \\ \left[D+(B-D)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right] \end{array}\right\}, & t_f\le t\le t_t \\ AI_{ref}^2R_{DS(on)}\left[1-\left(\dfrac{t-t_t}{t_x-t_t}\right)\right]\left[B+(1-B)\left(\dfrac{t-t_t}{t_x-t_t}\right)\right], & t_t\le t\le t_x \\ 0, & t_x\le t\le t_y \\ 0, & t_y\le t<t_{on}+T_s \end{cases} \quad (21)$$

Moreover, the instantaneous power loss of MOSFET can be acquired as follows:

$$p_{Sa1}(t)=\begin{cases} 0, & t_{on}\le t\le t_b \\ \left[DI_{ref}\left(\dfrac{t-t_b}{t_d-t_b}\right)\right]^2R_{DS(on)}, & t_b\le t\le t_d \\ \left[DI_{ref}\right]^2R_{DS(on)}, & t_d\le t\le t_f \\ \left[I_{ref}\left(D+(B-D)\left(\dfrac{t-t_f}{t_t-t_f}\right)\right)\right]^2R_{DS(on)}, & t_f\le t\le t_t \\ \left[I_{ref}\left(B+(1-B)\left(\dfrac{t-t_t}{t_x-t_t}\right)\right)\right]^2R_{DS(on)}, & t_t\le t\le t_x \\ \left[I_{ref}\left(1-\left(\dfrac{t-t_x}{t_y-t_x}\right)\right)\right]^2R_{DS(on)}, & t_x\le t\le t_y \\ 0, & t_y\le t<t_{on}+T_s \end{cases} \quad (22)$$

Therefore, the average power loss of the IGBT/MOSFET pair can be calculated as

$$P_{S1+Sa1}=\frac{1}{T_s}\int_{t_{on}}^{t_{on}+T_s}\left(p_{S1}(t)+p_{Sa1}(t)\right)dt \quad (23)$$

With the help of MOSFET, the switching loss of each IGBT during turn-off can be reduced substantially. Therefore, the total loss of the modified soft-switched converter is significantly less than that of the standard hard-switched asymmetric half-bridge converter. The efficiency of the proposed converter is correspondingly improved.

The current transition constants *C* and *D* should be selected appropriately to optimally operate the IGBT/MOSFET pair. Using a high value of *D* can lead to a large current sharing in MOSFET. Contrarily, when a low value of *D* is employed, it results in a small current sharing in MOSFET. These conditions affect the current sharing of IGBT as shown in Fig. 8 (Interval 3: $t_d \rightarrow t_f$). Using small *D* in the operation cannot effectively decrease the switching loss of IGBT. Nevertheless, if a large *D* is used, then the MOSFET will experience a large conduction loss accordingly. In addition, an expensive MOSFET with an increased current rating is required.

Therefore, 0.5 is a compromised value for D, which is claimed optimal.

During Interval 3 ($t_d \rightarrow t_f$), the voltage across the IGBT/MOSFET pair (v_{S1}) is the IGBT forward voltage, while the MOSFET current is D times of the reference current. Consequently, the corresponding static drain-to-source resistance of MOSFET ($R_{DS(on)}$) can be calculated as follows:

$$R_{DS(on)} = \frac{v_{S1}}{i_{Sa1}} = \frac{V_{CE(on)}}{DI_{ref}},\ t_d \le t \le t_f \qquad (24)$$

The IGBT selected for the proposed converter has its specific data summarized in the left column of Table II. The typical forward drop voltage of IGBT is 1.6 V. When $D = 0.5$ and $I_{ref} =$ 5 A are adopted in Equ. (24), the corresponding $R_{DS(on)}$ is determined as $0.64\ \Omega$. The appropriate MOSFET can be specified as shown in the right column of Table II.

Compared with the standard three-phase asymmetric half-bridge converter, the new converter requires six extra MOSFET switches. Although the component count in the proposed converter is increased, the added cost can be considered less significant because the semiconductor devices nowadays are inexpensive. In this technique, the current rating of MOSFET can be lower than that of IGBT that may result in economical specification. Moreover, a good printed circuit board design can help manage the increased size of the proposed converter at an acceptable level.

C. Optimal Timing of the IGBT/MOSFET Gate Drive

Gate drive timing can be determined according to the switching characteristics of IGBT and MOSFET (Table II) as well as to the proposed switching waveforms (Fig. 8). The IGBT turn-off delay time (t_{delay}) should be at least equal to the MOSFET rise time (50 ns). However, MOSFET should be fully conducted before the IGBT is turned off. Therefore, the appropriate IGBT turn-off delay time can be obtained by summing up the MOSFET rise time (Interval 2:$t_b \rightarrow t_d$) and the additional delay (Interval 3: $t_d \rightarrow t_f$) as denoted in Fig. 8. The optimal t_{delay} is two times of the MOSFET rise time (i.e., 100 ns).

The optimal MOSFET conduction time (t_{MOSFET}) is the sum of the IGBT turn-off delay time t_{delay} ($t_b \rightarrow t_f$), the IGBT fall time t_{fall} ($t_f \rightarrow t_t$), and the IGBT tail time t_{tail} ($t_t \rightarrow t_x$) as presented below.

$$t_{MOSFET} = t_{delay} + t_{fall} + t_{tail} \qquad (25)$$

Applying the corresponding data in Table II to Equ. (25) yields an optimal MOSFET conduction time of 800 ns.

TABLE II
SPECIFICATION OF THE IGBT AND MOSFET USED

IGBT (GT60M303)	Value	MOSFET (FDPF10N60NZ)	Value
$V_{CE(\max)}$	900 V	$V_{DS(\max)}$	600 V
$I_{C(\max)}$	60 A	$I_{D(\max)}$	10 A
$V_{CE(on)}$ @5A (I_C)	1.6 V	$R_{DS(on)}$ @ 5A (I_D)	0.64 Ω
V_{GE}	±25 V	V_{GS}	±25 V
Fall Time	250 ns	Rise Time	50 ns
Fall Time	450 ns	Fall Time	50 ns

IV. SIMULATION RESULTS

A. Dynamic Model of the System

The dynamic model of the system is developed in a MATLAB/Simulink environment (Fig. 9). Specific data of a three-phase 12/8 SRM, as presented in the Appendix, are used to develop the simulation model of the machine. The measured flux linkage and static torque look-up tables are the essential parts of the SRM dynamic model. Once phase voltages and load torque are applied to the SRM model, the corresponding phase currents, electromagnetic torque, and rotor speed can be obtained. Fig. 9 demonstrates the closed-loop control of the phase currents using PI controllers. Rotor speed can be changed by properly adjusting the load torque.

Models of the standard and modified asymmetric half-bridge converters are implemented based on the techniques described in Sections II and III, respectively. The converter receives the gate drive signals from PWM generator blocks, and it has a DC-link voltage of 200 V. The hard chopping scheme is used with a selective fixed switching frequency ranging from 5 kHz to 25 kHz. The output of the converter is eventually connected to the SR machine block as presented in Fig. 9.

When the model of the standard converter is used in the system, the waveforms of the voltage, current, and associated power loss of IGBT during the turn-off interval can be simulated as depicted in Fig. 10. A large overlap between the switch voltage and switch current is clearly presented. Thus, this hard switching results in a significant switching loss in the standard asymmetric half-bridge converter.

When the model of the modified asymmetric half-bridge converter is employed, each IGBT in the converter is paralleled with a MOSFET to reduce the switching losses of the main switches. The gate drive voltage signals of the IGBT/MOSFET pair are tightly synchronized. Every single time the IGBT turn-off signal is commanded, 800 ns v_{GS} of MOSFET is fired. As explained in Section III, the v_{GS} of MOSFET always overlaps with the v_{GE} of IGBT for 100 ns. Fig. 11 illustrates that the generated MOSFET gate drive can accurately track the falling edges of the IGBT's gate drive even when the switching frequency and duty cycle are changed.

With the same simulation condition used in the standard converter, the proposed converter presents soft-switching characteristics of IGBT that closely correspond to the theoretical analysis (Fig. 12). Unlike the previous case, the overlap between the voltage and current of IGBT in the modified converter is considerably decreased. As such, the switching loss of IGBT can be successfully reduced, and the additional MOSFET loss can be considered insignificant. The

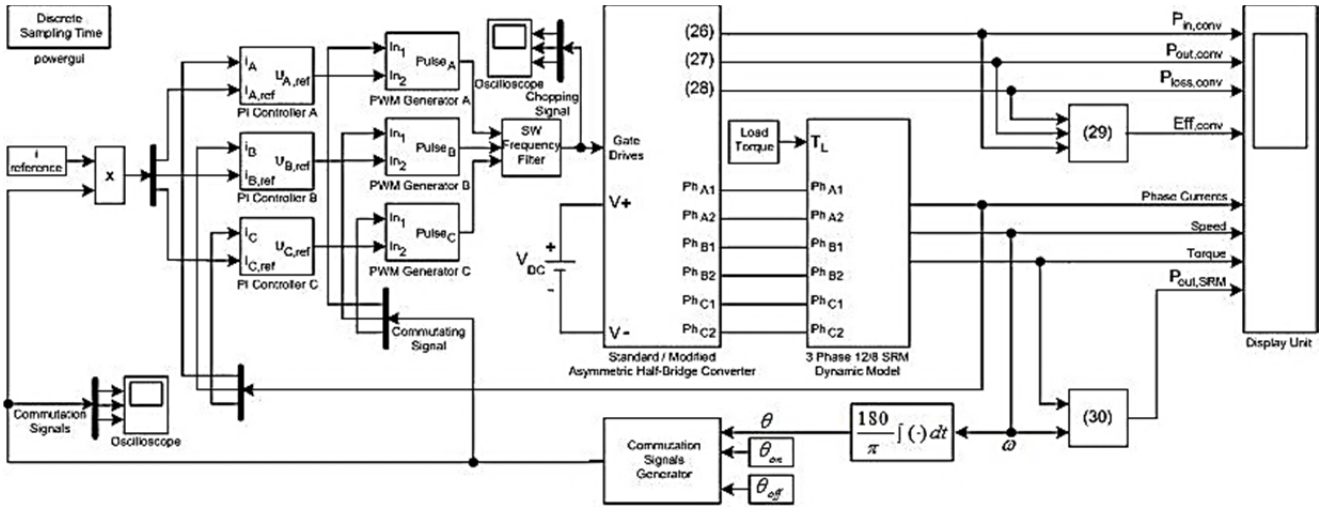


Fig. 9. Simulated system using the developed MATLAB/Simulink model.

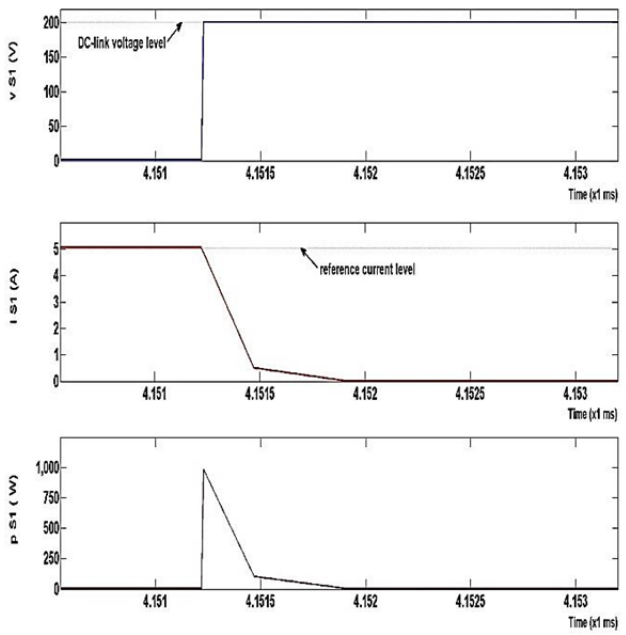


Fig. 10. Simulated waveforms of voltage, current, and power loss during the turn-off of IGBT (S_1) in the standard converter.

total losses are eventually reduced, thereby improving the efficiency of the converter.

B. Simulated Converter Losses and Efficiency

The efficiency of the standard and modified converters is verified by determining their input power, output power, and power losses using the mathematical equations presented in the succeeding paragraphs. These expressions are also used in the dynamic model shown in Fig. 9.

The average input power of the converter can be expressed as

$$P_{in,conv} = \frac{1}{T}\int_0^T (V_{DC} \cdot i_{DC})dt = P_{out,conv} + P_{loss,conv} \quad (26)$$

where T is the work period, V_{DC} is the DC-link voltage, and

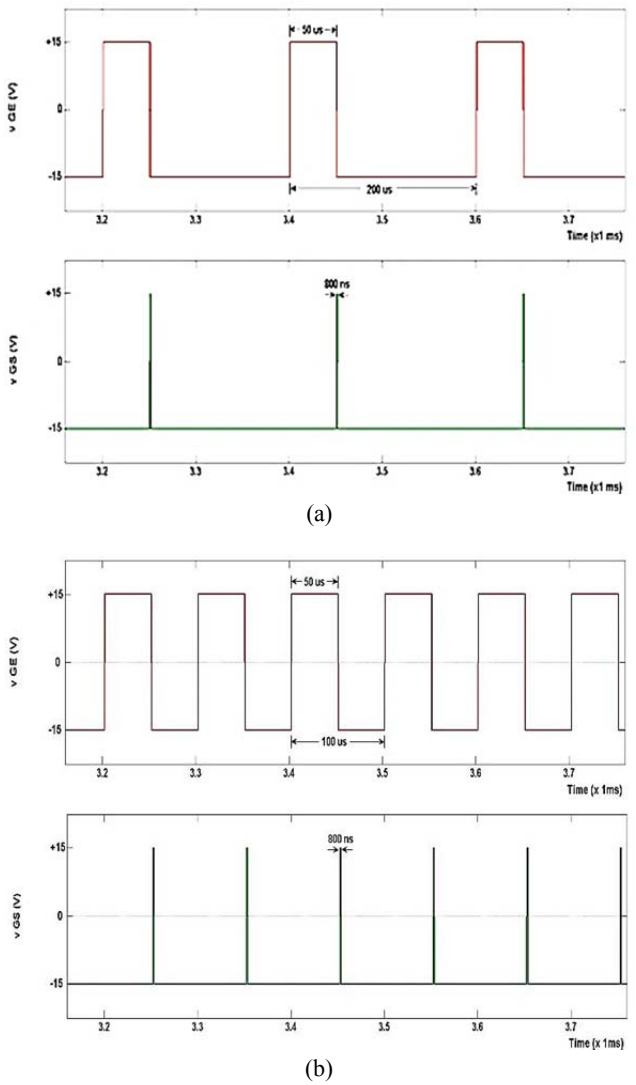


Fig. 11. Simulated waveforms of the gate drive voltages of IGBT (v_{GE}) and MOSFET (v_{GS}) in the proposed converter. (a) Duty cycle of 25% at the switching frequency of 5 kHz. (b) Duty cycle of 50% at the switching frequency of 10 kHz.

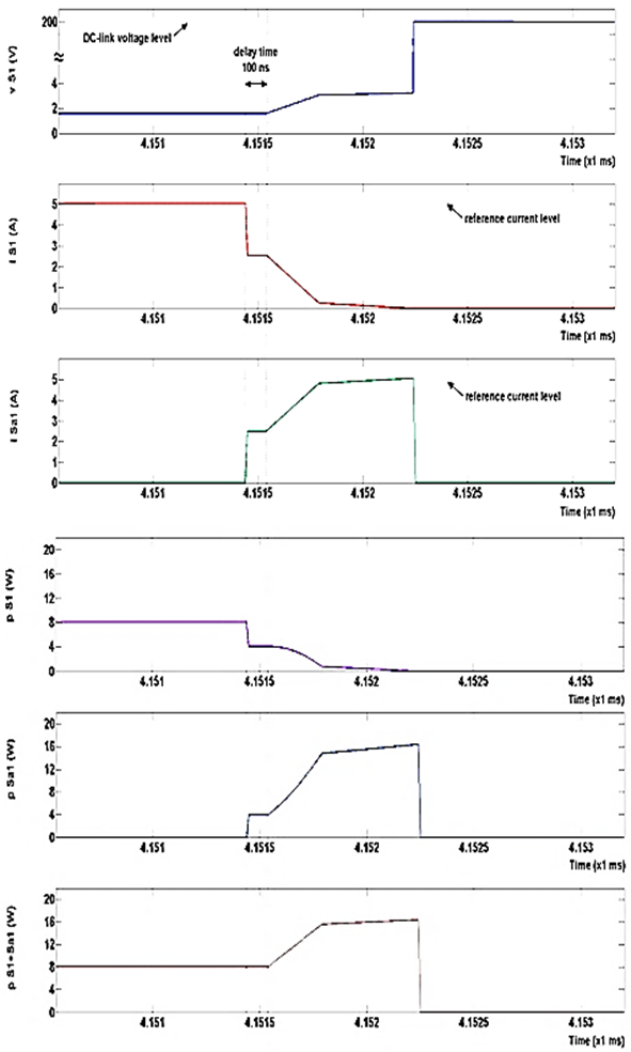


Fig. 12. Simulated waveforms of the voltage, current, and power losses of IGBT (S_1) and MOSFET (S_{a1}) in the proposed converter

i_{DC} is the current from DC-link.

The average output power of the three-phase converter can be obtained with the below equation.

$$P_{out,conv} = \frac{1}{T}\int_0^T (v_{phA}\cdot i_{phA} + v_{phB}\cdot i_{phB} + v_{phC}\cdot i_{phC})dt \quad (27)$$

where v_{phA}, v_{phB}, and v_{phC} are the voltages of phases-A, -B, and -C, respectively, and i_{phA}, i_{phB}, and i_{phC} are the currents of phases-A, -B, and -C, respectively.

The average power loss of the modified converter can be determined as follows:

$$P_{loss,conv} = \frac{1}{T}\int_0^T \left(\sum_{n=1}^{n=6} p_{IGBT,n} + \sum_{n=1}^{n=6} p_{MOSFET,n} + \sum_{n=1}^{n=6} p_{Diode,n}\right)dt \quad (28)$$

where p_{IGBT}, p_{MOSFET}, and p_{Diode} are the instantaneous power losses of IGBT, MOSFET, and diode, respectively.

The power losses of the standard converter can also be identified with (28), but the second term should be ignored.

Using the previous simulation condition, the total losses of the standard and modified converters at two different switching frequencies (i.e., 5 and 25 kHz) are determined and summarized in Table III. The total losses of the proposed converter are lower than those of the standard converter. The switching loss is reduced with the modified converter by 1.1 and 5.3 W for the switching frequencies of 5 and 25 kHz, respectively. While the total losses of the standard converter increase with the increased switching frequency, the total losses of the proposed asymmetric half-bridge converter remain virtually unchanged. In other words, the soft-switching technique of the modified converter is relatively effective for the different switching frequencies used. Both converters have unavoidable conduction loss, which depends on the voltage drop and current of the device. Such loss cannot be removed by the proposed technique.

TABLE III
CONVERTER LOSSES FROM SIMULATION

Converter Type	Converter Losses (W) @ I_{ref} = 5 A and Speed = 200 rpm	
	f_s = 5 kHz	f_s = 25 kHz
Standard	15.40	19.90
Proposed	14.30	14.60

Once the average input power, average output power, and average power loss of the converter are available, the converter efficiency can be achieved as

$$\%\,\eta_{conv} = \left(\frac{P_{out,conv}}{P_{int,conv}}\right)\times 100 = \left(\frac{P_{out,conv}}{P_{out,conv}+P_{loss,conv}}\right)\times 100 \quad (29)$$

The output power of the converter becomes the input power of the SRM. Thus, the average output power of SRM is equal to its load power and can be identified with the below equation.

$$P_{out,SRM} = \frac{1}{T}\int_0^T (T_e\cdot\omega)dt = P_{load,SRM} \quad (30)$$

where T_e is the electromagnetic torque.

In this simulation work, (26) to (30) can be verified using the MATLAB/Simulink model in Fig. 9. The standard and modified asymmetric half-bridge converters are first tested with a switching frequency of 25 kHz. Three different SRM rotor speeds (i.e., 200, 400, and 600 rpm) are investigated.

The power losses of the converters at different rotor speeds are compared in Fig. 13. The modified converter has low loss for all rotor speeds and results in a large converter efficiency. Fig. 14 indicates that the efficiency of both converters increases with the increasing rotor speed. The reason behind this condition is the fact that when SRM speed increases, the waveform of the phase current changes from a chopped wave into a single-pulse (less-chopped) wave, which has an inherently low switching loss.

As demonstrated in Fig. 14, the efficiency of the proposed converter at 200 rpm is 3.5% higher than that of the standard converter. The efficiency improvement is 2.4% and 1.82% at

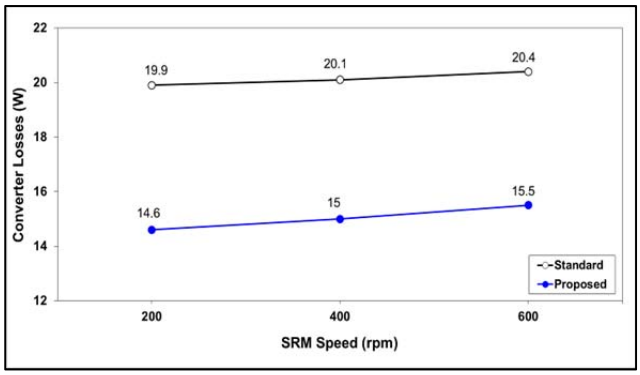


Fig. 13.Converter losses versus SRM speed from simulation at the switching frequency of 25 kHz.

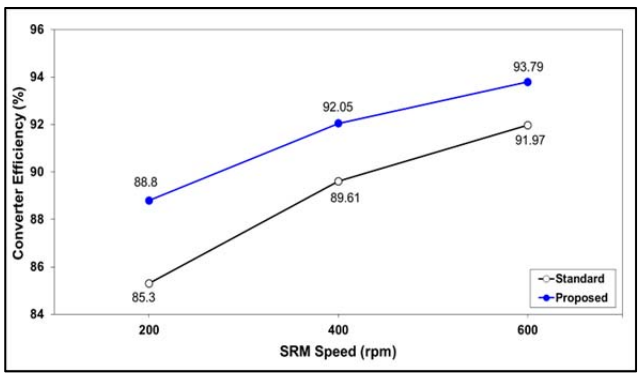


Fig. 14. Converter efficiency versus SRM speed from simulation at the switching frequency of 25 kHz.

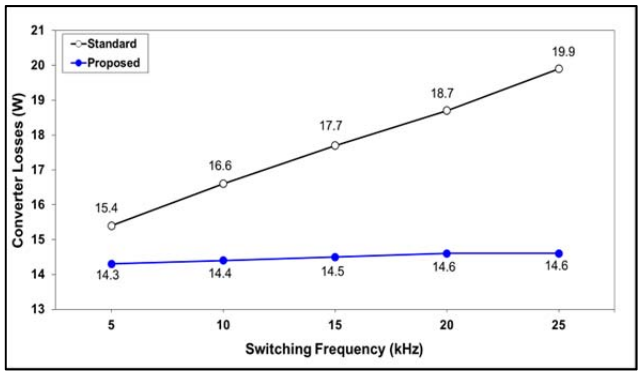


Fig. 15. Converter losses versus switching frequency from simulation at the SRM speed of 200 rpm.

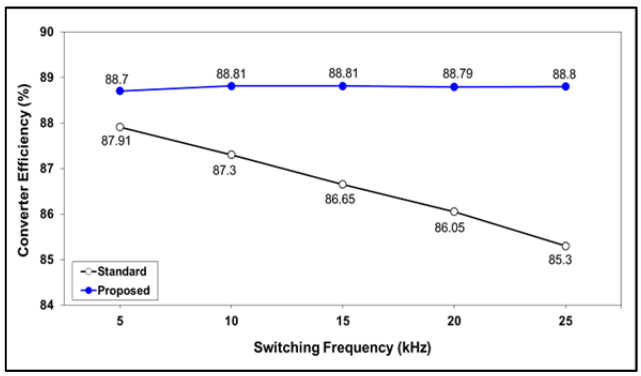


Fig. 16. Converter efficiency versus switching frequency from simulations at the SRM speed of 200 rpm.

400 and 600 rpm, respectively. Therefore, the modified converter is significantly effective, particularly at a low rotor speed.

In the second case, the SRM is investigated at the rotor speed of 200 rpm. Both converters are verified by varying the switching frequency from 5 kHz to 25 kHz. The power losses of the converters at different switching frequencies are compared in Fig. 15. When the switching frequency increases, the power loss of the standard converter increases linearly, whereas that of the proposed converter remains constant. The switching loss of the standard converter is proportional to the switching frequency used. By contrast, the switching loss of the modified converter is restricted by the proposed soft-switching technique. This method is exceedingly effective and completely independent of the switching frequency used.

Therefore, the efficiency of the modified converter remains constantly high at around 88.8% for all the tested switching frequencies (Fig. 16). However, the efficiency of the standard converter progressively decreases with the increasing switching frequency. The proposed asymmetric half-bridge converter is suitable to operate with a high switching frequency without the problem of excessive power losses.

V. Experimental Results

The microcontroller-based real-time control is implemented to verify the validity of the computer simulation. Fig. 17 illustrates the experimental hardware for this work. The three-phase converter with a DC-link voltage of 200 V is designed to function as both the standard and modified asymmetric half-bridge converters. The converter type is manually selected by operating the six mechanical switches either to parallel the MOSFETs to the corresponding IGBTs (modified converter) or to disconnect them out (standard converter). The tested 0.5-hp, three-phase, 12/8 SRM is continuously loaded with a DC generator within a certain range of rotor speed (i.e., 200 rpm to 600 rpm). Hence, the reference phase current of the SRM is set as 5 A. The data from the rotor position sensor (slotted disc and opto-interrupter) and hall-effect current sensors are read as control system inputs. The suitable PWM and gate drive signals for IGBT and MOSFET are generated when the signals are processed in the PIC24HJ128GP306 microcontroller. The switching frequency of the converters is selected between 5 and 25 kHz. Differential probe and hall-effect sensors are used to monitor and record the voltage and currents of each IGBT/MOSFET pair into the digital storage oscilloscope (DSO) for further analysis.

The standard three-phase asymmetric half-bridge converter is first selected to drive the loaded SRM at 200 rpm. The reference phase current of 5 A is selected, and 5 kHz is the

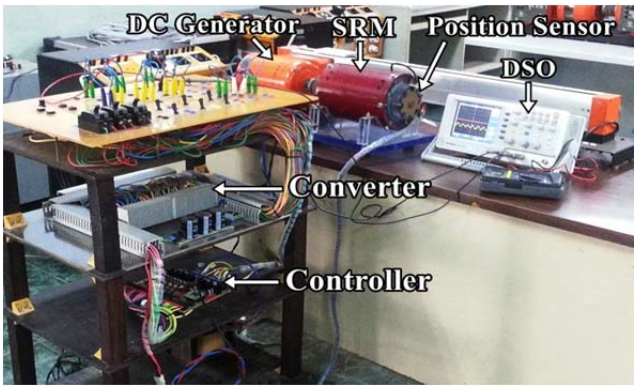


Fig. 17. Experimental hardware.

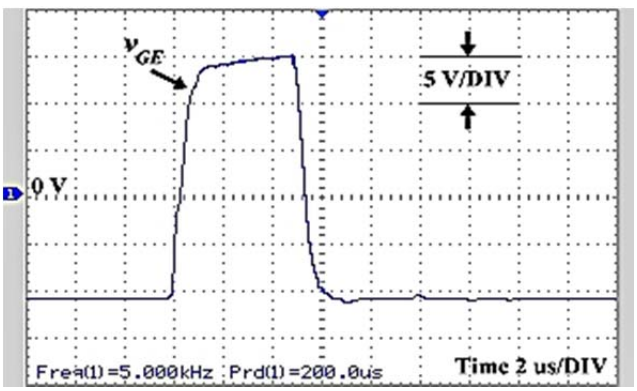


Fig. 18. Gate drive voltage of IGBT (v_{GE}) in the standard converter.

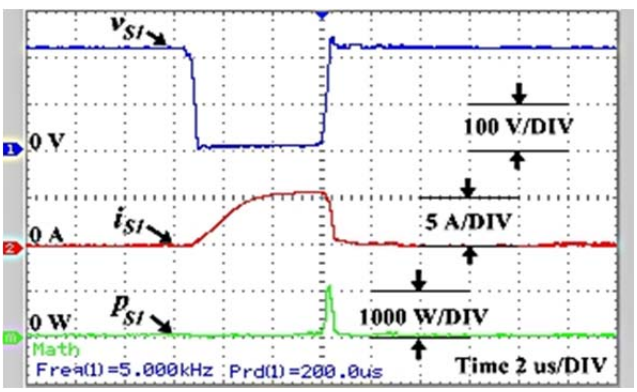


Fig. 19. Voltage (v_{S1}), current (i_{S1}), and power loss of IGBT (p_{S1}) in the standard converter.

switching frequency used. Fig. 18 shows the IGBT gate drive voltage (v_{GE}) of the standard converter, and Fig. 19 depicts the corresponding IGBT voltage (v_{S1}), IGBT current (i_{S1}), and IGBT power loss (p_{S1}). The hard switching characteristics during turn-off are clearly presented. The peak power of almost 1000 W due to the major overlap between voltage and current leads to a significant switching loss. The area under the power loss curve of IGBT is calculated as 480 µJ. When the switching period is 200 µs, the per-IGBT switching loss is determined as 2.4 W.

The standard converter is then replaced with the modified asymmetric half-bridge converter. The same experimental

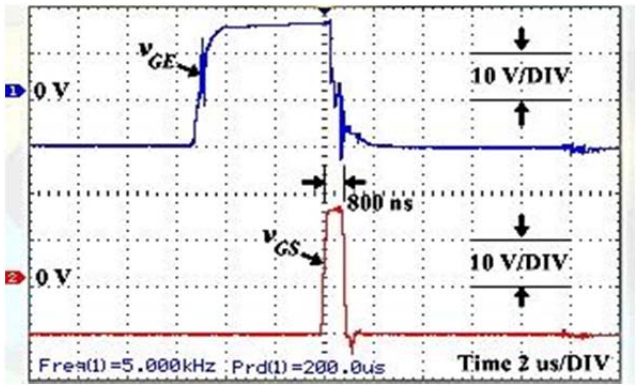


Fig. 20. Gate drive voltages of IGBT (v_{GE}) and MOSFET (v_{GS}) in the proposed converter.

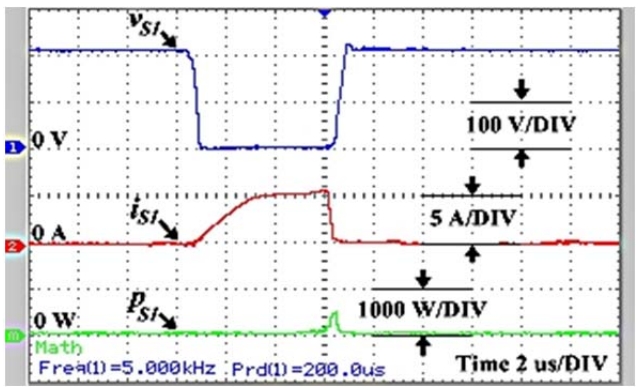


Fig. 21. Voltage (v_{S1}), current (i_{S1}), and power loss of IGBT (p_{S1}) in the proposed converter.

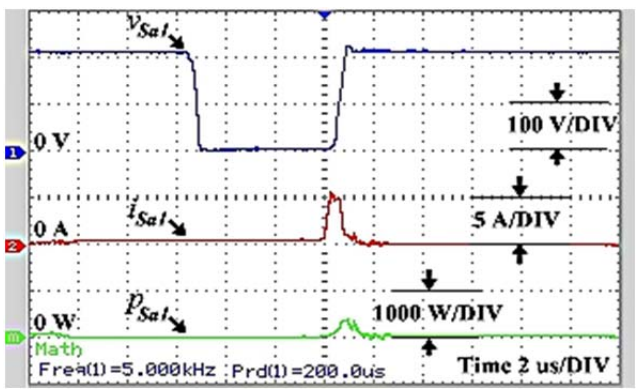


Fig. 22. Voltage (v_{Sa1}), current (i_{Sa1}), and power loss of MOSFET (p_{Sa1}) in the proposed converter

conditions are used in this second test. Fig. 20 demonstrates the gate drive voltages of IGBT (v_{GE}) and MOSFET (v_{GS}) of the proposed converter. The gate signal of MOSFET lasts for 800 ns and overlaps with the falling edge of the IGBT gate signal for 100 ns. These data are precise as originally designed.

The corresponding IGBT voltage (v_{S1}), IGBT current (i_{S1}), and IGBT power loss (p_{S1}) are illustrated in Fig. 21, and the corresponding MOSFET voltage (v_{Sa1}), MOSFET current (i_{Sa1}), and MOSFET power loss (p_{Sa1}) are depicted in Fig. 22. The IGBT and MOSFET voltages are the same because they

TABLE IV
SWITCHING LOSSES FROM EXPERIMENT

Converter Type (Number of Switch)	Switching Losses (W) @ I_{ref} = 5 A, Speed= 200 rpm, and f_s = 5 kHz
Standard (2 IGBTs)	4.8
Proposed (2 IGBTs + 2 MOSFETs)	3.9

are connected in parallel. The soft-switching characteristics of IGBT can be observed. A minor overlap between the IGBT voltage and current substantially reduces the switching loss. Nevertheless, the additional power loss of MOSFET should be included. The area under the power loss curve of IGBT is calculated as 150 μJ, and the energy of MOSFET is identified as 240 μJ. These values can be summed up to 390 μJ per switch pair. Correspondingly, the switching loss of each IGBT/MOSFET pair is computed as 1.95 W.

Two IGBT switches are used in each phase of the standard converter. In the modified converter, two IGBT/MOSFET pairs are employed. Therefore, twice of the per-IGBT and per-IGBT/MOSFET pair switching losses are the switching losses of the standard and modified converters, respectively.

These switching losses are summarized in Table IV. The experimental results suggest that the switching loss is reduced with the proposed converter by 0.9 W. This finding relatively corresponds to the previous simulation result (1.1 W).

Consequently, the switching frequency is increased to 25 kHz, and the converters are experimentally verified at three rotor speeds. The converter losses are obtained from the difference between the measured input and output powers.

The total losses of both converters at 200, 400, and 600 rpm are shown in Fig. 23, and the test results are compared with the simulation results reported in Fig. 13. Correspondingly, the findings reveal some acceptable differences. The loss of the proposed converter approximately ranges from 5.2 W to 7.5 W, which is lower than that of the standard converter.

After the converter efficiencies are verified experimentally, the efficiency graphs are plotted against the rotor speeds (Fig. 24). The tested efficiencies are compared with the corresponding simulation results (Fig. 14), and a good agreement is achieved. The efficiency of the modified converter is improved by 1.87% to 3.43% from that of the standard converter.

Finally, when the rotor speed is fixed at 200 rpm, the power losses of both converters at different switching frequencies (5 kHz to 25 kHz) are obtained experimentally (Fig. 25). The same tendency is observed when the test results are compared with the simulation ones (Fig. 15). The measured loss of the standard converter increases linearly with the switching frequency, but that of the modified converter remains almost unchanged at around 16.2 W to 16.8 W.

The converter efficiency graphs from the experiments are

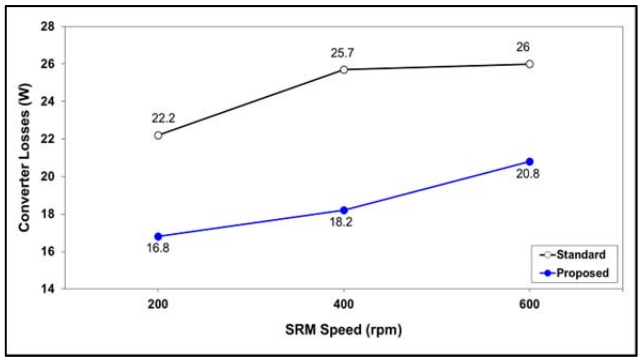


Fig. 23. Converter losses versus SRM speed from the experiment at the switching frequency of 25 kHz.

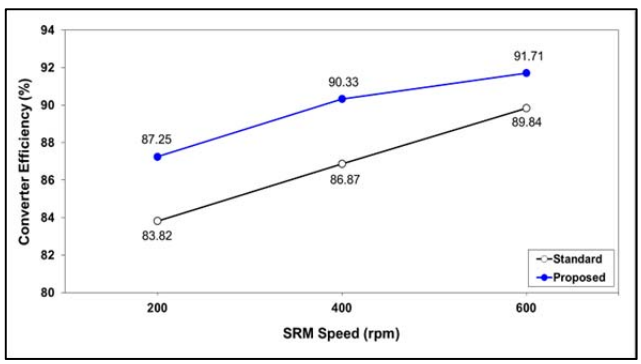


Fig. 24. Converter efficiency versus SRM speed from the experiment at the switching frequency of 25 kHz.

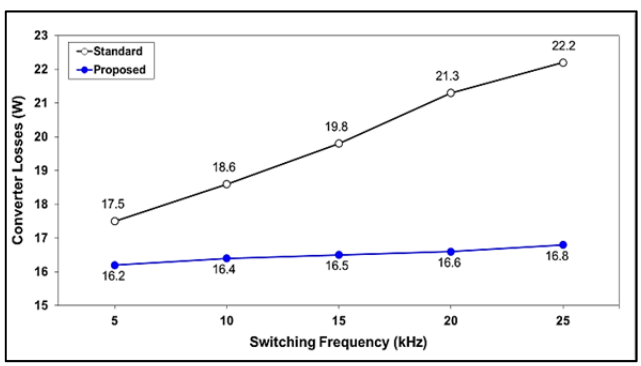


Fig. 25. Converter losses versus switching frequency from the experiment at the SRM speed of 200 rpm.

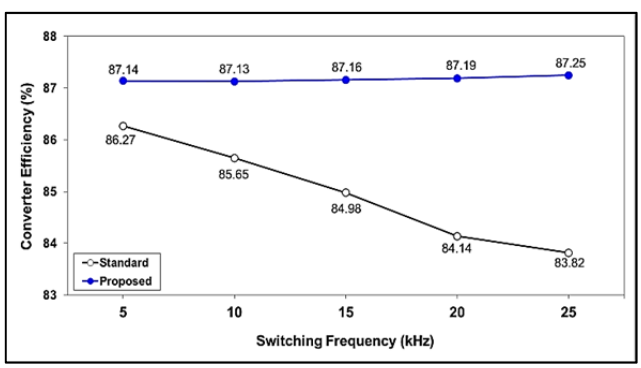


Fig. 26. Converter efficiency versus switching frequency from the experiment at the SRM speed of 200 rpm.

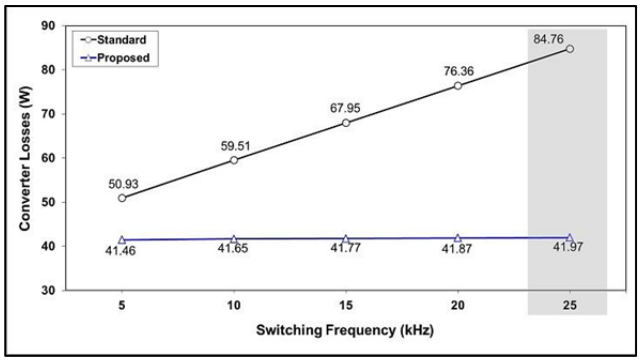


Fig. 27. Simulated converter losses versus switching frequency (RL Load, regulated current: 5 A, and DC-link voltage: 500 V).

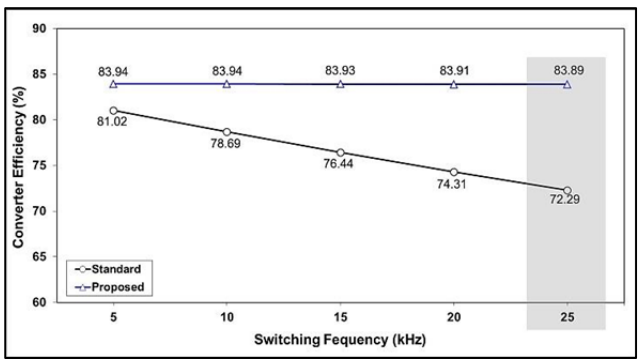


Fig. 28. Simulated converter efficiency versus switching frequency (RL Load, regulated current: 5 A, and DC-link voltage: 500 V).

then plotted against the switching frequencies (Fig. 26). Again, the results agree well with those obtained in the previous simulation (Fig. 16). The efficiency of the proposed converter remains nearly constant at around 87.14% to 87.25% independent of the switching frequency used. By contrast, the measured efficiency of the standard converter decreases linearly when the switching frequency is increased. However, the improved efficiency at the 25-kHz switching frequency is still not substantial (around 3.43%) because of the limitation of this research (i.e., the SRM used has a relatively low DC-link voltage of 200 V). If a large-sized SRM with a high DC-link voltage is deployed, then the benefit of the proposed converter is vivid. In other words, the switching loss reduction using the modified technique is outstanding, especially in systems with high switching frequency and DC-link voltage.

To confirm this proposition, a computer simulation of the proposed converter with a 500-V DC-link voltage supplying the RL load is conducted. The same IGBT and MOSFET are used in this case, in which the regulated current is 5 A. The simulation results shown in Figs. 27 and 28 confirm that the modified asymmetric half-bridge converter can function efficiently. At 25 kHz, the switching loss reduction of almost 42.79 W is achieved. Accordingly, the converter efficiency is significantly improved as high as 11.60%. At this large scale, the energy saved because of the switching loss reduction can compensate for or even offset the additional cost of extra MOSFET switches required in the proposed converter.

VI. Conclusion

This study presents a novel means for improving the efficiency of the asymmetric half-bridge converter for a three-phase, 12/8 SRM operated in low speed with the current chopping mode. The proposed technique employs the mixed parallel operation of IGBT (chopping switch) and MOSFET (auxiliary switch). In each pair of switches, MOSFET is activated before the turn-off interval of IGBT, thereby maintaining a zero voltage across the switches. Therefore, the turn-off switching losses of the IGBT are significantly reduced. The chopping switches do not have voltage and current stresses as normally observed in resonance-based soft-switching techniques. As shown by the developed mathematical expressions, the power losses of the modified converter are considerably minimized compared with those of the standard asymmetric half-bridge converter. A comparative study of both SRM converters operated below base speed is clearly presented in this paper. Computer simulation and experimental results verify the validity of the new method. Correspondingly, the proposed converter can be applied to low-speed heavy-duty equipment and traction drives such as forklift trucks.

Appendix

SRM data:
Number of phases = 3
Number of poles (stator/rotor) = 12/8
Alignment-to-unalignment displacement = 22.5° (0.393 rad)
DC-link voltage = 200 V
Reference (rated) current = 5 A
Rated power = 375 W
Phase resistance = 2 Ω
Aligned inductance = 100 mH
Unaligned inductance = 15 mH

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