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Reduction of Common Mode Voltage in Asymmetrical Dual Inverter Configuration Using Discontinuous Modulating Signal Based PWM Technique

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Abstract

Conventional space vector pulse width modulation based asymmetrical dual inverter configuration produces high common mode voltage (CMV) variations. This CMV causes the flow of common mode current, which adversely affects the motor bearings and electromagnetic interference of nearby electronic systems. In this study, a simple and generalized carrier based pulse width modulation (PWM) technique is proposed for dual inverter configuration. This simple approach generates various continuous and discontinuous modulating signals based PWM algorithms. With the application of the discontinuous modulating signal based PWM algorithm to the asymmetrical dual inverter configuration, the CMV can be reduced with a slightly improved quality of output voltage. The performance of the continuous and discontinuous modulating signals based PWM algorithms is explored through both theoretical and experimental studies. Results show that the discontinuous modulating signal based PWM algorithm efficiently reduces the CMV and switching losses.

Key words: Asymmetrical dual inverter configuration, Common mode voltage, Continuous modulating signal, Discontinuous modulating signal, Induction motor, Scalar PWM, Space vector PWM

I. INTRODUCTION

With the advancement in power semiconductor technology, induction motors receive considerable importance in variable speed drive applications. Three-phase voltage source inverter (VSI) is widely used power electronic converter for induction motor drive applications. Various PWM techniques have been employed to control the output voltage and frequency of VSI [1]-[7]. Among these methods, the continuous PWM (CPWM) (e.g, space vector PWM) and discontinuous PWM (DPWM) techniques display satisfactory performance in terms of DC bus utilization, switching losses, and current ripple [1]-[7]. However, these techniques exhibit high common mode voltage (CMV), which is the potential difference between the neutral point of induction motor and ground.

Correspondingly, high switching frequency is employed in VSI to increase its efficiency and reduce its current ripple and filter size. Nonetheless, at high switching frequencies, the sharp edges of CMV cause common mode current, which adversely affects motor bearings [8], [9]. This particular effect can be reduced actively and passively. Passive methods use passive components such as inductors, transformers, and other passive elements [10], [11]. Nevertheless, these passive elements increase the cost, size, and weight of inverter. Active methods involve multilevel inverter topologies [12]-[14] and modified pulse patterns for VSI topologies [15]-[17].

The modified pulse pattern methods for the conventional

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two-level VSIs apply the active zero state PWM [15]-[17] and near state PWM [16], [17] methods to reduce CMV without using any extra components. These methods reduce CMV with a slightly increased ripple in line current because of the opposite pulses in line voltage.

The multilevel inverter topologies, such as diode clamped inverter [12] and H-bride inverter topologies [13], [14], moderately reduce CMV with an output voltage of improved quality. However, the operation of these topologies requires clamping diodes, voltage balancing capacitors, and separate DC sources, which increase the cost and weight of the multilevel inverter with reduced efficiency. Moreover, these conventional multilevel inverter topologies have a few drawbacks, including neutral point fluctuations [18] and complex control algorithms. To overcome these drawbacks, the dual inverter topology, a new multilevel inverter topology, was introduced for induction motor drive applications [19]-[26]. In this inverter configuration, the neutral point of squirrel-cage induction motor is removed, and a total of six stator terminals are available as shown in Fig. 1. Correspondingly, an open end winding induction motor is realized.

The open end winding induction motor is fed by two 2-level inverters from both ends as shown in Fig. 2. This setup is called a dual inverter configuration, which is popular in high power applications (e.g., submarine, electric vehicles, and electric locomotives). This particular configuration can be classified into symmetrical [20] and asymmetrical [21] configurations (Fig. 2) based on the application of input DC voltage. In these configurations, two 2-level inverters feed the induction motor from both ends to generate 3- and 4-level output voltages with the same number of switching devices [21].

The related literature has discussed various modulating strategies for controlling output voltage. However, these methods cannot reduce the CMV variations. Therefore, [25] presented a modified circuit topology for symmetrical dual inverter configuration. Nonetheless, this topology eliminates CMV with output voltage of poor quality. Consequently, many researchers [26] have tried to reduce CMV by improving the quality of output voltage with different converter topologies, which use several switching devices and complex control algorithms.

In this study, simple scalar based control algorithms are presented for four-level asymmetrical dual inverter configuration to reduce CMV with an output voltage of good quality. In particular, this study analyzes the conventional CPWM algorithm for asymmetrical dual inverter topology. A discontinuous modulating signal based PWM algorithm is then proposed to reduce the CMV. The proposed approach also reduces the switching losses of inverters. To validate the proposed method, experimental studies are performed, and the results are presented.

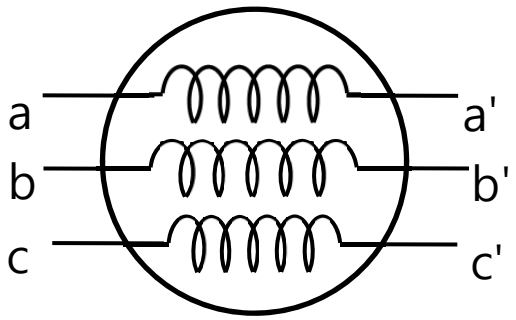
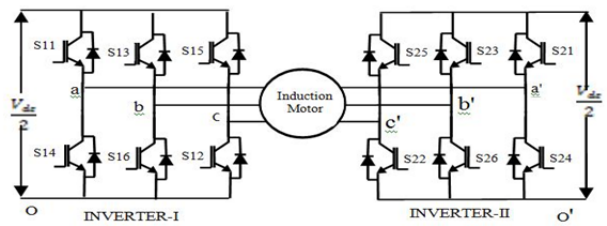
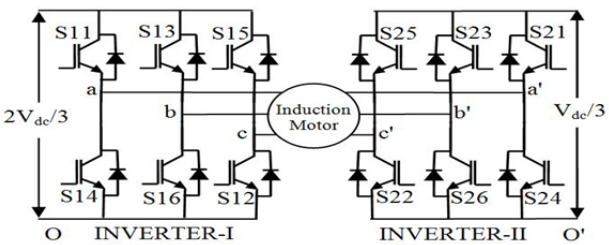


Fig. 1. Open end winding induction motor.



(a) symmetrical.



(b) asymmetrical.

Fig. 2. Dual inverter configurations.

II. ASYMMETRICAL DUAL INVERTER CONFIGURATION

The asymmetrical dual inverter circuit configuration shown in Fig. 2(b) is a combination of two 2-level inverter topologies. Input voltages $2V_{dc}/3$ and $V_{dc}/3$ are applied to inverters-I and -II, respectively, to achieve the four-level output voltage. In this case, V_{ao}, V_{bo}, and V_{co} are the pole voltages of inverter-I, $V_{a'o'}$, $V_{b'o'}$, and $V_{c'o'}$ are the pole voltages of inverter-II, $V_{aa'}$, $V_{bb'}$, and $V_{cc'}$ are the effective phase voltages, and V_{ab}, V_{bc}, and V_{ca} are the line voltages. The potential $V_{oo'}$ is the CMV. For an input DC voltage of $2V_{dc}/3$, inverter-I generates a pole voltage of 0 or $2V_{dc}/3$. Inverter-II yields a pole voltage of 0 or $V_{dc}/3$for an input voltage of $V_{dc}/3$. Substituting these individual pole voltages in (1) yields the effective pole voltages. The switching pattern and effective pole voltages generated by the asymmetrical dual inverter configuration are given in Table I.

$$V_{xox'o'} = V_{xo} - V_{x'o'} \qquad x = a,b,c \tag{1}$$

Table I indicates that the dual inverter configuration can produce a four-level pole voltage, and it is therefore called as a four-level inverter topology. The expression of CMV ($V_{oo'}$)

can be derived from the pole voltages as shown below.

$$V_{cm} = \frac{V_{ao} - V_{a'o'} + V_{bo} - V_{b'o'} + V_{co} - V_{c'o'}}{3} = V_{oo'} \quad (2)$$

To control the output voltage and frequency, PWM techniques are employed for the asymmetrical dual inverter configuration. In general, PWM techniques can be implemented based on scalar and space vector approaches [6]. This study mainly focuses on scalar-based PWM techniques.

III. Conventional Continuous Modulating Signal based Scalar PWM Algorithm

The control signals of the scalar PWM algorithm are generated by comparing the reference signals (modulating signals; V_r) with a high frequency carrier signal (triangular; V_t).Fig. 3 illustrates that the intersection points define the switching instants. A scalar PWM technique generally provides freedom for the selection of reference [7] and carrier signals [15]. Therefore, for the three-phase 2-level inverter topology, three reference signals are compared with a common carrier signal to generate the control signals.

From the concept of scalar PWM techniques for multilevel inverters [14], N-1 level shifting carrier signals are required to generate the control signals for an N-level inverter topology. As the proposed asymmetrical dual inverter configuration is capable of generating four-level output voltage, three-level shifting triangular signals are required (Fig. 4).

The comparison of reference signals with three-level shifting triangular signals as given in Table II generates the control signals. Table II presents the switching logic for phase-a of inverters-I and -II.

In the same manner of generating control signals for the three-phase dual inverter configuration, three sinusoidal reference signals, each with a120°phase displacement, are compared with common-level shifting triangular signals. The mathematical expressions for the three reference signals are given in (3).

$$\begin{aligned} V_a &= \cos(\omega t) \\ V_b &= \cos(\omega t - 2\pi/3) \\ V_c &= \cos(\omega t - 4\pi/3) \end{aligned} \quad (3)$$

With the isolation of DC link voltages of each inverter (the isolation of terminals O and O' shown in Fig. 2(b)), the triplen harmonic current path does not exist in the three-phase dual inverter configuration. In such condition, the potential $V_{OO'}$ can be freely varied by injecting a zero-sequence signal to the commended reference signals given in (3). The addition of zero-sequence signal improves the DC bus utilization and influences the harmonic distortion. The zero-sequence signal and resultant modulating signals can be obtained with the following equations [7]:

$$V_{zs} = \frac{V_{dc}}{2}(2a_o - 1) - a_o V_{\max} + (a_o - 1)V_{\min} \quad (4)$$

TABLE I

Effective Pole Voltage Calculation

Switches to be made ON in Inverter-I	Inverter -I Pole Voltage	Switches to be made ON in Inverter-II	Inverter -II Pole Voltage	Effective pole voltage
S14 or S16 or S12	0	S25 or S23 or S21	$V_{dc}/3$	$-V_{dc}/3$
S14 or S16 or S12	0	S22 or S24 or S26	0	0
S11 or S13 or S15	$2V_{dc}/3$	S25 or S23 or S21	$V_{dc}/3$	$V_{dc}/3$
S11 or S13 or S15	$2V_{dc}/3$	S22 or S24 or S26	0	$2V_{dc}/3$

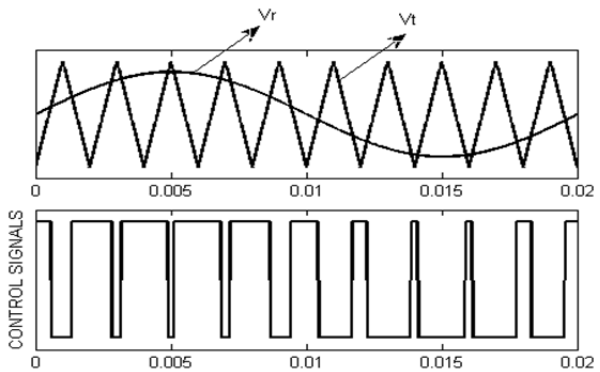


Fig. 3. Realization of scalar PWM.

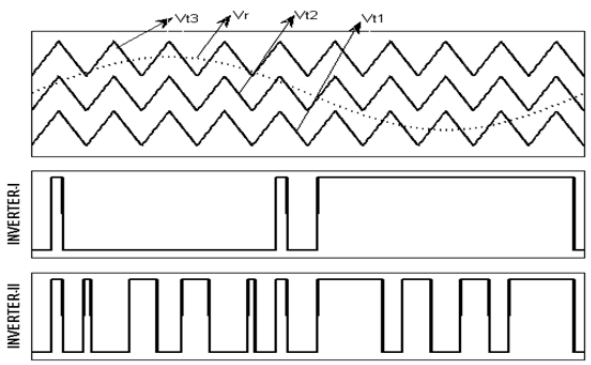


Fig. 4. Realization of scalar PWM technique for the asymmetrical dual inverter configuration.

TABLE II

Generation of Switching Logic

Condition	Switch Status
$V_r > V_{t1}, V_r > V_{t2}$ and $V_r > V_{t3}$	$S_{11} = OFF, S_{14} = ON$ $S_{21} = ON, S_{24} = OFF$
$V_r > V_{t1}, V_r > V_{t2}$ and $V_r < V_{t3}$	$S_{11} = OFF, S_{14} = ON$ $S_{21} = OFF, S_{24} = ON$
$V_r > V_{t1}, V_r < V_{t2}$ and $V_r < V_{t3}$	$S_{11} = ON, S_{14} = OFF$ $S_{21} = ON, S_{24} = OFF$
$V_r < V_{t1}, V_r < V_{t2}$ and $V_r < V_{t3}$	$S_{11} = ON, S_{14} = OFF$ $S_{21} = OFF, S_{24} = ON$

$$V_i^* = V_i + V_{zs} \qquad i = a,b,c \tag{5}$$

where V_{max} and V_{min} are the maximum and minimum of commended reference signals given in (3) at a given instant, respectively.

In (4), the zero-sequence signal is generated based on the voltage magnitude test. Constant a_o lies between 0 and 1.

The block diagram shown in Fig. 5 illustrates the scalar PWM algorithm for the dual inverter configuration. With proper selection of the zero-sequence signal (for different values of a_0 between 0 and 1) various continuous and discontinuous modulating signals are generated [7]. These modulating signals are compared with high frequency level shifting triangular signals to generate the pulses for inverters-I and -II. The most commonly used zero-sequence signal (with a_o=0.5) and the resultant continuous modulating signals are shown Fig. 6.

The use of the continuous modulating signal with common level shifting carrier signals produces a conventional continuous modulating signal based PWM technique as discussed in [21].

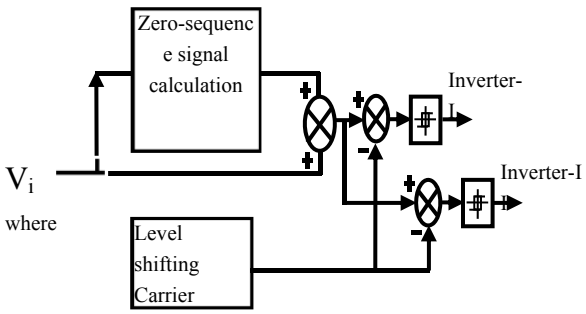


Fig. 5. Block diagram illustrating the scalar PWM technique for the dual inverter configuration.

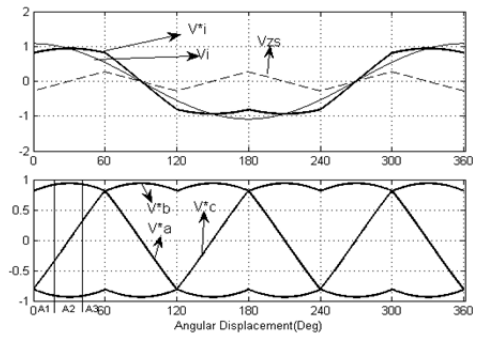


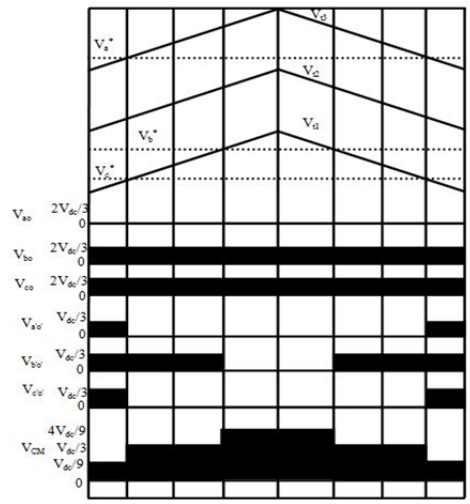
Fig. 6. Modulating and zero-sequence signals.

IV. Pulse Pattern Of PWM Techniques

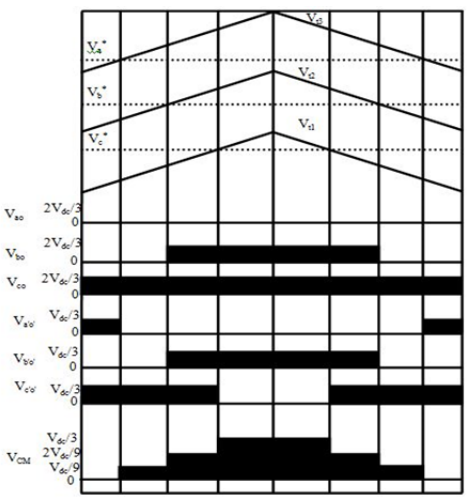
The three-phase continuous modulating signals shown in Fig. 6 demonstrate that within the modular range of $0°\leq\omega t\leq60°$, V^*_a, V^*_c, and V^*_b have maximum , minimum, and intermediate values, respectively. For every 60°, these values vary. Therefore, the entire modular range is divided into six intervals. All these intervals are symmetrical; thus, the discussion is limited to the modular range of $0°\leq\omega t\leq60°$. To generate the pulse pattern, the modulating signals are compared with level shifting carrier signals (i.e., V_{t1},$V_{t2,}$, and V_{t3}) as shown in Fig. 4. In the modular range $0°\leq\omega t\leq60°$, V^*_a has a maximum instantaneous value and is compared with V_{t3}. Contrarily, V^*_c has a minimum instantaneous value and therefore intersects with V_{t1}.V^*_b has an intermediate value in the modular range $0°\leq\omega t\leq60°$, but its value is near to V^*_c and V^*_a at the start and end points, respectively. Hence, at the beginning of interval ($0°\leq\omega t\leq60^0$) V^*_b is compared with V_{t1}, at the ending of interval with V_{t3} and for a part of time with V_{t2}. Based on this modular range, $0\leq\omega t\leq60°$ is again divided into three regions (i.e., A1,A2, and A3) as shown in Fig. 6. Because of this reason pulse pattern of the asymmetrical dual inverter configuration is analyzed at three different regions in the modular range of $0°\leq\omega t\leq60°$.

In all regions, a small time period (Ts=1/fs; carrier frequency) is considered for the analysis. Thus, the modulating signals appear as appear as straight lines as shown in Fig. 6. The discussion is conducted based on pole voltages because these voltages are replicas of the pulse pattern. In Fig. 7, three modulating signals (i.e., V_a^*, V_b^*, and V_c^*) intersect with three different level shifting carrier signals (i.e., V_{t1}, $V_{t2,}$,and V_{t3}). Based on switching logic given in Table II inverters-I and -II pole voltages are shown in Fig. 7. At any instant, inverter-I generates a pole voltage of 2Vdc/3 or 0, and inverter-II generates a pole voltage of Vdc/3 or 0.CMV can be calculated from the individual pole voltages with (2). The bottom traces in Fig. 7 imply that the value of CMV generated by the conventional continuous modulating signal based PWM algorithm may vary between $-V_{dc}/9$ and $4V_{dc}/9$.

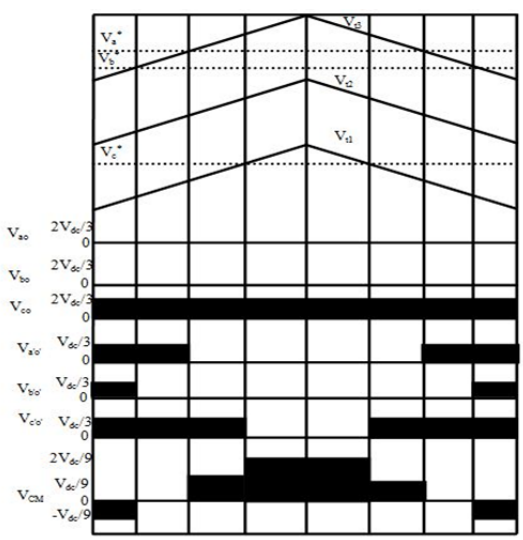
In Fig. 7(a), the CMV has a maximum value of $4V_{dc}/9$ with a multilevel jump from $V_{dc}/9$ to $V_{dc}/3$. As previously mentioned, scalar PWM techniques generally provide freedom for the selection of reference and carrier signals. With this freedom, if the position of reference signal is changed the PWM technique gives significant advantages. With the change in position of reference signals V^*_a or V^*_c, the CMV is reduced. However, with the clamping of reference signal V^*_a as shown in Fig. 8(a) along with CMV reduction phase-a switching is reduced. In particular, Fig. 8(a) reveals that the peak value of CMV generated in region A1 is reduced to a magnitude of $V_{dc}/3$ from $4V_{dc}/9$ with reduced phase-a switching of inverter-II. The pole voltages of the inverters and the generated CMV at instant A2 with continuous modulating signal based PWM technique are shown in Fig. 7(b). With the clamping of phase-a as shown in Fig. 8(b),the CMV is decreased from $V_{dc}/3$ to $2V_{dc}/9$. Similarly, when phase-a is clamped in region A3, the CMV is reduced from $2V_{dc}/9$ to $V_{dc}/9$. With the clamping of phase-a in the entire modular range of $0°\leq\omega t\leq60°$, the CMV is decreased from $-V_{dc}/9$ and $4V_{dc}/9$ to $-V_{dc}/9$ and $V_{dc}/3$, respectively. With the clamping of phase-c in region A3 (Fig.



(a) A1.



(b) A2.



(c) A3.

Fig. 7. Resulting output pole voltages of inverters and CMV with the continuous modulating signal based PWM algorithm in regions.

8(c)), the CMV in that region is reduced from $-V_{dc}/9$ and $2V_{dc}/9$ to 0 and $2V_{dc}/9$, respectively. Hence, the CMV in the modular range ($0° \le \omega t \le 60°$) is decreased from $-V_{dc}/9$ and $4V_{dc}/9$ to 0 and $V_{dc}/3$, respectively. Therefore, to reduce the CMV and switching losses within the modular function range of $0° \le \omega t \le 60°$, in region A1 phase-a is clamped, in region A2 phase-a clamped and in region A3 phase-c is clamped. This type of symmetry is repeated in the entire modular range of ($0° \le \omega t \le 360°$) to reduce the CMV.

V. Discontinuous Modulating Signal Based Scalar PWM Algorithm

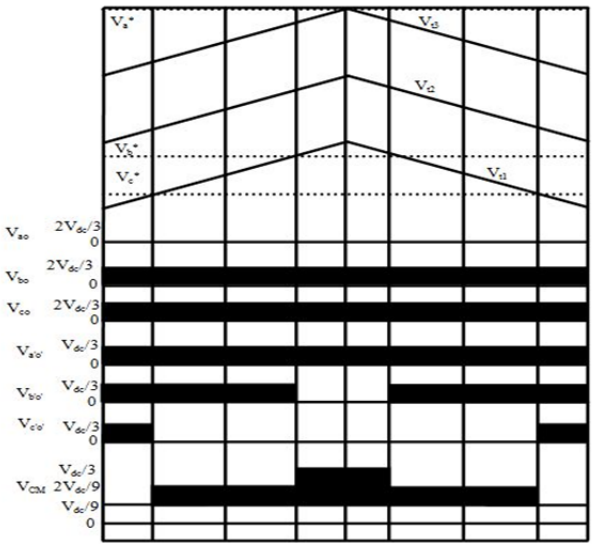
In the previous discussion and analysis, in the modular function range $0° \le \omega t \le 60^0$, in region A1 phase-a is clamped, in region A2 phase-a is clamped and in region A3 phase-c is clamped respectively. Based on observation, it can be generalized by using simple maximum and minimum magnitude test to the commended reference signals (i.e., V_a,V_b, and V_c). The magnitudes of these reference signals are calculated. If the signal has a maximum value and the intermediate signal is near to the minimum value signal, then the signal which is having maximum value is clamped to the positive DC bus. In the similar manner if the signal has a minimum value and the intermediate signal is near to the maximum value signal, then the signal which is having minimum value is clamped to the negative DC bus.

Based on observation of modulating signals in the entire modulation range, the modulating signals are almost similar to those (DPWM1) shown in Fig. 9 as discussed in [6]. Each modulating signal is clamped to either a positive or negative DC bus for a period of 120°. As such, the switching of the corresponding device is ceased.

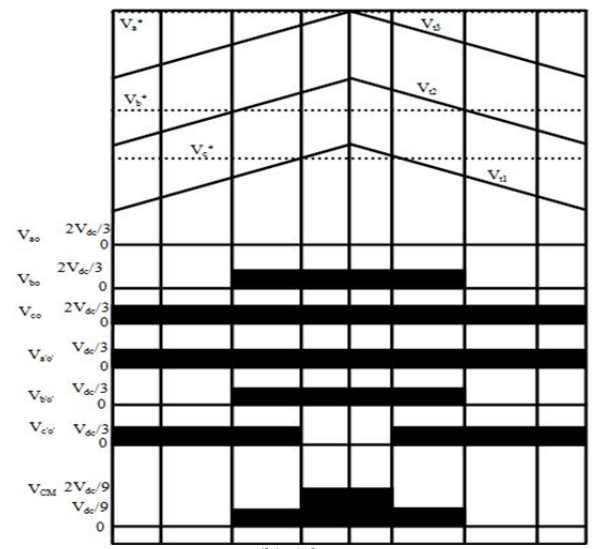
Similar to the continuous modulation signal, the discontinuous modulating signals shown in Fig. 9 can also be expressed mathematically. Three reference signals (V_i) are considered as depicted in (3), and zero sequence (V_{zs}) is added to the reference signals as in (4). Therefore, a new set of reference or modulating signals (V^*_i) is obtained as in (5). The graphical representation of the reference signal, zero-sequence signal, and obtained modulating signals are shown in Fig. 9(a). Figs. 6(a) and 9(a) demonstrate that the commended reference signals are the same, but the zero-sequence signal is changed. In (4), constant a_o is set as 0.5 in the entire modular range to obtain the continuous modulating signal. To generate the discontinuous modulating signal as in Fig. 9, constant a_o is set as 0 or 1 in the entire modular range. The value of a_o is chosen based on the following equations:

$$V_{\max} + V_{\min} < 0 \text{ then } \quad a_o = 0$$
$$V_{\max} + V_{\min} \ge 0 \text{ then } \quad a_o = 1 \tag{6}$$

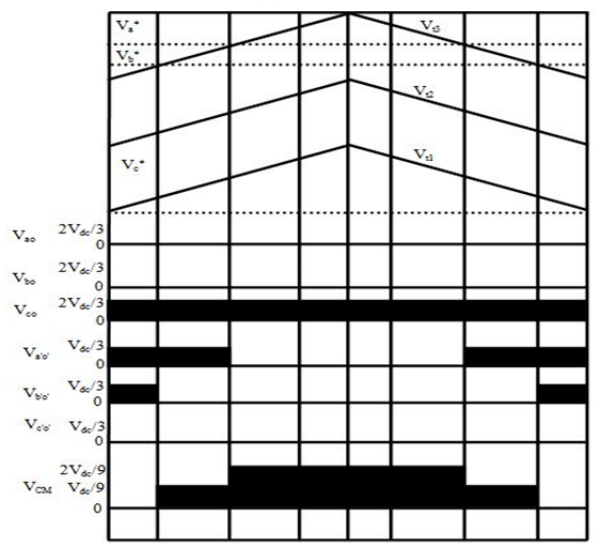
where V_{max} and V_{min} are the maximum and minimum values of the commended reference signals (i.e., V_a,V_b, and V_c),



(a) A1.



(b) A2.



(c) A3.

Fig. 8. Pulse pattern of the discontinuous modulating signal based PWM algorithm in regions.

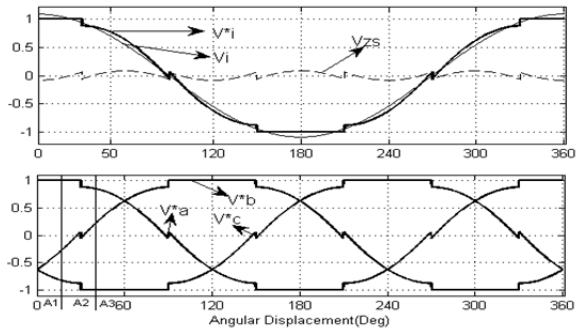
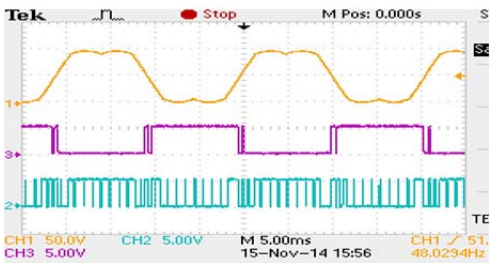
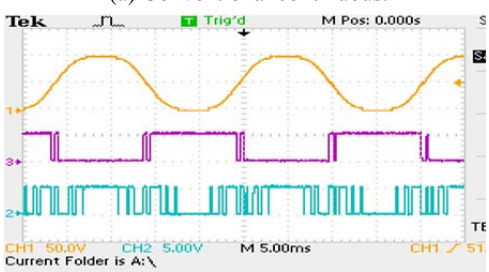


Fig. 9. (a) Modulating signals and zero-sequence signals. (b) three-phase modulating signals.



(a) Conventional continuous.



(b) Discontinuous modulating signal based PWM techniques at M=0.87.

Fig. 10. Modulating signal, inverter-I A-phase pulse pattern, inverter-II A-phase pulse pattern.

respectively. Table III lists the values of constant a_0.

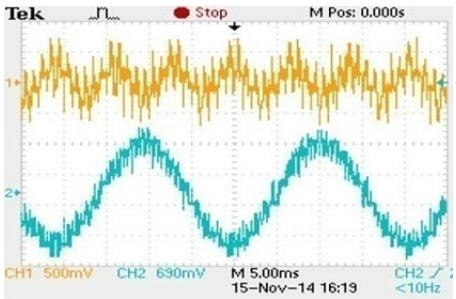
VI. Results and Discussion

To validate the performance of the proposed PWM techniques, various numerical simulation studies are conducted on a v/f controlled induction motor drive. A prototype model of the asymmetrical dual inverter fed induction motor is developed, and control signals are generated based on the carrier comparison approach using a dSPACE 1104 control board. The carrier frequency is set as 1 kHz for the experimental studies.

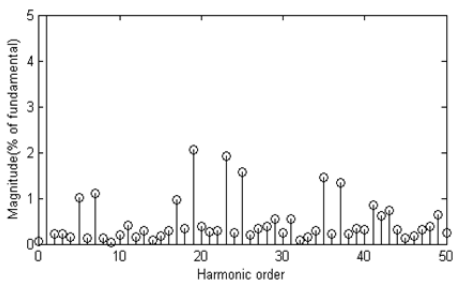
The three-phase induction motor (with 1Hp, 415V, 1.8A, and 50Hz) is fed from two 9.2 kVA PWM inverters with uncontrolled rectifiers at the front end. A DC bus voltage of 200V is employed to inverter-I, and 100V is employed to inverter-II. Therefore, an effective DC voltage of 300V is adopted. To observe the results in a digital storage oscilloscope 500V to 3.3V regulator (LV20-P) is employed. As depicted in Fig. 10, the inverter with high input voltage is

TABLE III
a_o VALUES FOR VARIOUS MODULATING SIGNALS

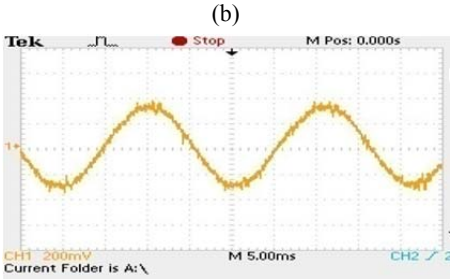
Type of modulating signal	a_o Value
Continuous modulating signal	0.5
Discontinuous modulating signal	$V_{max} + V_{min} < 0$ then $a_o = 0$ $V_{max} + V_{min} \geq 0$ then $a_o = 1$



(a)



(b)

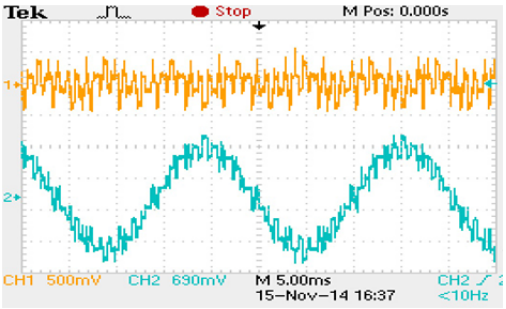


(c)

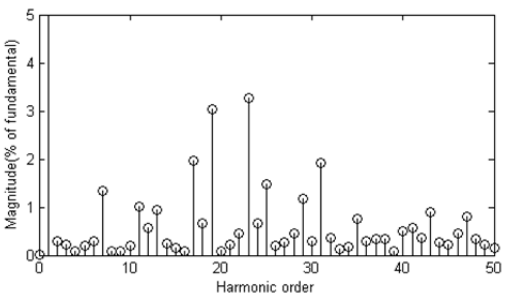
Fig. 11. (a) CMV and effective phase voltage. (b) harmonic spectrum of effective phase voltage. (c) A-phase stator current with conventional continuous modulating signal based PWM technique at M=0.87 and fs=1000Hz.

operated with low frequency ,whereas the inverter with low input DC voltage is operated with high frequency. With the continuous modulating signal, inverter-II is continuously switched (Fig. 10(a)). However, this inverter is clamped for a time period of $T_0/3$(output frequency fo=$1/T_0$) with the discontinuous modulating signal (Fig. 10 (b)).

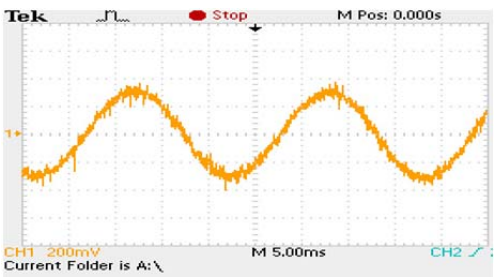
With the discontinuous modulating signal, the switching of inverter-II is reduced as well as its switching losses. The CMV, effective phase voltage, harmonic spectrum of effective phase voltage, and a-phase stator currents with continuous and discontinuous modulating signal based PWM techniques are shown in Figs.11 and 12.



(a)



(b)



(c)

Fig. 12. (a) CMV and effective phase voltage. (b) Harmonic spectrum of effective phase voltage. (c) A-phase stator current with conventional discontinuous modulating signal based PWM technique at M=0.87 and fs=1000Hz.

With an effective DC input voltage of 300 V and continuous modulating signal based PWM technique, the CMV varies between –33.3V ($-V_{dc}/9$) and 133.3 V ($4V_{dc}/9$). The frequency of CMV is three times that of the output voltage frequency (f_o). With the application of the discontinuous modulating signal based PWM technique (by clamping any one phase at a time), the CMV is reduced from –33.3 V ($-V_{dc}/9$) and 133.3 V ($4V_{dc}/9$) to 0 V and 100 V ($V_{dc}/3$), respectively. Therefore, the CMV is reduced by 40% with the discontinuous modulating signal based PWM technique.

The phase-a stator current under no-load condition is shown in Figs. 11(c) and 12(c). The switching frequency is maintained constant at 1 kHz for both the continuous and discontinuous modulating signal based PWM techniques. In this event, the harmonic spectrum exhibits a large amount of energy at the harmonics (multiples) of switching frequency (around 20 as shown in Figs. 11(b) and 12(b)). Compared with the continuous modulating signal based PWM

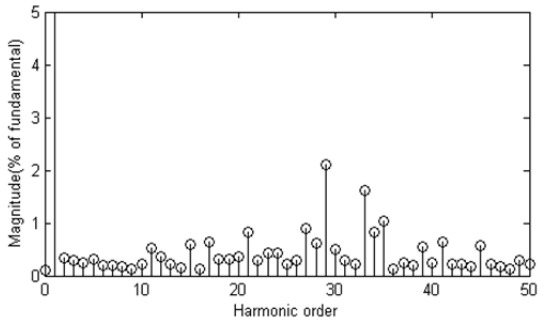


Fig. 13. Harmonic spectrum of effective phase voltage with discontinuous modulating signal based PWM technique at fs=1500Hz.

technique, the discontinuous modulating signal based PWM technique produces a high total harmonic distortion.

When the average switching frequency is maintained constant (1 and 1.5 kHz for the continuous and discontinuous modulating signal based PWM techniques, respectively), the discontinuous modulating signal based PWM techniques exhibit better performance in terms of the total harmonic distortion (Fig. 13) than the continuous modulating signal based PWM techniques.

The preceding analysis verifies that at high modulation index the discontinuous modulating signal based PWM technique and at low modulation index continuous modulating signal based PWM technique show a satisfactory performance in reducing CMV. When the modulation index decreases, the discontinuous modulating signal based PWM techniques show high CMV. Therefore, the drives with discontinuous modulating signal based PWM technique should be operated at high modulation index to efficiently reduce the CMV and harmonics.

VII. CONCLUSION

Conventional control strategies for two-level inverter topologies reduce the CMV by decreasing the quality of output voltage. In this study, continuous and discontinuous modulation signal based PWM techniques were discussed for the asymmetrical dual inverter configuration. In particular, the pulse pattern and implementation of these PWM techniques were analyzed. Theory of CMV reduction was verified by theory and laboratory experiments. The research results confirmed that the clamping of modulating signal to either a positive or negative DC bus reduces the CMV by maintaining the same quality of output voltage at high modulation index. Along with the CMV, the reduction switching losses of the inverters were reduced with the application of discontinuous modulating signal based PWM techniques.

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