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Wavelet PWM Technique for Single-Phase Three-Level Inverters

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Abstract

The wavelet PWM (WPWM) technique has been applied in two-level inverters successfully, but directly applying the WPWM technique to three-level inverters is impossible. This paper proposes a WPWM technique suitable for a single-phase three-level inverter. The work analyzes the control strategy with the WPWM and obtains the design of its parameters. Compared with the SPWM technique for a single-phase three-level inverter under the same conditions, the WPWM can obtain high magnitudes of the output fundamental frequency component, low total harmonic distortion, and simpler digital implementation. The feasibility experiment is given to verify of the proposed WPWM technique.

Key words: Single-phase three-level inverters, Sinusoidal pulse width modulation (SPWM), Wavelet modulation

I. INTRODUCTION

In recent years, Saleh has proposed and developed the wavelet modulation techniques on different two-level converters [1]-[5]. The wavelet modulation technique is based on establishing a non-dyadic type multi resolution analysis (MRA), which is required to support a non-uniform recurrent sampling–reconstruction process. The merits of this approach includes simpler realization by digital algorithm, higher magnitudes of the fundamental output voltage, and lower harmonic contents better than other types of modulation techniques. In [1] and [2], the manner of implementation of a wavelet modulation technique for single-phase voltage source inverters was proposed. The manner of implementation of a wavelet modulation technique for three-phase voltage-source six-pulse inverters was proposed in [3] and [4]. In [5], the manner of implementation of a wavelet modulation technique for AC–DC converters was proposed. Hence, the present research on the WPWM technique focuses on the two-level inverter.

Compared with the two-level inverter, the three-level inverter is a new type of high-voltage large capacity power converter with advantages of having improved voltage waveform on the AC side, smaller filter size, lower electromagnetic interference, and lower acoustic noise [6]. Therefore, three-level inverter options are attracting greater attention in the fields of the grid interconnection, new energy, fuel electromagnetic [7], [8]. Because of the wide application of three-level inverters, the study of its control strategy has been increasingly highlighted [9]-[15]. One of commonly used control strategies is sinusoidal pulse width modulation (SPWM). The SPWM technique for two-level inverters only needs a modulating signal and a carrier signal, but the conventional SPWM technique for three-level inverters needs a modulating signal, two carrier signals, and a square signal. Thus, directly applying the WPWM technique to three-level inverters is impossible because the WPWM technique to two-level inverters can only generate two unipolar-controlled signals or two bipolar-controlled signals.

Thus, this paper presents the development and performance testing of the WPWM technique for single-phase three-level inverters. The single-phase three-level inverter with SPWM technique is reviewed in Section II. The single-phase three-level inverter with WPWM technique is proposed in Section III. The analysis of the WPWM technique for the single-phase three-level inverter is provided in Section IV. The experimental results are obtained in Section V. Conclusions are given in Section VI.

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II. SINGLE-PHASE THREE-LEVEL INVERTER WITH SPWM TECHNIQUE

Fig. 1 shows the circuit schematic of an asymmetric single-phase three-level inverter [17], [18]. The circuit is composed of a two-level bridge and a three-level bridge. C_1 and C_2 are the DC side filter capacitor. U_d is the DC voltage source. When U_d=E, Uao has three levels, i.e., +E/2, 0, and –E/2, and U_{bo} has two levels: +E/2, and –E/2, which, in total, gives output voltage U_{ab} five levels. The operation states of single-phase three-level inverter are listed in TABLE I.

A conventional SPWM scheme is shown in Fig. 2 [18], which has a reference rectified sine wave (V_{ref}) and two carrier signals (v_{tri1} and v_{tri2}). The comparison result of V_{ref} and v_{tri1} is the control signal of A_1; the comparison result of V_{ref} and v_{tri2} is the control signal of B_1; the comparison result of V_{ref} and zero is the control signal of C_1. Then, the control signals for switches S_1–S_6 can be derived by A_1, B_1, and C_1, as shown in Fig. 3, where $S_1 = A_1$ and $C_1 + \overline{B_1}$ and $\overline{C_1}$; $S_2 = \overline{S_4}$; $S_3 = \overline{S_1}$; $S_4 = A_1$ and $\overline{C_1} + \overline{B_1}$ and C_1 ; $S_5 = \overline{C_1}$; and $S_6 = C_1$.

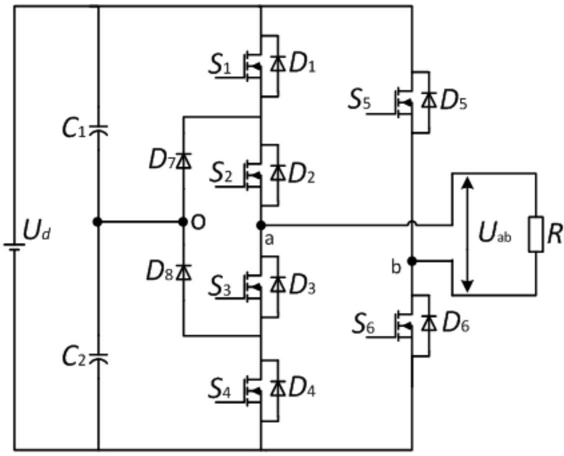


Fig. 1. Scheme of the single-phase three-level inverter.

TABLE I
OPERATION STATES OF THE SINGLE-PHASE THREE-LEVEL INVERTER

The turned-on switches	The turned-off switches	U_{ab}
S_1 S_2 S_6	others	+E
S_2 S_3 S_6	others	E/2
S_3 S_4 S_6	others	0
S_3 S_4 S_5	others	-E
S_2 S_3 S_5	others	-E/2
S_1 S_2 S_5	others	0

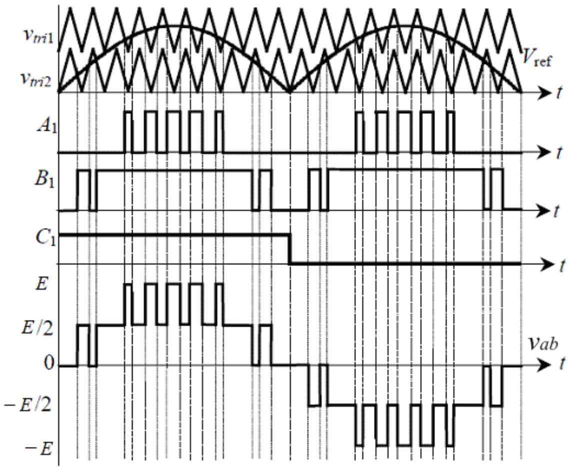


Fig. 2. SPWM operation principle of the three-level inverter.

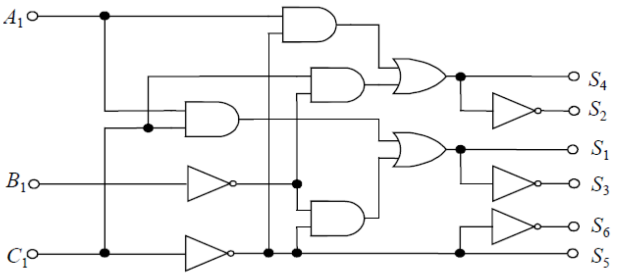


Fig. 3. Logic control scheme for switches S1–S6.

III. WPWM TECHNIQUE FOR SINGLE-PHASE THREE-LEVEL INVERTER

A. *Principle of the WPWM Technique*

The WPWM technique is based on sampling–reconstructing a reference-modulating signal in a non-uniform recurrent manner using sets sampling and synthesis basis functions [1,2]. These sampling basis functions are generated as dilated and translated versions of the scale-based linearly-combined scaling function $\varphi_{(j,k)}(t)$. Furthermore, synthesis basis functions are generated as dilated and translated versions of the scale-based linearly combined synthesis scaling function $\tilde{\varphi}_{(j,k)}(t)$. The scale-based linearly-combined scaling function is defined at scale j as

$$\varphi_j(t) = \phi_H(2^{j+1}t) + \phi_H(2^{j+1}(t-1+2^{-(j+1)})) \qquad (1)$$

and $\varphi_{(j,k)}(t) = \varphi\left(2^j t - k\right)$, where j=0, 1, 2, 3, … and $\phi_H(t)$ is the Harr scaling function that is given by $\phi_H(t) = \begin{cases} 1 & t \in [0,1] \\ 0 & t \notin [0,1] \end{cases}$.

Moreover, synthesis scaling function $\tilde{\varphi}(t)$ associated with $\varphi(t)$ can be defined as

$$\tilde{\varphi}_j(t) = (\phi_H)_j(t) - \varphi_j(t) \text{ and } \tilde{\varphi}_{(j,k)}(t) = \tilde{\varphi}\left(2^j t - k\right). \qquad (2)$$

Using these two dual scaling functions, a continuous-time signal $x_c(t)$ can be expanded as

$$x_c(t) = \sum_k \sum_j \left\langle x_c(t), \varphi\left(2^j t - k\right)\right\rangle \tilde{\varphi}\left(2^i t - k\right) \qquad (3)$$

where j, $k \in$ Z, where Z is the set of integer numbers. Such form of signal processing suggests that a continuous-time signal $\left\langle x_c(t), \varphi\left(2^j t-k\right)\right\rangle$ can be recovered from its samples using sets of synthesis functions $\tilde{\varphi}\left(2^j t-k\right)$.

The work on [10] proved that the switching pulses for the inverter can be generated by using dilated and shifted versions of synthesis scaling function $\tilde{\varphi}_{(j,k)}(t)$. When each cycle of $x_c(t)$ is divided by a finite number of sample groups *D*, the length of the time interval of the sample group [t_{d1}, t_{d2}] changes as scale j changes, where

$$\begin{aligned} t_{d1} &= d+2^{-j-1} \\ t_{d2} &= d+1-2^{-j-1}, d=0,1,2,\cdots,(D-1) \end{aligned} . \quad (4)$$

In addition, based on the the procedure on how to implement the WPWM technique given in [1], the flowchart for WPWM can be shown as Fig. 4 [16], where Tm is the period of the reference sine wave.

B. WPWM Strategy for the Single-Phase Three-Level Inverter

According to the above flowchart of WPWM, once T_m, *j*0 and *D* are given, the time points (t_{d1} and t_{d2}) of each sample group can be calculated, and the driving pulses can be generated by the time points in each sample group, which can be integrated into two unipolar-controlled signals (W_1 and W_2). However, the signals (W_1 and W_2) cannot be used to control the switches of single-phase three-level inverter directly. Thus, based on Figs. 2 and 3, the WPWM operation principle for the three-level inverter can be shown as Fig. 5. W_1 and W_2 are generated according to the flowchart of the WPWM technique shown in Fig. 4. Pulse P_1 has a half-cycle symmetry property, its frequency is the double of reference sine wave, and its pulse width can be varied to adjust the distribution of the output voltage levels, which will be discussed in detail in the following. Pulse C_1 is a square signal, and its frequency is the same as the reference sine wave. Then, the control signals for switches S_1–S_6 can be derived by the specific logic relationship among W_1, W_2, P_1, and C_1, as shown in Fig. 6, where

$$\mathrm{S1}=\overline{S_3}=\overline{W_1}\,\&\,\overline{W_2}\,\&\,\overline{P_1}\,\&\,\overline{C_1}+(W_1+W_2)\&P_1\&C_1$$

$$\mathrm{S4}=\overline{S_2}=\overline{W_1}\,\&\,\overline{W_2}\,\&\,\overline{P_1}\,\&C_1+(W_1+W_2)\&P_1\&\,\overline{C_1} \quad (5)$$

and

$$\mathrm{S6}=\overline{S_5}=C_1.$$

Moreover, Fig. 6 shows that the WPWM control strategy for the single-phase three-level inverter can be implemented simply by a digital algorithm.

IV. ANALYSIS OF THE WPWM TECHNIQUE FOR THE SINGLE-PHASE THREE-LEVEL INVERTER

To verify the control strategy of the WPWM technique for the single-phase three-level inverter, a MATLAB/SIMULINK model is built and simulation is made by selecting *D*=30, f_m=50 Hz (f_m is the frequency of the reference sine wave), *j*0=0, the

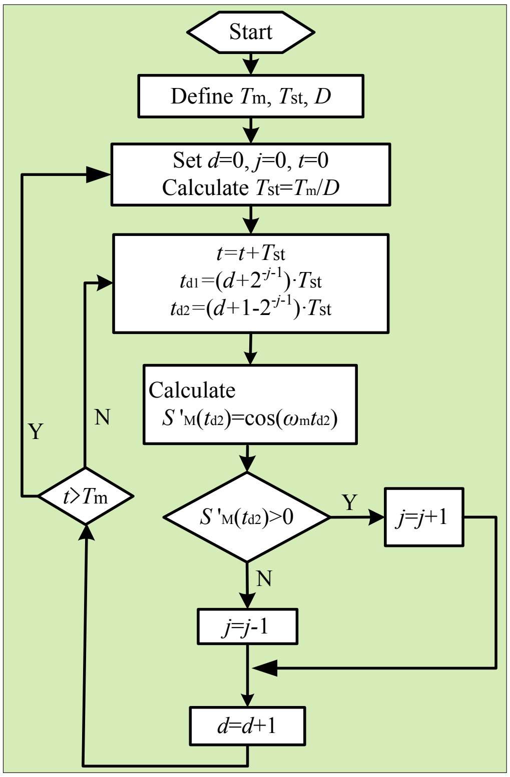


Fig. 4 Flowchart of the WPWM technique implementation.

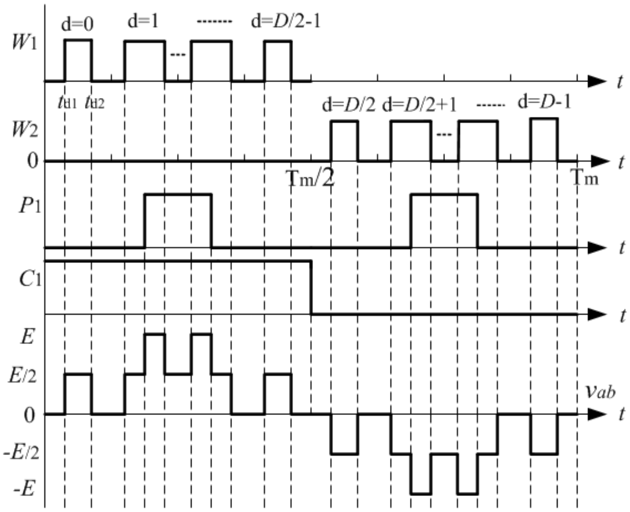


Fig. 5. WPWM operation principle of three-level inverter.

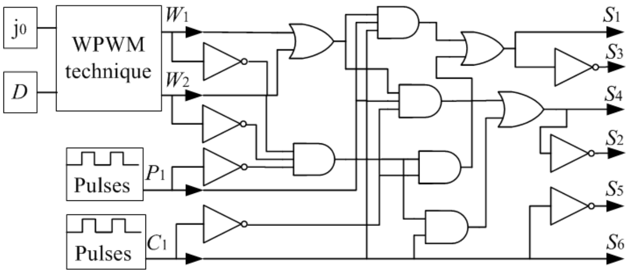


Fig. 6. Logic control scheme for the switches S_1~S_6 with WPWM technique.

pulse width of P_1 is 50%, the simulation results of signals W_1, W_2, W_3, P_1, C_1, and S_1–S_6 can be obtained, as shown in Fig. 7. When input voltage U_d=50 V, output voltage U_{ab} is shown in Fig. 8.

According to the control strategy of the WPWM technique for the single-phase three-level inverter, the width and position of the pulses (W_1 and W_2) generated by the WPWM technique are determined when D and $j0$ are given, and C_1 is a determined square wave when the frequency of the reference sine wave is given. Therefore, the only way of changing the control signals for switches S_1–S_6 is by adjusting the pulse width of P_1, the distribution of the output voltage levels is affected.

To analyze the effects of pulse P_1 on the distribution of the output voltage levels, this study selects D=30, f_m=50 Hz, $j0$=0, and input voltage U_d=50 V as a sample object to be simulated based on the MATLAB/SIMULINK model of a single-phase three-level inverter, as shown in Fig. 2. The pulse width of P_1 is chosen in the range of 10%–90%. The simulation results of the total harmonic distortion (THD) and the amplitude of fundamental voltage V_1 for output voltage U_{ab} are shown in Figs. 9 and 10, respectively. Fig. 9 shows that the THD is smallest when the pulse width of P_1 is about 62%. Fig. 10 shows that V_1 increases as the pulse width of P_1 increases, and V_1 can be larger than the input voltage when the pulse width is larger than 50%.

V. EXPERIMENTAL RESULTS

To verify the analysis of the WPWM technique for the single-phase three-level inverter, the algorithm of the WPWM technique is implemented by using DSP (TMS320LF2812), and the input voltage of the single-phase three-level inverter is $V_{dc} = 50\text{V}$, MOSFET IRFPE40 is selected as switch, TLP250 is used as driver, and pure resistance R = 50 Ω is used as the load. A photograph of the experimental setup is shown in Fig. 11. Note that the value of the THD is tested by Fluke Norma 5000 Power Analyzer.

First, the experiments have been performed by choosing f_m=50 Hz, $j0$=0, D=30, and the pulse width of P_1=40%, 50%, 60%, 62%, 63%, 70%, 80%, and 90%. The experimental results are shown in Fig. 12. Fig. 12(a) shows that the THD is smallest when the pulse width of P_1 is about 62%, and Fig. 12(b) shows that V_1 increases as the pulse width of P_1 increases, which are consistent with the simulation results shown in Figs. 9 and 10.

Second, the experiments have been performed by choosing f_m=50 Hz, $j0$=0, the pulse width of P_1 =62%, and D=20, 30, 40. The experimental results are shown in Figs. 13(a)-13(c). Fig. 13 shows that using the WPWM technique to control the single-phase three-level inverter is effective.

Finally, to validate the performance of the single-phase three-level inverter with the WPWM technique, this paper

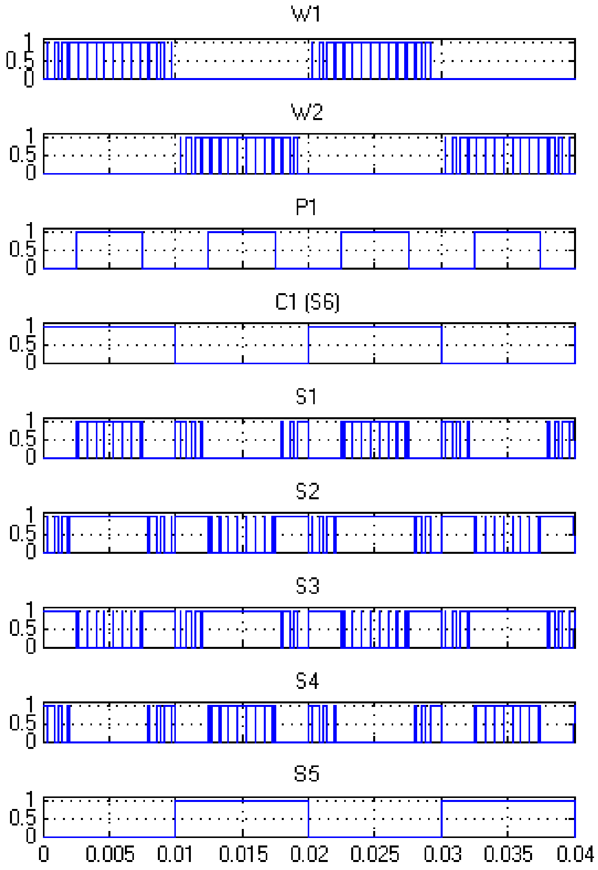


Fig. 7. Signals of W_1, W_2, W_3, P_1, C_1, and S_1–S_6 at D=30, f_m =50 Hz, $j0$=0.

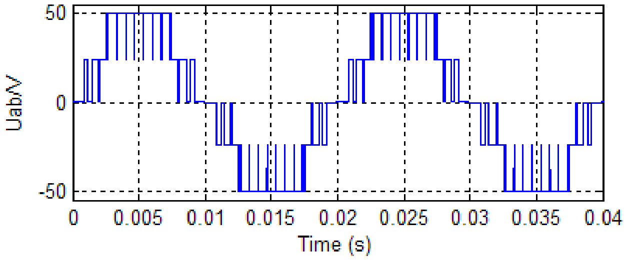


Fig. 8. Output voltage U_{ab}.

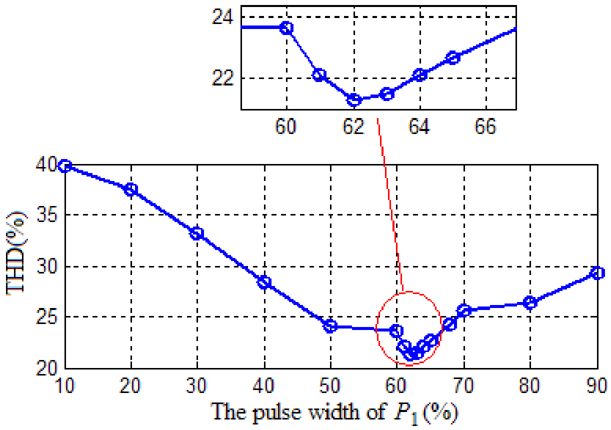


Fig. 9. THD of U_{ab} vs. the pulse width of P_1.

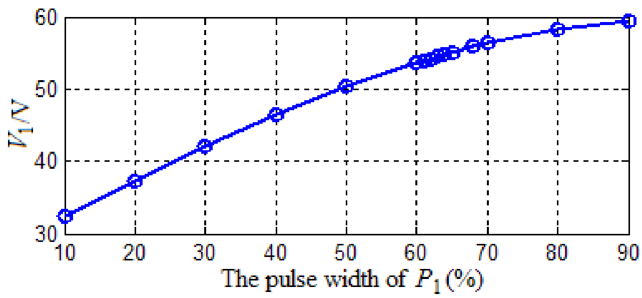


Fig. 10. V_1 of U_{ab} vs. the pulse width of P_1.

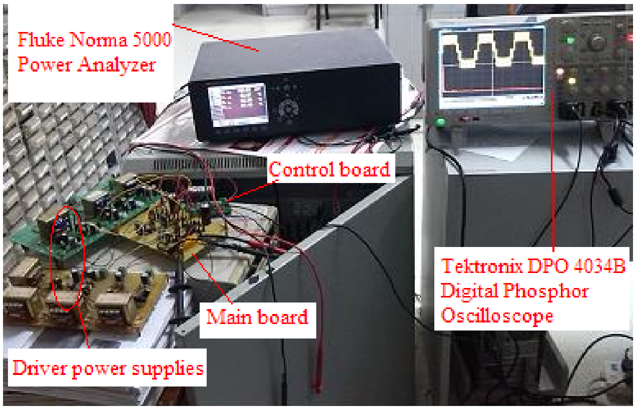
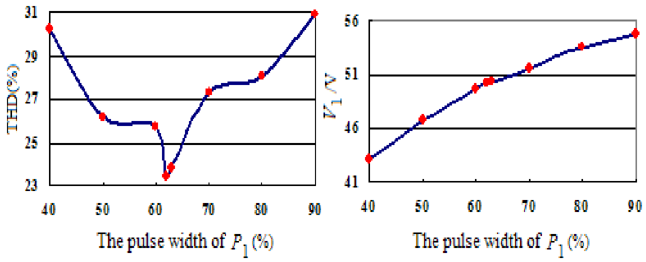


Fig. 11. Photograph of the experimental setup.



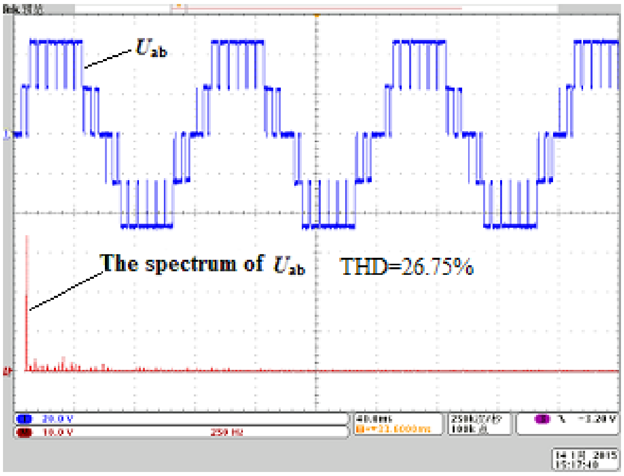
(a) THD. (b) V_1.

Fig. 12. Experimental results of the THD and V_1 vs. the pulse width of P_1 at j0=0, f_m=50 Hz, D=30.

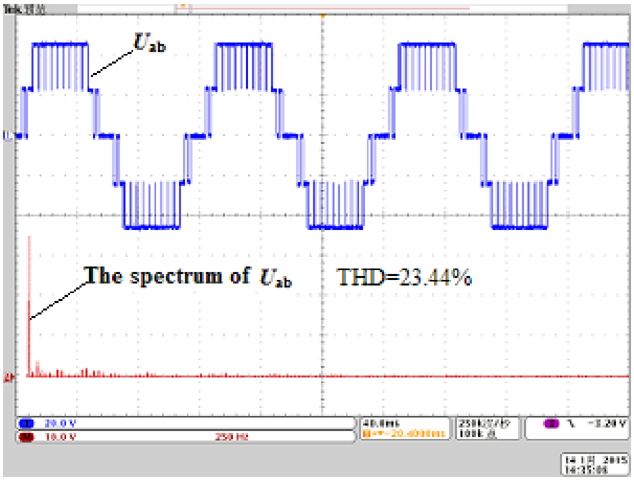
TABLE II

COMPARISON OF RESULTS BETWEEN WPWM AND SPWM FROM FIGS. 13 AND 14

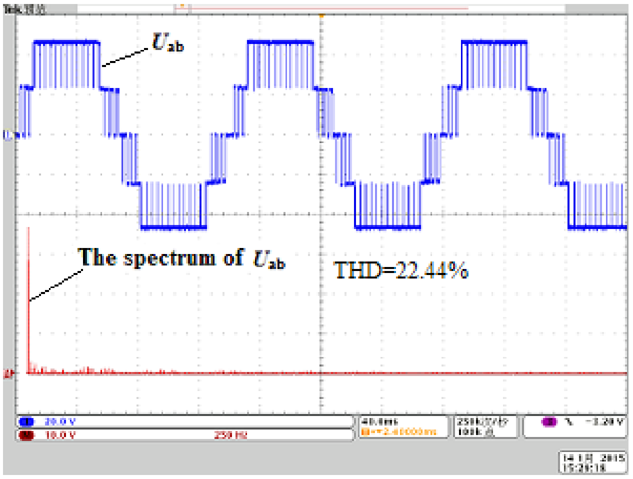
Switching frequency		WPWM	SPWM
f_s =1 kHz (D=20)	V_{1rms}(V)	34.38	31.9
	THD(%)	26.75	28.24
f_s =1.5 kHz (D=30)	$V_{1\ rms}$(V)	35.28	32.01
	THD(%)	23.44	28.01
f_s =2 kHz (D=40)	$V_{1\ rms}$(V)	36.70	32.07
	THD(%)	22.44	27.94



(a) D=20.



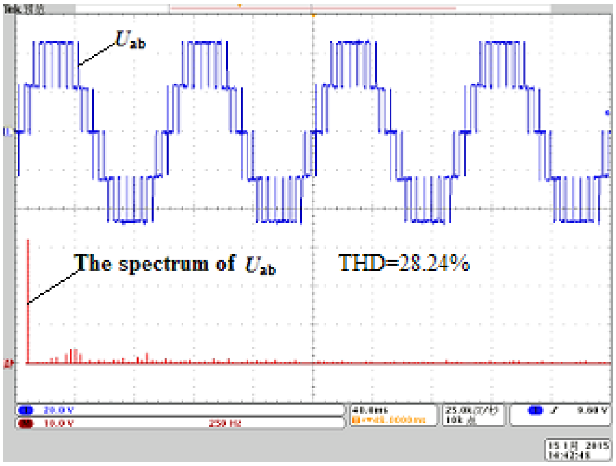
(b) D=30.



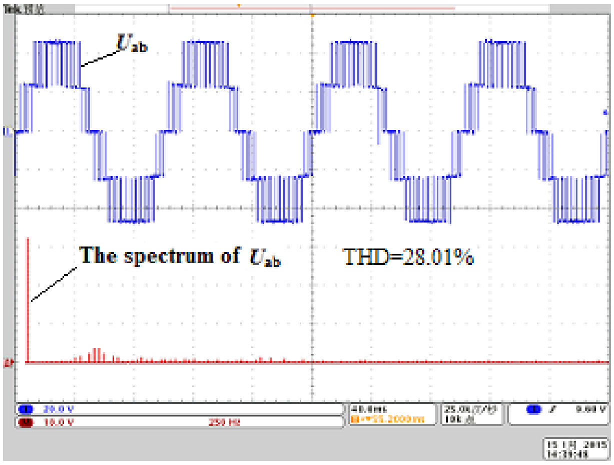
(c) D=40.

Fig. 13. Output voltage U_{ab} and its spectrum of the single-phase three-level inverter by WPWM.

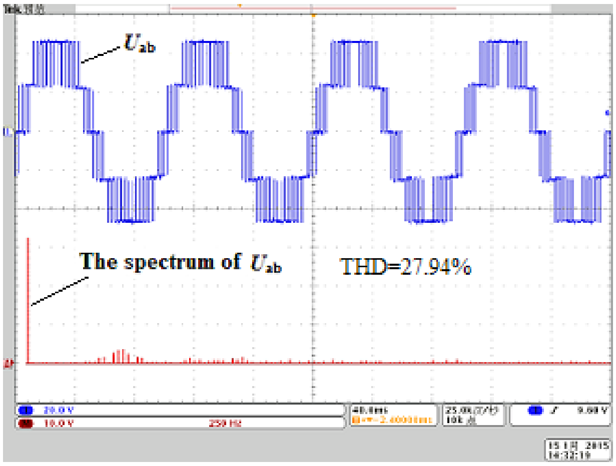
compares the WPWM with conventional SPWM, as shown in Fig. 2. The algorithm of the conventional SPWM is implemented by using DSP (TMS320LF2812), and the experiments have been performed by choosing f_m=50 Hz, m=1.0 (m denotes the modulation index), the switching frequency f_s =1 kHz (D=20), f_s =1.5 kHz (D=30), and f_s =2 kHz (D=40). The experimental results are shown in Fig. 14(a), (b), (c) respectively.



(a) f_s =1 kHz.



(b) f_s =1.5 kHz.



(c) f_s =2 kHz.

Fig. 14. Output voltage U_{ab} and its spectrum of the single-phase three-level inverter by the SPWM.

The compared results between WPWM and SPWM from Figs. 13 and 14 are listed in TABLE II. From TABLE II, it can be concluded that (1) WPWM can get higher magnitudes of the fundamental component than SPWM; (2) WPWM technique can get smaller THD and more disperser spectrum than SPWM.

VI. CONCLUSION

This study has developed the WPWM technique for single-phase three-level inverters. The design of the parameter for the WPWM is obtained by analyzing the magnitudes of the fundamental frequency component and harmonic distortion of its output voltage. The simulation and experimental results have shown that the proposed WPWM for the three-level inverter can obtain higher magnitudes of the output fundamental frequency component, lower THD, and simpler digital implementation than the SPWM, which will promote the application of WPWM technique in power electronics converters.

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REFERENCES

[1] S. A. Saleh, C. R. Moloney, and M. A. Rahman, "Developing a nondyadic MRAS for switching DC–AC inverters," in *Proc. IEEE 12th DSP Conf, Jackson Lake Lodge, WY*, pp. 544-549, Sep. 2006.

[2] S. A. Saleh, C. R. Moloney, and M. A. Rahman, "Development and testing of wavelet modulation for single-phase inverters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 7, pp. 2588-2599, Jul. 2009.

[3] S. A. Saleh and M. A. Rahman, "Development and testing of a new controlled wavelet modulated inverter for IPM motor drives," *IEEE Trans. Ind. Appl.*, Vol. 46, No.4, pp. 1630-1643, Jul./Aug. 2010.

[4] S.A. Saleh, C. R. Moloney, and M. A. Rahman, "Analysis and development of wavelet modulation for three phase voltage source inverters," *IEEE Trans. Ind. Electron.* Vol. 58, No. 8, pp. 3330-3348, Aug. 2010.

[5] S. A. Saleh and M. A. Rahman, "Development and experimental validation of resolution-level controlled wavelet modulated inverters for three phase induction motor drives," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 4, pp. 1958-1970, Jul./Aug. 2011.

[6] S. A. Saleh, "The implementation and performance evaluation of 3φVS wavelet modulated AC-DC converters," *IEEE Trans. Power Electron.*, Vol. 28, No. 3, pp. 1096-1106, Mar. 2013.

[7] J.-S. Lai and F. Z. Peng, "Multilevel converters - a new breed of power converters," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 3, pp. 509-517, May/Jun. 1996.

[8] G. W. Chang, H.-W. Lin, and S.-K. Chen, "Modeling characteristics of harmonic currents generated by high-speed railway traction drive converters," *IEEE Trans. Power Deliv.*, Vol. 19, No. 2, pp. 766-773, Apr. 2004.

[9] K.-H. Chao, P.Y. Chen, C.-H. Cheng, "A three-level converter with output voltage control for high-speed railway tractions," *The 33rd Annual Conf. IEEE Ind. Electron. Society (IECON), Taipei, Taiwan*, pp. 1793-1798, Nov. 2007.

[10] R. M. Tallam, R. Naik, and T. A, Nondahl, “A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters,” *IEEE Trans. Ind. Appl.*, Vol. 41, No. 6, pp. 1734-1743, Nov. 2005.
[11] W. Song, X. Feng, and C. Xiong, “A neutral point voltage regulation method with SVPWM control for single-phase three-level NPC converters,” in *Proc. IEEE VPPC Conference*, pp. 1-4, Sep. 2008.
[12] R. Salehi, N. Farokhnia, M. Abedi, and S. H. Fathi, “Elimination of low order harmonics in multilevel inverter using genetic algorithm,” *Journal of Power Electronics*, Vol. 11, No. 2, pp. 132-139, Mar. 2011.
[13] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, “An improved pulse width modulation method for chopper-cell-based multilevel inverters,” *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3472-3481, Aug. 2012.
[14] A. Marzoughi, H. Imaneini, and A. Moeini, “An optimal selective harmonic mitigation technique for high power converters,” *International Journal of Electrical Power and Energy Systems*, Vol. 49, pp. 34-39, Jul. 2013.
[15] M. Zhang, L. Huang, W. Yao, and Z. Lu. “Circulating harmonic current elimination of a CPS-PWM-based modualr mulitlevel converter with a plug-in repetitive controller,” *IEEE Trans. Power Electron.*, Vol. 29, No.4, pp. 2083-2097, Apr. 2014.
[16] C. F. Zheng, X. M. Xu, B. Zhang, and D. Y. Qiu, “Inverter’s characteristic analysis under different parameters of Wavelet PWM Technique,” *EPE’14 ECCE, Europe*, pp. 1-7, Aug. 2014.
[17] X.-H. Wang and X. B. Ruan, “SPWM control single-phase three-level inverter,” in *Proc. of the CSEE*, Vol. 25, No. 1, pp. 73-76, Jan. 2005.
[18] F. J. Wu, B. Sun, and H. R. Peng, “Single-phase three-level SPWM scheme suitable for implementation with DSP,” *Electronics Letters*, Vol. 47, No. 17, pp. 994-996, Aug. 2011.

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