

Control Strategy of MMC-HVDC under Unbalanced Grid Voltage Conditions

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Abstract

High voltage direct current transmission based on modular multilevel converter (MMC-HVDC) is one of the most promising power transmission technologies. In this study, the mathematical characteristics of MMC-HVDC are analyzed in a synchronous rotational reference frame. A hybrid current vector controller based on proportional integer plus resonant is used to uniformly control the DC and double-base frequency AC currents under unbalanced grid voltage conditions. A corresponding voltage dependent current order limiter is then designed to solve the overcurrent problems that may occur. Moreover, the circulating current sequence components are thoroughly examined and controlled using a developed circulating current suppressor. Simulation results verify the correctness and effectiveness of the proposed control schemes.

Key words: Circulating current, HCVC, MMC, VDCOL

I. INTRODUCTION

The high voltage direct current transmission based on modular multilevel converter-hybrid current vector controller (MMC-HVDC) is one of the most promising power converter technologies, especially for transmitting offshore wind power and providing passive grids with power [1]-[3]. The control strategies and inner loop current controller critically influence the performance of MMC-HVDC under unbalanced grid voltage conditions. A dual current vector control scheme (DCVC), which includes positive and negative sequence current vector controllers, was introduced in [4]-[6]. This scheme has been applied to MMC-based HVDC systems [7]-[12]. Nonetheless, the control system has become relatively complex because of the existence and availability of four current vector controllers and additional current sequence extraction module. Other improved controllers, such as proportional resonant (PR), were also proposed to uniformly control the positive and negative sequence currents [13]-[17]. However, the current transformation between two different reference frames (i.e., d q and α β) is required to obtain the inner loop current reference. These related studies failed to

discuss the active power ripples suppressing method and the voltage dependent current order limiter (VDCOL).

Given that the capacitor in a submodule (SM) is subjected to a fundamental frequency current, ripples are superimposed on each SM voltage. The three-phase parallel connected arms shown in Fig. 1 may have different voltages. Consequently, circulating currents are produced, distorting the sinusoidal arm current and increasing the rated current of power devices [18]. An effective circulating current suppressing controller (CCSC) for MMC based on the negative sequence synchronous rotational reference frame was proposed in [19]. Nevertheless, this controller could not completely suppress the positive and zero sequence circulating currents under unbalanced grid voltages [8]. Another CCSC was designed based on PR controller to control all the circulating current components [20]. However, this device needs a high pass filter to separate the circulating current sequences, and it may affect the control performance. A CCSC was developed based on proportional integer plus resonant to control the circulating current, but it requires the zero sequence circulating current to be controlled individually [8].

Under unbalanced grid voltage conditions, DC and double-base frequency AC currents exist in MMC systems (for grid AC current and arm current). Therefore, this study uses an HCVC based on proportional integer plus resonant to uniformly control the DC and AC currents in a positive synchronous rotational reference frame. This control scheme

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not only avoids the transformation between dq and $\alpha\beta$, but also reduces the number of current controllers from four to two as the PR control. In this case, the control system is simple. The VDCOL is designed according to the relationship between the positive and negative sequence voltages. Moreover, the circulating current, including the positive, negative, and zero sequences, is analyzed, and a circulating current controller is developed based on a low-pass filter and the HCVC. The current sequence components are suppressed uniformly, and the effect of the high-pass filter is mitigated. The remainder of the paper is organized into six sections. Following the Introduction, Section II introduces the generic structure of MMC and its mathematical model in a synchronous rotational frame. Section III presents the control scheme, including the current reference calculation method, VDCOL, grid voltage sequence extraction method, and the HCVC. Section IV explains the modulation method and the circulating current sequence component. Section V presents the simulation results of the control strategies, and Section VI cites the conclusions of the study.

II. SYSTEM STRUCTURE AND MATHEMATICAL MODEL

Fig. 1 shows the general circuit structure of a three-phase MMC in HVDC applications. This structure consists of six arms, each containing N serial connected and nominally identical half-bridge SMs.

The relationship between the grid and valve side voltages under the three-phase static reference frame is expressed as follows:

$$(L_T + 0.5L) \frac{di_j}{dt} = u_{sj} - u_j \quad (1)$$

where $j \in (a, b, \text{ and } c)$.

Equation (2) can be deduced from (1), where u_{sd} , u_{sq} , u_d , and u_q are the voltages in the grid and valve sides, i_d and i_q are the currents in the synchronous rotational reference frame.

$$\begin{cases} (0.5L + L_T) \frac{di_d}{dt} = u_{sd} - u_d + \omega(0.5L + L_T) i_q \\ (0.5L + L_T) \frac{di_q}{dt} = u_{sq} - u_q - \omega(0.5L + L_T) i_d \end{cases} \quad (2)$$

Under unbalanced grid voltage conditions, the active and reactive power inputs at the connecting point between the converter and grid are depicted as [4] and [21].

$$\begin{cases} P = P_0 + P_c \cos 2\omega t + P_s \sin(2\omega t + \theta) \\ Q = Q_0 + Q_c \cos 2\omega t + Q_s \sin(2\omega t + \varphi) \end{cases} \quad (3)$$

The constant active P_0 and reactive powers Q_0 and the power fluctuations P_c , P_s , Q_c , and Q_s can be obtained with Equations (4) to (6), where U_{sdq+} and U_{sdq-} are the positive and negative sequence voltages, respectively, and I_{dq+} and I_{dq-} are the positive and negative sequence currents, respectively [4].

$$\begin{cases} P_0 = U_{sd+} I_{d+} + U_{sq+} I_{q+} + U_{sd-} I_{d-} + U_{sq-} I_{q-} \\ Q_0 = U_{sd+} I_{q+} + U_{sq+} I_{d+} + U_{sd-} I_{q-} + U_{sq-} I_{d-} \end{cases} \quad (4)$$

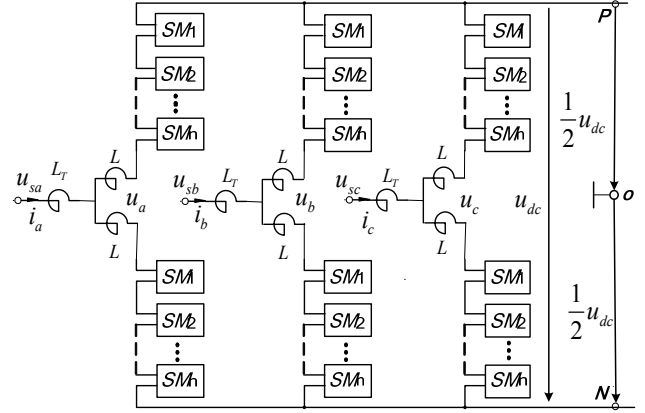


Fig. 1. General circuit structure of MMC.

$$\begin{cases} P_c = U_{sd+} I_{d-} + U_{sq+} I_{q-} + U_{sd-} I_{d+} + U_{sq-} I_{q+} \\ P_s = U_{sd+} I_{q-} - U_{sq+} I_{d-} - U_{sd-} I_{q+} + U_{sq-} I_{d+} \end{cases} \quad (5)$$

$$\begin{cases} Q_c = -U_{sd+} I_{q-} + U_{sq+} I_{d-} - U_{sd-} I_{q+} + U_{sq-} I_{d+} \\ Q_s = U_{sd+} I_{d-} + U_{sq+} I_{q-} - U_{sd-} I_{d+} + U_{sq-} I_{q+} \end{cases} \quad (6)$$

Compared with the balanced grid condition, the active and reactive powers in unbalanced grid condition fluctuate because of the cross products between the negative and positive sequences. Moreover, the fault current may significantly grow, causing an overcurrent problem. As such, proper control strategies for improving the system fault through ability should be developed.

III. CONTROL SCHEME ANALYSIS AND DESIGN

Two different power control strategies are normally used for conventional converters under unbalanced conditions [22]. One strategy is adopted to eliminate the negative sequence current components and keep the AC currents balanced. The other approach is used to eliminate the active power double-base frequency ripples. To implement these control strategies, a current reference calculation method, an efficient current controller, and a sequence extraction system should be developed.

A. Current Reference Calculation

The first control strategy for controlling the negative sequence current is designed to lessen the power oscillation and overcurrent level. According to [4] and [5], this approach can be realized by setting $I_{d-} = 0$, $I_{q-} = 0$ in Equation (4) as follows:

$$\begin{cases} I_{d+}^* = P^* \frac{U_{sd+}}{U_{sd+}^2 + U_{sq+}^2} - Q^* \frac{U_{sq+}}{U_{sd+}^2 + U_{sq+}^2} \\ I_{q+}^* = P^* \frac{U_{sq+}}{U_{sd+}^2 + U_{sq+}^2} + Q^* \frac{U_{sd+}}{U_{sd+}^2 + U_{sq+}^2} \end{cases} \quad (7)$$

Another control strategy is designed to minimize the three-phase active power oscillations and keep the active power input to the AC grid constant. [4] and [5] posited that by setting P_c and P_s in (5) as zero, the four current references

can be calculated with the following equations:

$$\begin{cases} I_{d+}^* = P^* U_{sd+} / K_1 + Q^* U_{sq+} / K_2 \\ I_{q+}^* = P^* U_{sq+} / K_1 - Q^* U_{sd+} / K_2 \\ I_{d-}^* = -P^* U_{sd-} / K_1 + Q^* U_{sq-} / K_2 \\ I_{q-}^* = -P^* U_{sq-} / K_1 - Q^* U_{sd-} / K_2 \end{cases} \quad (8)$$

$$\begin{cases} K_1 = (U_{sd+}^2 + U_{sq+}^2) - (U_{sd-}^2 + U_{sq-}^2) \\ K_2 = (U_{sd+}^2 + U_{sq+}^2) + (U_{sd-}^2 + U_{sq-}^2) \end{cases} \quad (9)$$

The preceding analysis suggests that the current reference is related to the transmitted P and Q. When the grid faults are serious (e.g., metallic short) and when P and Q remain unchanged during the fault period, the overcurrent problem occurs according to (7) and (8). In this case, VDCOL should be considered to adjust the transmitted power.

The overcurrent factor is defined as

$$\lambda = I^* / I_N^*$$

k depicts the amplitude of the positive and rated voltages.

$$k = \sqrt{(U_{sd+}^2 + U_{sq+}^2) / (U_{sd+}^2 + U_{sq+}^2)}$$

The current reference can be calculated with (10) for control strategy 1 (Q^* is set as zero to transmit several active powers).

$$\begin{cases} I_N^* = \sqrt{(I_{d+}^*)^2 + (I_{q+}^*)^2} = P^* / \sqrt{U_{sd+}^2 + U_{sq+}^2} \\ I^* = \sqrt{(I_{d+}^*)^2 + (I_{q+}^*)^2} = P^* / (k \sqrt{U_{sd+}^2 + U_{sq+}^2}) \end{cases} \quad (10)$$

P_{ocl}^* , which is the modified active power reference when the overcurrent problem occurs, is expressed as follows:

$$\begin{cases} P_{ocl}^* = P^* & k \geq 1/\lambda \\ P_{ocl}^* = kP^* & k < 1/\lambda \end{cases} \quad (11)$$

For control strategy 2, η is defined as

$$\eta = \sqrt{(U_{sd-}^2 + U_{sq-}^2) / (U_{sd+}^2 + U_{sq+}^2)} \quad (12)$$

The amplitude of the positive and negative sequence currents can be expressed as

$$\begin{cases} I_+^* = \sqrt{(I_{d+}^*)^2 + (I_{q+}^*)^2} = \frac{1}{(1-\eta^2)k} \frac{P^*}{\sqrt{U_{sd+}^2 + U_{sq+}^2}} \\ I_-^* = \sqrt{(I_{d-}^*)^2 + (I_{q-}^*)^2} = \frac{\eta}{(1-\eta^2)k} \frac{P^*}{\sqrt{U_{sd+}^2 + U_{sq+}^2}} \end{cases} \quad (13)$$

The current can be expressed as (14) with respect to the same frequency characteristic between the positive and negative sequence currents.

$$i^* = i_+^* + i_-^* = I_+^* \angle 0^\circ + I_-^* \angle \varphi \quad (14)$$

The mode value I^* is expressed as

$$I^* = \sqrt{(I_+^*)^2 + (I_-^*)^2} + 2I_+^* I_-^* \cos \varphi \leq I_+^* + I_-^* \quad (15)$$

According to (13), the above equation can be rewritten as follows:

$$I^* \leq \frac{1}{(1-\eta^2)k} \frac{P^*}{\sqrt{U_{sd+}^2 + U_{sq+}^2}} \quad (16)$$

P_{ocl}^* is defined as

$$\begin{cases} P_{ocl}^* = P^* & (1-\eta)k \geq 1/\lambda \\ P_{ocl}^* = \lambda P^* (1-\eta)k & (1-\eta)k < 1/\lambda \end{cases} \quad (17)$$

The above analysis indicates that the transmitted active power can be adjusted automatically, and the maximum current amplitude is limited to a certain value with (11) and (17).

B. Sequence Extraction and Synchronization

The effective operation of MMC under unbalanced grid voltages requires an accurate grid voltage sequence extraction method to calculate the current reference as mentioned in Section IIIA. The delayed signal cancellation method is an effective detection method both for steady state and transient performance [23], [24]. The positive and negative sequence components of grid voltages in $\alpha\beta$ reference frame can be expressed as (18), where T is the period of the base frequency.

$$\begin{cases} u_{s\alpha+} = 0.5(u_{s\alpha} - u_{s\beta} e^{-s0.25T}) \\ u_{\beta+} = 0.5(u_{s\beta} + u_{s\alpha} e^{-s0.25T}) \\ u_{s\alpha-} = 0.5(u_{s\alpha} + u_{s\beta} e^{-s0.25T}) \\ u_{s\beta-} = 0.5(u_{s\beta} - u_{s\alpha} e^{-s0.25T}) \end{cases} \quad (18)$$

The sequence components u_{sdq+} and u_{sdq-} can be calculated with (19).

$$\begin{bmatrix} u_{sd\pm} \\ u_{sq\pm} \end{bmatrix} = \begin{bmatrix} u_{s\alpha\pm} \cos \theta_{\pm} & u_{s\beta\pm} \sin \theta_{\pm} \\ -u_{s\alpha\pm} \sin \theta_{\pm} & u_{s\beta\pm} \cos \theta_{\pm} \end{bmatrix} \quad (19)$$

Given that the voltages are in the same phase and are orthogonal to the voltage of phase A, the voltage in the $\alpha\beta$ reference frame is directly used to calculate the phase angle in (19) to avoid the error caused by the PLL [23].

$$\begin{bmatrix} \theta_+ \\ \theta_- \end{bmatrix} = \begin{bmatrix} \pi \pm \arctg(u_{s\beta+} / u_{s\alpha+}) \\ \pi \pm \arctg(u_{s\beta-} / u_{s\alpha-}) \end{bmatrix} \quad (20)$$

C. Proportional Integer Plus Resonant Controller

Accurately controlling the positive and negative sequence currents is crucial for the current controller because DC and double-base frequency AC current components exist in the positive synchronous rotational reference frame. The current controller should provide an extremely high gain both at the zero and double-base frequencies to track the hybrid current with a zero static error.

The proportional integral control can control the DC current, but it inefficiently suppresses the AC current. By contrast, the resonant controller with an infinite gain at a specific frequency can achieve a zero steady status error in tracking AC signals. Thus, this study uses a hybrid current vector controller based on the proportional integer plus resonant scheme, which directly regulates all currents, including the DC and negative sequence components with double-base frequency, in the positive synchronous rotational

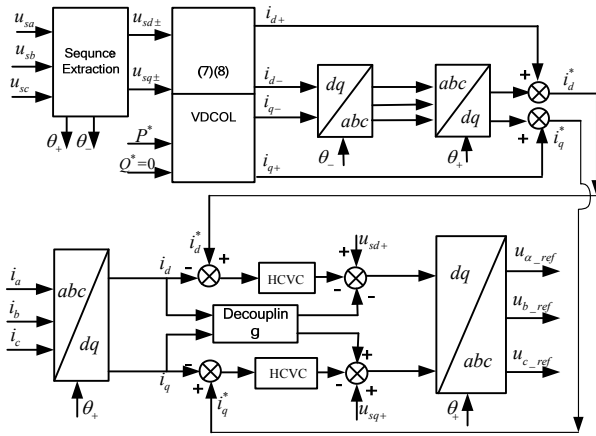


Fig. 2. Control block diagram based on HCVC.

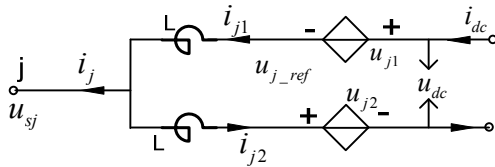


Fig. 3. Single arm equivalent circuit of phase J.

reference frame.

The transfer function of HCVC is expressed as (21) with feathurs $G_{PIR}(0) = \infty$ and $G_{PIR}(\omega_0) \approx K_R$, where K_p is the proportional coefficient, K_R is the resonant coefficient, and ω_0 is the resonant frequency.

$$G_{PIR}(S) = K_p + K_I \frac{1}{S} + \frac{2K_R S \omega_c}{S^2 + \omega_0^2 + 2\omega_c S} \quad (21)$$

The whole control scheme is illustrated in Fig. 2.

IV. MODULATION AND CIRCULATING CURRENT

A. Modulation Method

The modulation methods used in multilevel converters can be classified as pulse width and staircase modulation methods at high and low switching frequencies, respectively [25]. As a representative method of staircase modulation, the nearest level modulation (NLM) is used in this study because of its simple principle and convenient realization [26].

In Fig. 3, u_{j1} and u_{j2} are the output voltages of the upper and down arm SMs of phase J, respectively, and u_{j_ref} is the instantaneous modulation reference waveform.

The voltage relationship of phase J in Fig. 3 is given by

$$\begin{cases} u_{j1} = 0.5u_{dc} - u_{j_ref} \\ u_{j2} = 0.5u_{dc} + u_{j_ref} \end{cases} \quad (22)$$

The upper and down arm SM numbers (i.e., n and m) switched at the on status of phase J can be calculated with (23), where $\text{Round}[x]$ is the nearest integer function of x , and u_c is the rated capacitor voltage [25].

$$\begin{cases} n = \text{Round}[u_{j1}/u_c] \\ m = \text{Round}[u_{j2}/u_c] \end{cases} \quad (23)$$

B. Circulating Current Analysis

The voltage fluctuations of SM capacitor and the working mechanism of MMC may cause circulating currents to flow through arms. These currents may distort the sinusoidal arm current and increase the rated current of power devices. The circulating current components and their characters under unbalanced grid voltages are analyzed in the succeeding paragraphs.

The upper u_{jp} and down u_{jn} arm voltages are defined as follows:

$$\begin{cases} u_{jp} = \sum_{k=1}^n u_{j1_c_k} + L \frac{di_{j1}}{dt} \\ u_{jn} = \sum_{k=1}^m u_{j2_c_k} + L \frac{di_{j2}}{dt} \end{cases} \quad (24)$$

The k capacitor voltage at t is expressed below.

$$\begin{cases} u_{j1_c_k}(t) = u_{j1_c_k}(t_0) + 1/C \int_{t_0}^t i_{j1} d\tau \\ u_{j2_c_k}(t) = u_{j2_c_k}(t_0) + 1/C \int_{t_0}^t i_{j2} d\tau \end{cases} \quad (25)$$

Equation (26) can be obtained according to Fig. 3.

$$\begin{aligned} U_{j1} + U_{j2} + \sum_{k=1}^n \frac{1}{C} \int_{t_0}^t i_{j1} d\tau + \sum_{k=1}^m \frac{1}{C} \int_{t_0}^t i_{j2} d\tau \\ + L \frac{di_{j1}}{dt} + L \frac{di_{j2}}{dt} = U_{dc} \end{aligned} \quad (26)$$

where U_{j1} and U_{j2} are denoted as follows:

$$U_{j1} = \sum_{k=1}^n u_{j1_c_k}(t_0) \quad U_{j2} = \sum_{k=1}^m u_{j2_c_k}(t_0)$$

According to the relationship $i_j = i_{j1} - i_{j2}$, $n+m = N$, Equation (26) can be rewritten as below.

$$U_{dc} = U_{j1} + U_{j2} + \frac{N}{C} \int_{t_0}^t i_{j1} d\tau - \frac{m}{C} \int_{t_0}^t i_{j2} d\tau + 2L \frac{di_{j1}}{dt} - L \frac{di_{j2}}{dt} \quad (27)$$

The following expression is assumed:

$$\begin{cases} u_{j_ref} = U_{m+} \sin(\omega t + \theta_{j+}) + U_{m-} \sin(\omega t + \theta_{j-}) \\ i_j = I_{m+} \sin(\omega t + \Phi_{j+}) + I_{m-} \sin(\omega t + \Phi_{j-}) \end{cases}$$

Correspondingly, m is expressed as

$$\begin{aligned} m &= (0.5 U_{dc} + u_{j_ref}) / (U_{dc}/N) \\ &= 0.5N + N\lambda_+ \sin(\omega t + \theta_{j+}) + N\lambda_- \sin(\omega t + \theta_{j-}) \end{aligned} \quad (28)$$

where $\lambda_+ = U_{m+}/U_{dc}$, and $\lambda_- = U_{m-}/U_{dc}$.

Substituting m into (27) and derivation, the upper and down arm currents can be identified with the below equations.

$$\begin{cases} i_{j1} \approx 0.5i_j + i_{j_dc} - i_{j_circle} \\ i_{j2} \approx -0.5i_j + i_{j_dc} - i_{j_circle} \end{cases} \quad (29)$$

The DC component i_{j_dc} is given as (30).

$$\begin{aligned} i_{j_dc} &= \lambda_+ I_{m+} \cos(\Phi_{j+} - \theta_{j+}) + \lambda_- I_{m-} \cos(\Phi_{j-} - \theta_{j+}) \\ &\quad + \lambda_- I_{m+} \cos(\Phi_{j+} - \theta_{j-}) + \lambda_- I_{m-} \cos(\Phi_{j-} - \theta_{j-}) \end{aligned} \quad (30)$$

The circulating current sequence components in (31) are expressed as in (32).

$$i_{j_circle} = i_{j_circle+} + i_{j_circle-} + i_{j_circle0} \quad (31)$$

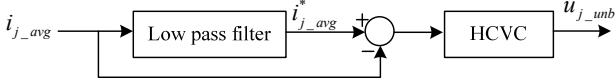


Fig. 4. Circulating current controlling scheme.

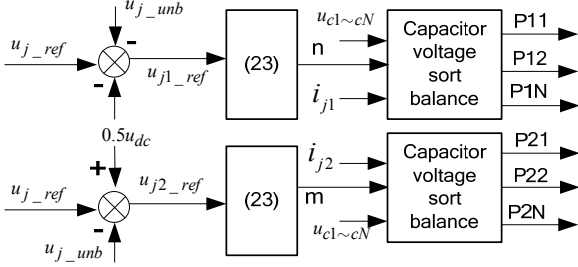


Fig. 5. Trigger pulse generation scheme based on NLM.

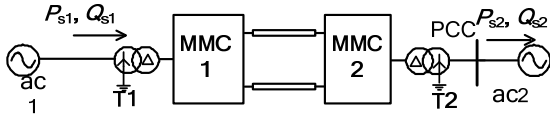


Fig. 6. Two simulation terminal models of MMC-HVDC

$$\begin{cases} i_{j_circle+} = \lambda_- I_{m-} \cos(2\omega t + \Phi_{j-} - \theta_{j-}) \\ i_{j_circle-} = \lambda_+ I_{m+} \cos(2\omega t + \Phi_{j+} - \theta_{j+}) \\ i_{j_circle0} = \lambda_+ I_{m-} \cos(2\omega t + \Phi_{j-} - \theta_{j+}) + \\ \quad \lambda_- I_{m+} \cos(2\omega t + \Phi_{j+} - \theta_{j-}) \end{cases} \quad (32)$$

The circulating current can be decomposed into positive, negative, and zero sequence components with 100 Hz under unbalanced grid voltages. Adding i_{j1} and i_{j2} to (29), the average arm current (i_{j_avg}) is depicted in (33). Given that DC component and circulating current with double-base frequency exist in the average arm current, the HCVC in the three-phase static frames is used to suppress all the circulating current components.

$$i_{j_avg} = 0.5(i_{j1} + i_{j2}) = i_{j_dc} - i_{j_circle} \quad (33)$$

A circulating current controller with HCVC ($\omega_0 = 200 \pi$) is designed as shown in the below figure.

Equation (22) is rewritten as (34). Fig. 5 illustrates the trigger pulse generation scheme based on NLM.

$$\begin{cases} u_{j1} = 0.5U_{dc} - u_{j_ref} - u_{j_unb} \\ u_{j2} = 0.5U_{dc} + u_{j_ref} - u_{j_unb} \end{cases} \quad (34)$$

V. STUDY RESULTS

The proposed control scheme of MMC-HVDC presented in Fig. 6 is simulated in the time domain PSCAD/EMTDC environment. MMC1 controls the DC bus voltage and reactive power input to the converter, whereas MMC2 regulates the active and reactive power inputs to the converter. A 21-level MMC is adopted to reduce the simulation times. Table I lists the main circuit parameters.

TABLE I
MAIN CIRCUIT PARAMETERS

Items	Value
Rated DC voltage	+/-200 kV
Rated active power	400 MW
AC system source voltage	210 kV
AC system source frequency	50 Hz
Transformer ratio	210 kV/220 kV
Transformer leakage inductance	0.1 pu
Number of SM per arm	20
SM capacitor C_0	3000 μ F
Arm inductance L_0	0.1 pu
SM capacitor voltage	20 kV
Length of DC cable	100 km

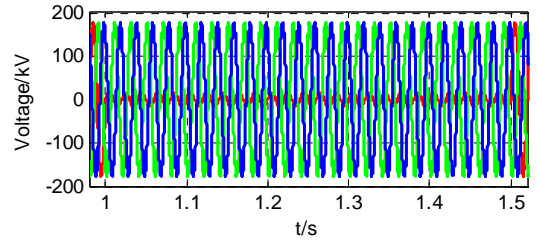


Fig. 7. Waveform of grid voltage under SLG fault.

A single line-to-ground fault (SLG) is the most possible fault to occur in the AC grid. Therefore, SLG is taken as an example in this study to verify the proposed strategies. The SLG fault depicted in Fig. 7 occurs at 1.0 s and is imposed on PCC, which lasts for 500 ms. The control strategy is enabled after 0.05 s, while the circulating current control is began at 1.2 s to show its control effect.

The DC bus voltage should be kept constant to guarantee the proper operation of the system. If MMC1 fails, then the control strategy of MMC2 should be switched to control the DC bus voltage. In this case, MMC1 controls the power. Correspondingly, all subsequent simulations are conducted in the MMC2 side.

A. Power Control under Balanced Conditions

To verify the steady state tracking performance of the proposed control scheme, the active and reactive power references are regulated according to the mechanisms described in the subsequent paragraphs.

The reactive power command ramps from 100 Mvar to -100 Mvar at 3 s, from -100 Mvar to 100 Mvar at 5 s, and decreases from 100 Mvar to 0 Mvar at 7s. The active power command is step changed from 400 MW to 200 WM at 4 s and is then reversed from 200 MW to -400 WM at 6 s. Both HCVC and DCVC controls are conducted to compare their control performance. Fig. 8 shows the dynamic response of the system to these power reference changes.

Figs. 8(a) and (b) show that the output active and reactive powers of MMC2 can quickly meet the active and reactive

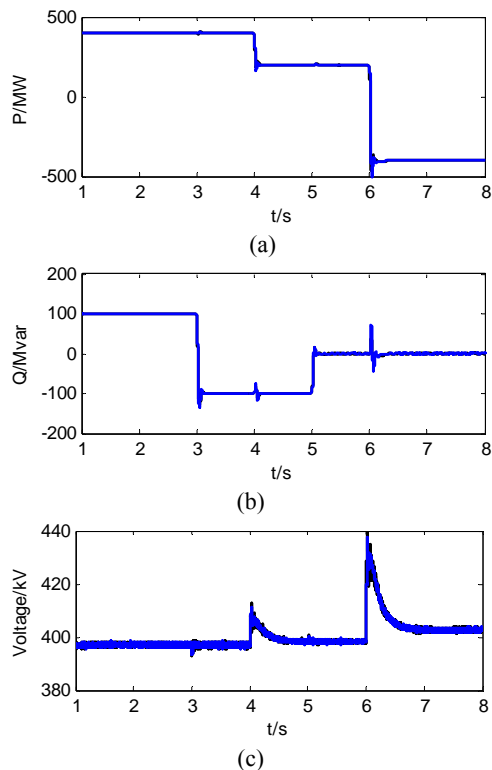


Fig. 8. Instruction tracking performance of MMC2. (a) Active power. (b) Reactive power. (c) DC bus voltage.

power references. Fig. 8(c) shows the DC bus voltage response. In particular, this voltage is observed to be well regulated after the disturbances.

As demonstrated in Figs. 8(a) to (c), the DC bus voltage increases gradually because the instant active power is decreased from 400 MW to 200 MW and is then inverted from 200 MW to -400 MW. This occurrence causes the unbalance between the input and output active powers. Thus, the redundant energy is absorbed and stored by the SM capacitors. The DC bus voltage decreases gradually to the rated value under the DC voltage control.

These simulation results indicate that both HCVC and DVCC control schemes show almost the same performance in independently tracking the active and reactive power references because double-base frequency current component does not exist.

B. Control the Negative Sequence Current

When the strategy for controlling the negative sequence current is used, the corresponding components in AC current decrease to zero. The AC currents in Fig. 6 are balanced during the SLG fault as shown in Fig. 9(a). The active power command remains constant; hence, the AC currents become higher than the rated value. Moreover, ripples emerge in the active and reactive powers during the fault period (Fig. 9(b)) because the negative sequence voltage remains. The SM capacitor voltages of the upper arm of phase A are illustrated in Fig. 9(c), which shows that the capacitor voltage ripples

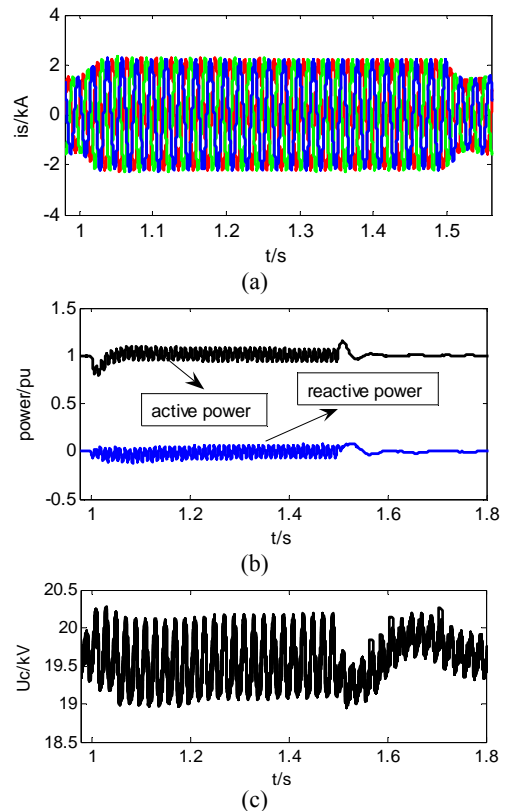


Fig. 9. Waveforms of controlling the negative sequence current. (a) Three-phase grid current. (b) Active and reactive powers. (c) Capacitor voltage of phase A.

increase under unbalanced conditions.

Fig. 10 demonstrates that HCVC and DCVC can both effectively control the negative sequence current, but some differences are observed between them. HCVC can control both the DC and AC current sequence components, but PI can only control the DC current. As such, the control effect of HCVC is better than that of DCVC before the negative current control is enabled. Moreover, HCVC can smoothly control the clearing period during fault even without the switching control scheme.

C. Control Active Power Ripples

In this case, control strategy 2 (without VDCOL) is first simulated.

As shown in Fig. 11(b), the three-phase active power ripples are eliminated, whereas the reactive power ripples remain according to (6) during fault. The amplitude of arm currents is increased because of the effects of the unchanged power reference and negative sequence current. In the phase A current, the current amplitudes in Fig. 11(a) are larger than those in Fig. 9(a). This condition implies the occurrence of a severe overcurrent problem, which may damage the electric devices if the fault lasts long.

The following simulation is conducted with VDCOL. The active power command is adjusted automatically to less over the current degree. The output active power is reduced from 1

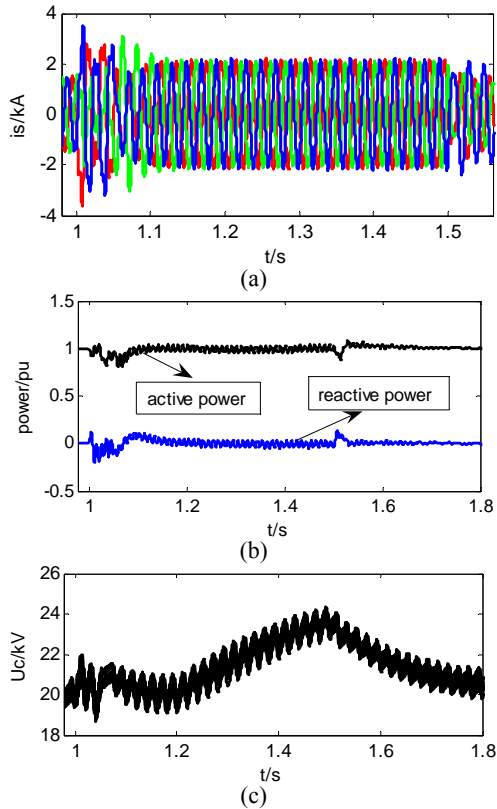


Fig. 10. Waveforms of controlling the negative sequence current. (a) Three-phase grid current. (b) Active and reactive powers. (c) Capacitor voltage of phase A.

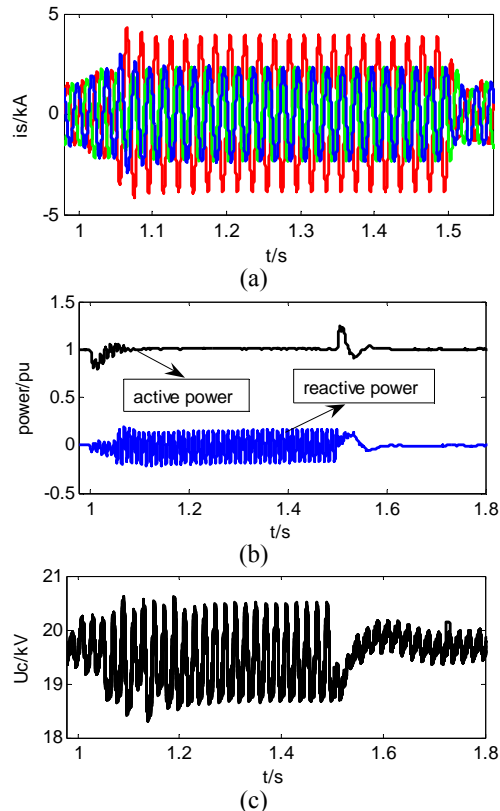


Fig. 11. Waveform of controlling the active power ripples without VDCOL. (a) Three-phase grid currents. (b) Active and reactive powers. (c) Capacitor voltage of phase A.

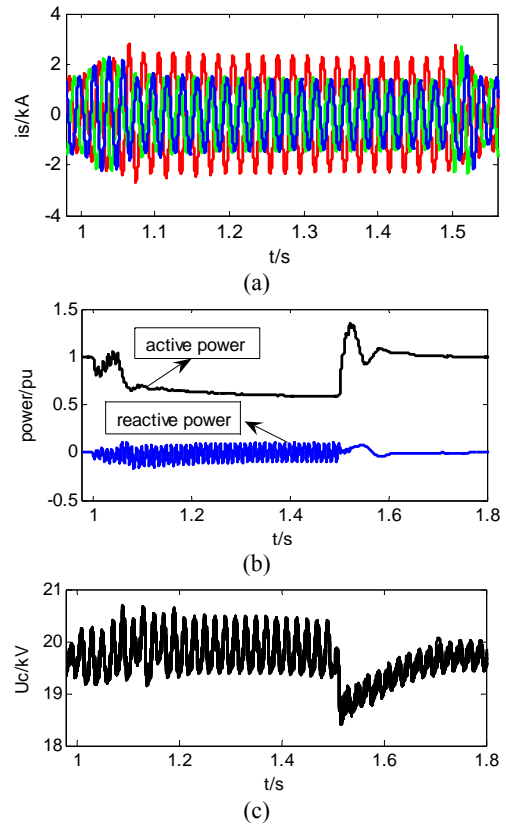


Fig. 12. Waveform of controlling the active power ripples with VDCOL. (a) Three-phase grid currents. (b) Three-phase active and reactive powers. (c) Capacitor voltage of phase A.

pu to 0.6 pu during fault as shown in Fig. 12(b). Similarly, the current amplitude of phase A in Fig. 12(a) is decreased from 4 kA to 2.3 kA ($\lambda = 1.5$, compared with Fig. 11(a)).

Fig. 13 shows that similar to HCVC, DCVC can also efficiently suppress the active power ripples. However, for the same reason as the negative sequence current control, the controlling smoothness of DCVC is relatively less compared with that of HCVC. In addition, the current waveforms of DCVC vary from those of HCVC during the fault period because different inner loop current controllers are used.

D. Control Circulating Current

As depicted in Fig. 14, the circulating current is suppressed. However, the three-phase arm average currents illustrated in this figure vary from one another during the fault period because the three-phase AC active power is unbalanced under the negative sequence current control. By contrast, for the active power control strategy, the three-phase arm average currents shown in Fig. 14(b) are almost identical with one another unlike those depicted in Fig. 14(a) because the three-phase AC active power is approximately balanced under this condition.

The succeeding figures demonstrate the simulating results of DCVC with the PI circulating current controller. The three-phase arm average currents of DCVC show the same trends as HCVC, but its control effect varies from that of

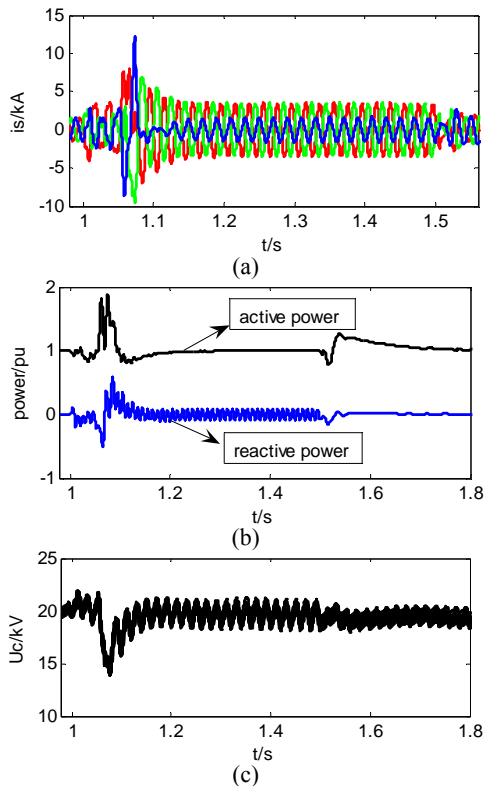


Fig. 13. Waveform of controlling the active power ripples. (a) Three-phase grid current. (b) Active and reactive powers. (c) Capacitor voltage of phase A.

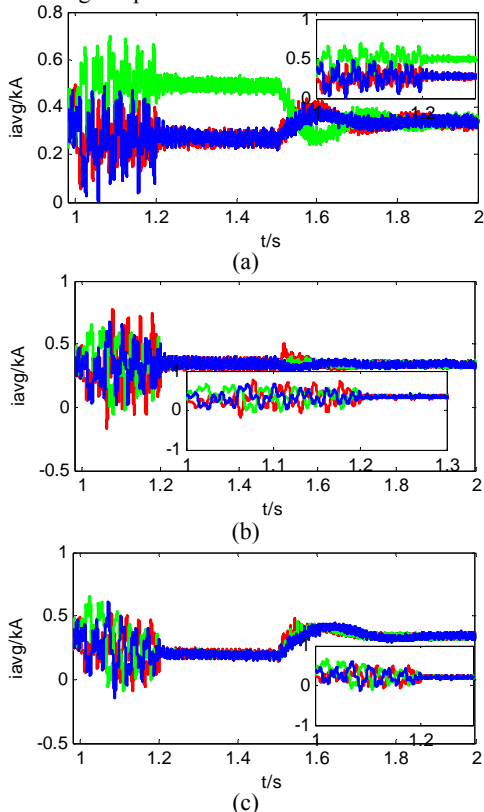


Fig. 14. Three-phase arm average current of HCVC under the (a) control negative sequence current. (b) control active power ripples without VDCOL, (c) control active power ripples with VDCOL.

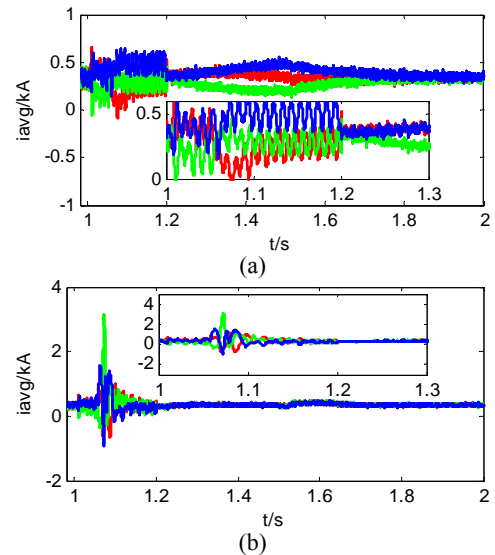


Fig. 15. Three-phase arm average current of DCVC under the (a) control negative sequence current, (b) control active power ripples.

HCVC because zero and positive sequence circulating currents exist when the unbalanced power grid failure occurs.

VI. CONCLUSIONS

Under a synchronous rotational reference frame, this study analyzes the mathematical model of the MMC-HVDC system and uses a hybrid current vector controller to uniformly control the negative and positive sequence currents under unbalanced grid voltage conditions. Correspondingly, the control complex problem and current sequence extraction procedure of DCVC are addressed. The arm circulating current sequence components are also analyzed from a different point of view. A CCSC is designed based on HCVC to control all these sequence components. The schemes under study are conducted in PSCAD/EMTDC to examine their respective performances. The simulating results show that the HCVC of MMC-HVDC provides the desired dynamic response under balanced and unbalanced grid conditions.

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