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High Efficiency High-Step-up Single-ended DC–DC Converter with Small Output Voltage Ripple

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Abstract

Renewable energy resources such as wind and photovoltaic power generation systems demand a high step-up DC–DC converters to convert the low voltage to commercial grid voltage. However, the high step-up converter using a transformer has limitations of high voltage stresses of switches and diodes when the transformer winding ratio increases. Accordingly, conventional studies have been applied to series-connect multioutput converters such as forward–flyback and switched-capacitor flyback to reduce the transformer winding ratio. This paper proposes new single-ended converter topologies of an isolation type and a non-isolation type to improve power efficiency, cost-effectiveness, and output ripple. The first proposal is an isolation-type charge-pump switched-capacitor flyback converter that includes an extreme-ratio isolation switched-capacitor cell with a charge-pump circuit. It reduces the transformer winding number and the output ripple, and further improves power efficiency without any cost increase. The next proposal is a non-isolation charge-pump switched-capacitor-flyback tapped-inductor boost converter, which adds a charge-pump-connected flyback circuit to the conventional switched-capacitor boost converter to improve the power efficiency and to reduce the efficiency degradation from the input variation. In this paper, the operation principle of the proposed scheme is presented with the experimental results of the 100 W DC–DC converter for verification.

Key words: High step-up, Isolated switched-capacitor cell, Output ripple, Single ended, Tapped inductor

I. INTRODUCTION

PV power generation technology, which typically has a low-voltage high-current characteristic, attracts great attention as a next-generation energy source. The PV power control unit, however, basically demands a high-step-up DC–DC converter to interface with other electrical networks. Hence, various types of conventional high-step-up converter topologies have been proposed for low-voltage power sources [1]. Switched-capacitor or charge-pump circuits are generally used in the high-step-up applications. In a previous article, a conventional switched-capacitor series-connected flyback converter or a switched-capacitor coupled-inductor boost converter has successfully achieved an efficiency breakthrough even under a wide input voltage variations. The coupled-inductor method is a voltage-enhancement technique that uses core-sharing magnetic devices that integrate the functions of auto-transformers and inductors [2]. Several improved version of high step-up converters with a coupled-inductor have also been introduced by adding a charge pump or a switched-capacitor cell because a flyback converter employing a coupled inductor is an isolation version of the low-efficiency buck-boost converter, as shown in Fig. 1(a) [3]. The voltage multiplier method is another enhancement technique using high-voltage capacitors and diodes [4]-[9]. With the help of the charge-pump switched capacitor inserted between the primary side and the secondary side of the coupled-inductor, the boost ratio was largely increased, whereas the rectifier-diode voltage stress was reduced closer to the output voltage. This method has a simple hardware; however, the output voltage of this method has discrete levels because of the absence of voltage regulation capability [10]-[16]. Moreover, the charge-pump cell has a limitation of voltage enhancement, i.e., double or triple. Therefore, multistage structures should be used in spite of the efficiency reduction.

Previous studies on the application of these engineering techniques to high-step-up converter topologies, particularly for low-voltage power sources, have reported some limitations. A previous article [17] mentioned that in a clamp-mode couple-inductor buck–boost converter [18], the output

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diode stress was similar to that of a traditional flyback converter, i.e., the output diode stress was higher than the output voltage, even with recycling the leakage energy of the coupled inductor. Further improvements were accomplished by combining a boost converter with a flyback converter [19], [20]. Compared with the converter in [18], the series combination of outputs of the boost and flyback converters improves the step-up ratio. Nevertheless, a problem still existed in [18]. By adding a switched capacitor in series with the transformer, a new high-ratio DC–DC converter with coupled inductor and switched capacitor was introduced in [21]. With the switched capacitor between the primary side and the secondary side of the coupled inductor, the boost ratio increases, and the output diode voltage stress was reduced. However, the magnetic core is not fully utilized because the operation does not include a transformer (on-time transfer) mode, but an inductor (off-time transfer) mode. A further-improved version is presented in [17]. This version combines pulse-width modulation (PWD) and resonant power conversions to increase the total power and to decrease the losses through a simultaneous energy transfer in an auxiliary inductor and a charge-pump capacitor. However, this version needs more devices for energy transfer [22]. Therefore, design complexity and cost can still be improved.

To handle these problems, a conventionally proposed switched-capacitor circuit that includes a transformer is introduced, as shown in Fig. 1(b) [22]. The circuit diagram of the proposed cell is similar to that of the conventional flyback converter, as shown in Fig. 1(a). However, the dot of transformer is the other side, which decides the operation principle critically [23]. The circuit has a very high step-up ratio, as well as isolation capability, through the use of a high turn ratio of the transformer. With the assumption that the transformer is ideal, the operating performance is extremely similar to the conventional switched capacitors. Therefore, the proposed cell was named the "*isolated switched-capacitor cell"* [22]. The secondary current flows directly to the load during the switch-on time, which helps the high efficiency, compared with the conventional forward-flyback topology [24]. The secondary winding coil of the transformer certainly has a parasitic resistance, which restricts the in-rush of the short current.

Then, the step-up ratio of the proposed cell is as follows:

$$V_o = \frac{N_s}{N_p} V_{in} \quad (1)$$

where V_o is the output voltage, V_{in} is the input voltage, N_s is the primary turn ratio of the transformer, and N_p is the secondary turn ratio. The step-up ratio is independent of the magnetizing inductance of the transformer [22].

The cell can be extended further by an auxiliary circuit such as a charge pump for a high step up. Fig. 2 shows a newly proposed charge-pump switched-capacitor cell that facilitates a charge-pump circuit with the transformer-type switched-capacitor cell.

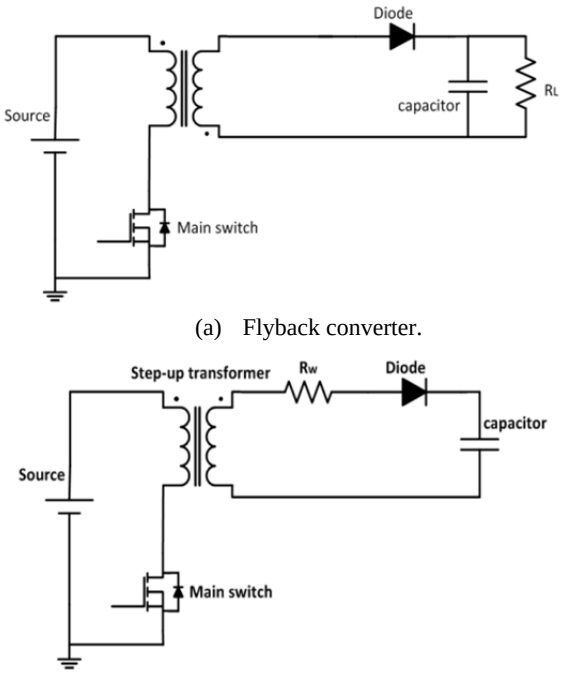


Fig. 1. Comparison between a couple-inductor converter and a transformer-type switched-capacitor one.

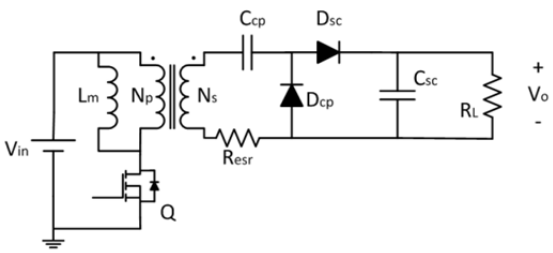


Fig. 2. Proposed single-ended isolated charge-pump switched-capacitor cell: note the dot pair. The cell is not a flyback.

The step-up ratio of the proposed cell is as follows:

$$V_o = \frac{N_s}{N_p} V_{in} + V_{C\_cp} \quad (2)$$

where V_{C_cp} is the voltage of the charge pump, which has the same boost ratio as the flyback converter.

The converter is cost effective because of the single switch and single magnetic device; however, the charge-pump cascaded single-output structure of the proposed cell requires a high-voltage rating devices for high-step-up applications because of the high-voltage stresses. In addition, the output capacitor should be of high voltage and large capacitance.

This paper proposes new converter topologies of both isolation type and non-isolation type that allow high step-up with a low turn-on ratio and small output ripple using a series connection of the outputs. With the magnetically coupling idea of the charge-pump switched-capacitor cell, flyback and tapped-inductor boost converters, which integrate each of the magnetic energy transfer modes together in alternatively driving method, are introduced in the proposed high boost-ratio DC–DC converter. In the high step-up topologies

connecting the outputs serially, the entire output voltage ripple is reduced through phase differences of the charging or discharging time between the upper and lower capacitances. For example, if the charge-pump switched-capacitor cell and the flyback converter are separated in charging and discharging time, i.e., the charge-pump switched-capacitor cell charges the output capacitor in switch on-time, and the flyback converter charges the output capacitor in switch-off time, then the total output ripple is made smaller through connecting the outputs in a series with each one of the converters. The reduction in alternatively driving can be called an "interleaving" technique, even though it is not an exact 180° shift [10].

Not only the cost reduction from the magnetic device integration, but also the continuous energy transfer during the switch-on and -off in every switching cycle can increase the total power delivery by reducing the losses in the circuit. The conduction losses in the primary side of the transformer are also remarkably reduced because of the reduced input-current RMS value through the primary side. The superposition of the magnetizing and the switched-capacitor transferred current makes the primary current to slightly fluctuate. In addition, the proposed scheme decreases the voltage rating of the main switch or the diodes by correctly adjusting the turn ratio of the transformer, as well as by expanding the design criteria for part selection. In terms of extra advantages of the novel converter, the single-ended circuit system is comparatively simple and cost effective, and its efficiency is extremely high with a low turn-on ratio. The controller design will be interesting, being closely associated with the PV generator dynamic responses [25]; hence, it will be considered for future study.

The remainder of this study is organized as follows. Section II presents the proposal of a new isolated CSFB converter and operating analysis of the proposed converter. Section III presents the power loss analysis of CSFB converter and design guideline. In addition, section IV presents the proposal of a non-isolated CSFB tapped-inductor (CSFTI) boost converter and operating analysis of the proposed converter. Section V presents the power loss analysis of the CSFTI converter and the design guideline. In Section VI, the experimental results of the 100-W hardware prototype as a pre-regulating stage of the multistage photovoltaic power conditioning systems are given for topologies verification. Finally, a conclusions are presented in Section VII.

II. Isolated DC–DC Converter Using Charge-Pump Switched-Capacitor Cell

A. Structure of the Proposed CSFB Converter

The structure of the proposed isolated DC-DC converter is shown in Fig. 3. The primary has PWM voltages generated by a single main switch. The secondary has the isolated charge-pump switched-capacitor and flyback. Both of the outputs are serially connected to boost the output voltage.

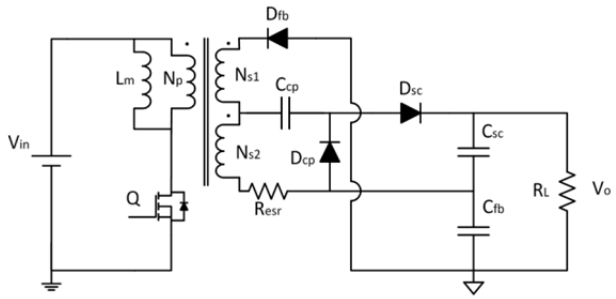


Fig. 3. Proposed isolated CSFB converter.

The proposed converter makes effective utilization of the transformer because power is delivered during both switch-on and -off time. Furthermore, the output ripple is reduced through the phase difference between charging and discharging of the output capacitors.

B. CCM Transfer Gain of a CSFB Converter

To analyze the steady-state gain, the charge-pump switched capacitor and flyback converter can be analyzed using an equivalent circuit transformation, as shown in Fig. 4 [24]. Both of the output currents (I_{O_sc} and I_{O_fb}) are the same as load current I_{Load} because of the series connection. The following equations indicate each of the load resistances for the equivalent transformation:

$$R_{sc} = \frac{V_{sc}}{I_{Load}} \quad \text{and} \quad R_{fb} = \frac{V_{fb}}{I_{Load}} \tag{3}$$

where V_{sc} is the switched capacitor output, and V_{fb} is the flyback output.

As aforementioned, the steady-state voltage gain of the isolated switched capacitor cell is only determined by the turn ratio of the transformer winding. Meanwhile, the charge-pump voltage is equal to the flyback converters. Thus, the voltage gain of the charge-pump switched-capacitor cell is as follows:

$$M_{VDC\_sc} = \frac{V_{sc}}{V_{in}} = N_{s2} + N_{s2}\left(\frac{D}{1-D}\right) = \frac{N_{s2}}{1-D} \tag{4}$$

where D is the switching ratio. Each parameter of the derivation is denoted in Fig. 4. The steady-state voltage gain of the CCM flyback is derived as follows:

$$M_{VDC\_fb} = (N_{s1} + N_{s2})\left(\frac{D}{1-D}\right). \tag{5}$$

Consequently, the final input–output transfer function of the CSFB converter derived from the equivalent transformation in CCM is established as

$$M_{VDC} = M_{VDC_{sc}} + M_{VDC_{fb}} = \frac{D(N_{s1}+N_{s2})+N_{s2}}{1-D}. \tag{6}$$

C. DCM Transfer Gain of a CSFB Converter

To analyze the steady-state input–output DCM transfer gain of the proposed converter, the charge-pump switched-capacitor and flyback converter can be analyzed by power balance and volt-second balance. The following equation

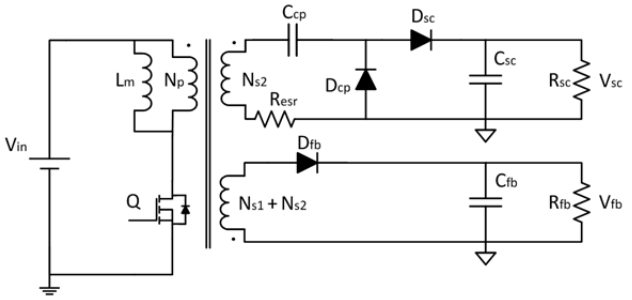


Fig. 4. Equivalent circuit of the proposed CSFB converter having separated outputs.

indicates the relation of input power and output power:

$$V_{in}I_s = \frac{{V_o}^2}{R_L} + R_{esr}{I_{N_{s2}}}^2 \quad (7)$$

where V_{in} is the input voltage, I_s is the input current, V_o is the output voltage, R_L is the load resistance, R_{esr} is the parasitic resistance of the transformer winding (N_{s2}), and $I_{N_{s2}}$ is the secondary current.

The input current (I_s) is as follows:

$$I_s = \frac{V_{in}D^2}{2L_mf} + \left(\frac{N_{s2}}{N_p}\right)\frac{V_o}{R_L} \quad (8)$$

where L_m is the magnetic inductance, and f is the switching frequency. From Equs. (7) and (8), the following equation can be derived:

$$\frac{{V_o}^2}{R_L} - V_{in}\left(\frac{N_{s2}}{N_p}\right)\frac{V_o}{R_L} - \left(\frac{{V_{in}}^2D^2}{2L_mf} - R_{esr}{I_{N_{s2}}}^2\right) = 0. \quad (9)$$

Thus, V_o is as follows:

$$V_o = \frac{V_{in}\left(\frac{N_{s2}}{N_p}\right) + \sqrt{{V_{in}}^2\left(\frac{N_{s2}}{N_p}\right)^2 + \frac{2{V_{in}}^2D^2R_L}{L_mf} - 4R_LR_{esr}{I_{N_{s2}}}^2}}{2}. \quad (10)$$

The final input–output transfer function of the CSFB converter derived from the equivalent transformation in DCM is derived as follows because $4RR_{esr}{I_{N_{s2}}}^2$ is negligible:

$$\frac{V_o}{V_{in}} = \frac{\left(\frac{N_{s2}}{N_p}\right) + \sqrt{\left(\frac{N_{s2}}{N_p}\right)^2 + \frac{2D^2R_L}{L_mf}}}{2}. \quad (11)$$

D. Operating Principles

The DCM operation, which eliminates the reverse recovery current of diodes, has some advantages in terms of power efficiency. The proposed converter has three operating modes, as shown in Figs. 5 and 6, according to the switching state.

Mode 1: The current flows in the magnetizing inductance and the primary winding (N_p) as a result of the switch (Q) turn-on. The primary current is transferred to the secondary (N_{s2}) coil of the isolated switched capacitor cell via the magnetic linkage (see Fig. 5, mode 1). Then, the secondary current is rectified into through the switched capacitor diode (D_{sc}), as shown in Figs. 5(a) and 6. The output capacitor (C_{fb}) discharges the load current because the flyback diode (D_{fb}) and charge pump diode (D_{cp}) are reverse biased.

Mode 2: When the switch (Q) is turned off, the switched

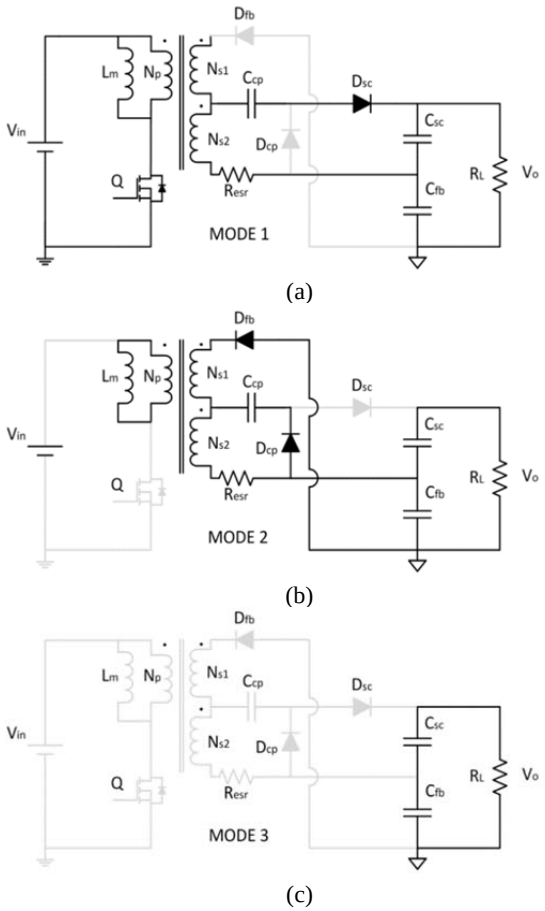


Fig. 5. Equivalent circuit of the CSFB in each operation mode. (a) Mode 1. (b) Mode 2. (c) Mode 3.

capacitor diode (D_{sc}) is reverse biased, and at the same time, the energy magnetically stored at L_m is released to the load through D_{fb} and D_{cp} of the charge pump and flyback converter (see Fig. 5, mode 2). The charge pump capacitor (C_{cp}) is charged by the reset current in this mode, as shown in Fig. 5(b), because the charge pump diode (D_{cp}) is forward biased. The output capacitor (C_{sc}) discharges the load current because the switched capacitor diode (D_{sc}) is reverse biased.

Mode 3: The transformer is de-magnetized completely during this period, and the output voltage is maintained by the discharge of the output capacitors (C_{sc}, C_{fb}) (see Fig. 5, mode 3). All rectifier diodes are reverse biased, as shown Fig. 5(c).

III. Power Loss Analysis and Design Guideline of the CSFB Converter

A. Power Loss Analysis of the CSFB Converter

The power efficiency of the CSFB converter changes depending on the boosting ratio and the load condition. To find the optimal operating point, the loss breakdown of the proposed converter is performed. The efficiency is estimated

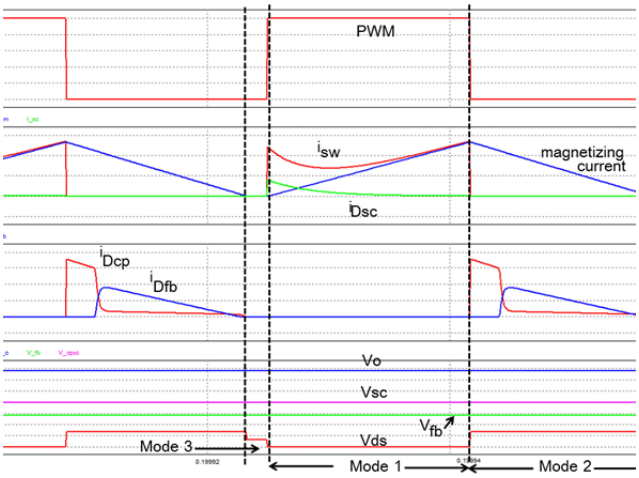


Fig. 6. DCM waveforms of the proposed CSFB converter.

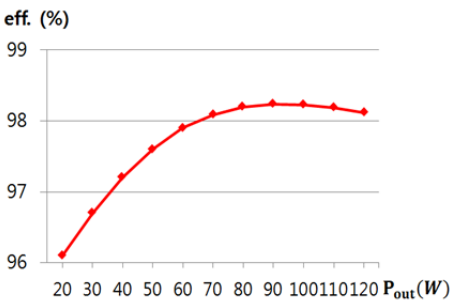


Fig. 7. Simulation result of the proposed CSFB converter according to the variation of the output power.

through an efficiency simulation according to the loss analysis of the high-frequency transformer, MOSFET, and diodes. The detail of the estimation procedure is presented in Appendix A. From the loss breakdown, the efficiency calculation has been done using MATLAB simulation. Figs. 7 and 8 show the MATLAB simulation result of the proposed CSFB converter according to the variation of the output power and the variation of the input voltage.

B. Analysis and Design of the Transformer

The key design components of the proposed CSFB converter are transformer, MOSFET, diodes, output capacitor, and so on. The following section suggests an example of the design procedure for the CSFB converter.

To guarantee the prevention of core saturation, primary winding number (N_p) should satisfy the constraint shown as follows,

$$N_p > \frac{10}{3}\frac{V_{s-max}D_{min}}{fA_e}. \quad (12)$$

The winding layer should be considered carefully for low leakage inductances that significantly contribute to the power efficiency and ringing suppression. To enhance the magnetic flux linkage, a coaxial cable transformer can be applied, as shown in Fig. 9 [26]. The coupling coefficient of an implemented transformer is more than 99.9%.

The transformer turn ratio should be determined by the

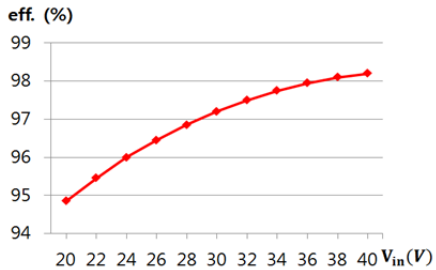


Fig. 8. Simulation result of the proposed CSFB converter according to the variation of the input voltage.

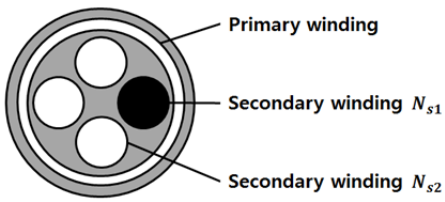


Fig. 9. Cross section of the coaxial cable.

voltage gain specification. The desirable proper operating duty cycle is within a range of 0.35–0.65; therefore, from the transfer gain of CCM or DCM, depending on the application, the turn ratios are determined. In CSFB, because the voltage gain range is from 8.95 to 14, the winding number is chosen from the DCM gain equation, such as:

$$N_p : N_{s1} : N_{s2} = 14 : 14 : 42. \quad (13)$$

To analyze the critical inductance for the DCM of the proposed converter, CCM and DCM transfer gain can be used as follows:

$$\frac{D(N_{s1}+N_{s2})+N_{s2}}{1-D} = \frac{N_{s2}+\sqrt{{N_{s2}}^2+\frac{2D^2R_L}{Lmf}}}{2}. \quad (14)$$

Thus, the critical inductance is as follows:

$$L_{m\_crit} = \frac{2D^2R_L}{f[(\frac{N_{s2}+D(2N_{s1}+3N_{s2})}{1-D})^2-{N_{s2}}^2]} \quad (15)$$

In this design example, the inductance is determined as 80 μH for the DCM operating margin.

C. MOSFET and Diodes

The voltage stress of the MOSFET is derived as

$$V_{ds-max} = V_{s-max} + \frac{V_o-N_{s2}V_{in-max}}{N_{s1}+2N_{s2}} = 71.43\ V. \quad (16)$$

The secondary-diode selection should consider voltage and current stresses, reverse-recovery characteristics, and so on. The voltage stress of charge pump V_{D_cp}, switched capacitor V_{D_sc}, and flyback diodes V_{D_fb} are respectively shown as

$$V_{D\_sc} = N_{s2}\left(V_{in} + \frac{V_o-N_{s2}V_{in}}{N_{s1}+2N_{s2}}\right) = 210\ \text{V} \quad (17)$$

$$V_{D\_cp} = V_{D\_sc} \quad (18)$$

and

$$V_{D\_fb} = (N_{s1}+N_{s2})\left(V_{in} + \frac{V_o-N_{s2}V_{in}}{N_{s1}+2N_{s2}}\right) = 287\ \text{V}. \quad (19)$$

Table I shows design results of CSFB rectifiers and MOSFET for the hardware prototype.

TABLE I
DIODES AND MOSFET UTLIZED IN THE HARDWARE

Symbol	Parameter(part number)	Spec.
D_{sc} , D_{cp}	MBR10250	250 V/ 10 A
D_{fb}	SF18	600 V / 1A
Q	IRFP4468PbF	100 V / 195 A

D. Output Capacitors

As mentioned earlier, the proposed CSFB converter has a reduced output ripple through an alternating charging action of the output capacitors. In order to analyze the output ripple, each capacitor currents need to be analyzed. In Fig. 10(a), switched capacitor current I_{D-sc} starts to charge at switch turn-on and starts to discharge when I_{D-sc} becomes equal to the output current I_o.

Switched capacitor current I_{D-sc} is as follows:

$$I_{D-sc}(t) = \frac{I_o T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)} e^{\frac{-t}{\tau}} \quad (20)$$

where $D_{x1}T$, which is the approximation discharging time, is as follows:

$$D_{x1}T = \tau \ln\left(\frac{2T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)}\right). \quad (21)$$

As shown in the last waveform in the figure, switch current i_{sw} becomes relatively more rectangular than that of previous topologies because of the superposition and triangular magnetizing current. This waveform contributes to the conduction loss reduction largely. As shown in Fig. 10(b), the flyback current starts to flow right after charge-pump charging (i_{Dcp}).

To find the start time of the flyback current, the conduction time correlation between the flyback and charge pump diodes need to be analyzed.

The average value of the flyback current (I_{D-fb}) and the charge pump current (I_{D-cp}) are the same. Therefore, the relationship between the currents is as follows:

$$\left(\frac{V_{in}DT}{N_{s2}L_m} - \frac{K_A D_{x2} T}{2}\right) D_{x2} = (D_1 - D_{x2})\left(\frac{D_1 - D_{x2}}{2} T K_B\right) T \quad (22)$$

where

$$K_A = \frac{V_o - N_{S2} V_{in}}{L_m(2N_{S2}+N_{S1})N_{S2}} \quad (23)$$

and

$$K_B = \frac{V_o - N_{S2} V_{in}}{L_m(2N_{S2}+N_{S1})(N_{S1}+N_{S2})}\ , \quad (24)$$

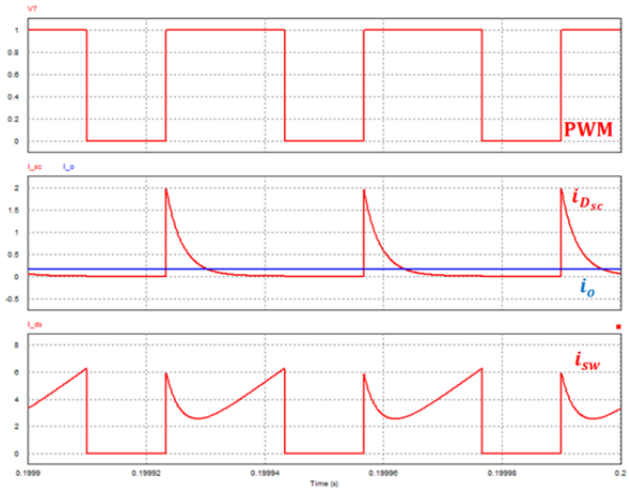
and D_1 is the reset ratio. Then, $D_{x2}T$, which means approximation discharging time, is as follows:

$$7{D_{x2}}^2 - 14D_{x2} + 3 = 0 \quad . \quad (25)$$

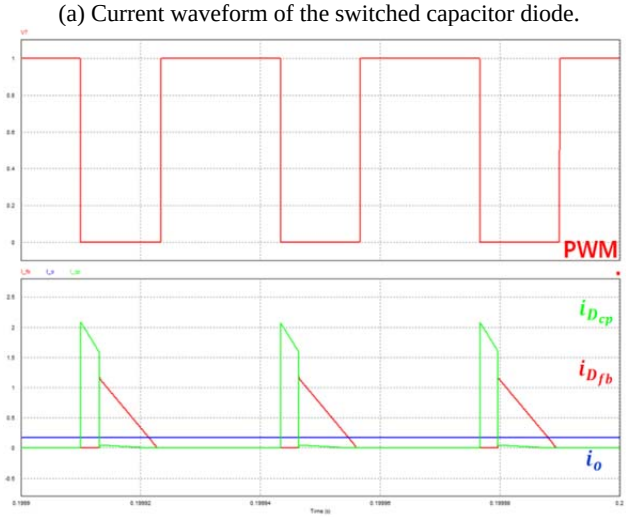
The output voltage ripple decided by the discharging time of both output capacitors is as follows:

$$\Delta V_o = \frac{I_o T(D - D_{x1} + D_{x2})}{C_o} \quad (26)$$

where C_o is an equivalent capacitance of both output capacitors. Consequently, the output capacitance for the 0.1% requirement output ripple is 7.89 μF.



(a) Current waveform of the switched capacitor diode.



(b) Current waveforms of the charge pump and the flyback rectifiers.

Fig. 10. Key waveforms of the diodes in the proposed topology.

IV. NON-ISOLATED CONVERTER USING THE PROPOSED CHARGE-PUMP SWITCHED-CAPACITOR CELL

A. Structure of the Non-Isolation Converter

The structure of the proposed non-isolated DC–DC converter is shown in Fig. 11. The primary has a PWM switching voltages generated by a single main switch in a tapped-inductor boost converter. The secondary has an isolated charge-pump switched capacitor and a flyback. All of the outputs are serially connected to boost the output voltage [27]. The converter is named the "CSFTI converter."

As a CSFB converter, the proposed CSFTI converter makes an effective utilization of the transformer and the output ripple is reduced through the phase differences of the charging or discharging time among the output capacitors.

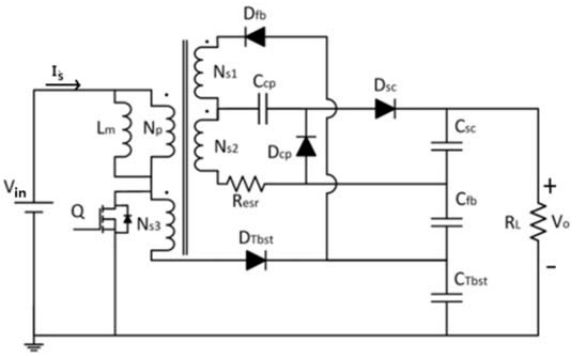


Fig. 11. CSFTI boost converter.

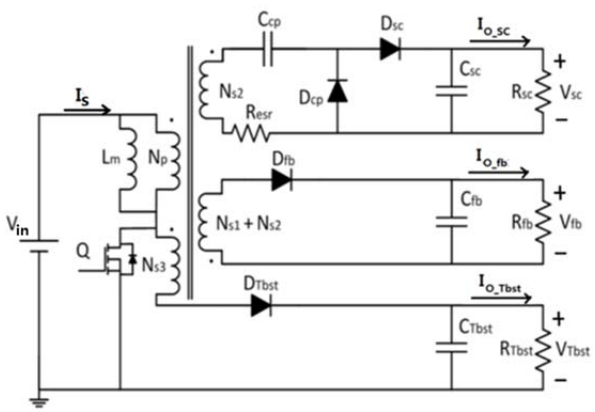


Fig. 12. Equivalent circuit of the proposed CSFTI converter having equivalent output separation.

Furthermore, the three outputs share the output voltage stress in series, so the application of Schottky diode is allowed.

B. CCM Transfer Gain of CSFTI Converter

To analyze the steady-state CCM transfer gain of the proposed CSFTI converter, the charge-pump switched-capacitor, flyback, and tapped-inductor boost converters can be analyzed by output separation using an equivalent circuit transformation, as shown in Fig. 12. Output currents I_{O_sc}, I_{O_fb}, and I_{O_Tbst} are the same because of the series connection in the series-connected CSFTI boost converter. Equ. (27) indicates each of the load resistances for the equivalent transformation:

$$R_{sc} = \frac{V_{sc}}{I_{Load}}, \quad R_{fb} = \frac{V_{fb}}{I_{Load}}, \quad R_{Tbst} = \frac{V_{Tbst}}{I_{Load}} \qquad (27)$$

where V_{sc} is the switched capacitor output, V_{fb} is the flyback output, and V_{Tbst} is the tapped-inductor boost output.

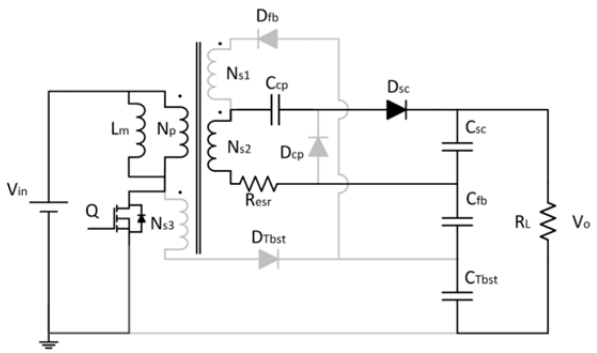
As aforementioned, the steady-state voltage gain of the isolated switched capacitor is as follows:

$$M_{VDC\_sc} = \frac{V_{sc}}{V_{in}} = N_{s2} + N_{s2}\left(\frac{D}{1-D}\right) = \frac{N_{s2}}{1-D} \qquad (28)$$

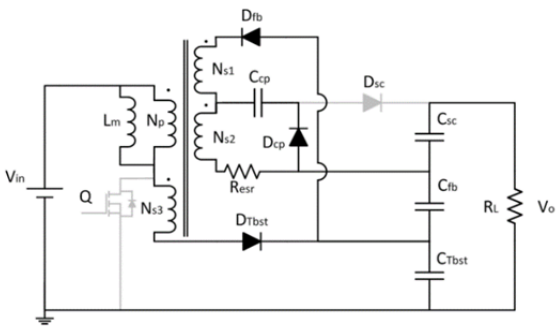
where D is the switching ratio. The steady-state voltage gain of the CCM flyback is derived as follows:

$$M_{VDC\_fb} = (N_{s1} + N_{s2})\frac{D}{1-D}. \qquad (29)$$

The steady-state voltage gain of the CCM tapped-inductor boost converter is derived as follows:



(a)



(b)

Fig. 13. Equivalent circuit of CSFTI in each operating mode. (a) Mode 1. (b) Mode 2.

$$M_{VDC\_Tbst} = \frac{\left(\frac{1-D}{1+N_{S3}}\right)+D}{\left(\frac{1-D}{1+N_{S3}}\right)}. \qquad (30)$$

Consequently, the final input–output transfer function is

$$M_{VDC} = \frac{1+N_{S2}+D(N_{S1}+N_{S2}+N_{S3})}{1-D} \quad . \qquad (31)$$

C. Operating Principles

The CCM operation, which reduces the RMS value of the magnetic current, has a benefit in terms of power efficiency by applying Schottky diodes, which eliminates the reverse recovery current of the diodes [28]. The proposed converter has two operating modes, as shown in Fig. 13. The mode analysis can be used not only for the steady-state analysis but also for the dynamic analysis using a state-space averaging technique [29]-[31].

Mode 1: The current flows in the magnetizing inductance and the primary winding (N_p), as the switch (Q) turns on. The primary current is transferred to the secondary (N_{s2}) coil of the isolated switched capacitor cell via the magnetic linkage. Then, the secondary current is rectified into DC through the switched capacitor diode (D_{sc}). Because the flyback diode (D_{fb}), tap-inductor boost diode (D_{Tbst}), and charge pump diode (D_{cp}) are reverse biased, output capacitors C_{fb} and C_{Tbst} discharge the load current.

Mode 2: When the switch ($\boldsymbol{Q}$) is turned off, the switched capacitor diode ($\boldsymbol{D_{sc}}$) is reverse biased, and at the same time, the energy magnetically stored at $\boldsymbol{L_m}$ is released to the load through $\boldsymbol{D_{fb}}$, $\boldsymbol{D_{Tbst}}$, and ($\boldsymbol{D_{cp}}$). Because the charge pump

TABLE II
DIODES AND MOSFET UTLIZED IN THE CSFTI HARDWARE

Symbol	Parameter(part number)	Spec.
D_{sc} , D_{cp}	MBR10200	200 V/ 10 A
D_{fb}	MBR10250	250 V / 10A
D_{Tbst}	SF18	600 V / 1 A
Q	IRFP4468PbF	100 V / 195 A

diode ($\boldsymbol{D_{cp}}$) is forward biased, the charge pump capacitor ($\boldsymbol{C_{CP}}$) is charged by the reset current in this mode. Because the switched capacitor diode ($\boldsymbol{D_{sc}}$) is reverse biased, the output capacitor ($\boldsymbol{C_{sc}}$) discharges the load current in this mode**.**

V. POWER LOSS ANALYSIS AND DESIGN GUIDELINE OF THE CSFTI CONVERTER

A. Power Loss Analysis of CSFTI Converter

To find the optimal operating point, the loss breakdown of the proposed converter is performed. The efficiency is estimated through an efficiency simulation according to the loss analysis of the high-frequency transformer, MOSFET, and diodes. The detail of the estimation procedure is presented in Appendix B. As a CSFB converter, the power efficiency is maintained high in the entire input and load ranges.

B. Analysis and Design of the Transformer

Boost ratios of the CSFTI converter is determined by the transformer winding, as shown in the CCM transfer gain. Therefore, the first procedure is to decide the primary winding number (N_p) for guarantee of high efficiency and of prevention from core saturation. Then, the next step is winding ratios.

The winding number of the transformer is chosen as

$$N_p : N_{s1} : N_{s2} : N_{s3} = 13 : 13 : 39 : 52. \quad (36)$$

The critical inductance is as follows:

$$L_{m\_crit} = \frac{2D^2 R_L}{f[(\frac{2+N_{S2}-N_{S3}+D(2N_{S1}+3N_{S2}+3N_{S3})}{1-D})^2-(N_{S2}+N_{S3})^2]}. \quad (37)$$

In this design example, the inductance is determined as 400 μH for the CCM operation margin.

C. MOSFET and Diodes

The voltage stress of the MOSFET, V_{ds-max}, and the diodes are derived as

$$V_{ds-max} = V_{in-max} + \frac{V_o - N_{s2}V_{in-max}}{N_{s1}+2N_{s2}+N_{s3}} = 56.36\ V \quad (38)$$

$$V_{D\_sc} = V_{D\_cp} = \frac{N_{s2}V_{in}}{1-\mathrm{D}} = 156\ V \quad (39)$$

$$V_{D\_fb} = \frac{(N_{s1}+N_{s2})V_{in}}{1-\mathrm{D}} = 208\ \mathrm{V} \quad (40)$$

and

TABLE III
KEY PARAMETER OF CSFB CONVERTER HARDWARE

Symbol	Parameter(part number)	Spec.
V_{in}	Input voltage	25–40 VDC
V_{out}	Output voltage	340 VDC
P_{out}	Output power	30–100 W
f_s	Switching frequency	30 kHz
L_m	Magnetizing inductance	80 μH
Q	Main switch (IRFP4468)	100 V, 195 A
N_p	Primary winding	14 turns
N_{s1}, N_{s2}	Secondary winding	14 / 42 turns
D_{sc}, D_{cp}	Switched capacitor's diode (MBR10250)	250 V, 10 A
D_{fb}	Boost's diode(SF18)	600 V, 1 A

$$V_{D\_Tbst} = \frac{(N_p+N_{s3})V_{in}}{1-\mathrm{D}} = 261\ V \quad (41)$$

where the voltage stress of the tapped inductor is V_{D_Tbst}, the switched capacitor is V_{D_sc}, and the flyback diodes is V_{D_fb}. Table II shows a design result of CSFTI rectifiers and MOSFET for the hardware prototype.

D. Output Capacitors

The output capacitance for the output ripple is similar to the CSFB. All the difference is tapped-inductor boost capacitor C_{Tbst}, which has the same current waveform as that of C_{fb}. The ripple equation is approximately the same as Equ. (26).

VI. EXPERIMENTAL VALIDATION

A. Experimental Results of the CSFB Converter

To verify the aforementioned analysis, a 100-W hardware prototype of the CSFB PWM converter has been implemented. The hardware part list is presented in Table III.

Fig. 14 shows the waveforms of the PWM gate signal, switch current, the secondary waveforms of the charge pump current, and the MOSFET drain–source voltage without a snubber. As shown in figure, the inductor of the charge pump switched capacitor and the flyback converter are operating in the DCM. From the results, the hardware waveforms agree well with the theoretical analysis shown in Section III. In the waveform of I_{ds} , the switch current becomes more rectangular, which contributes to the conduction-loss reduction because of the small RMS value.

Fig. 15 shows the power efficiency according to the input voltage and the output power variation. According to the experimental results, the efficiency is greater than 97% in the gain range of 8–9 (35–40 V input). Then, the efficiency is gradually reduced as the input voltage, and the output power decreases, which is similar to the simulation in Section III. As the figure shows, the proposed CSFB converter maintains high efficiency over 95% in the entire operating conditions,

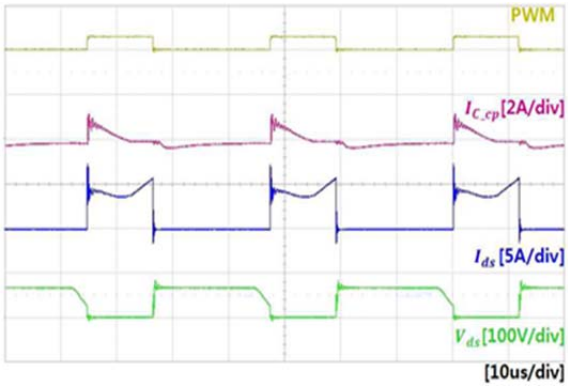


Fig. 14. Key waveforms of the hardware experiment (PWM: PWM gate signal; $\boldsymbol{I_{C-CP}}$: charge-pump current; $\boldsymbol{I_{ds}}$: drain–source current; $\boldsymbol{V_{ds}}$: drain–source voltage).

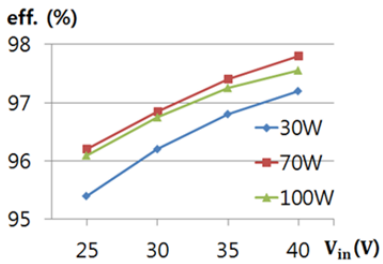
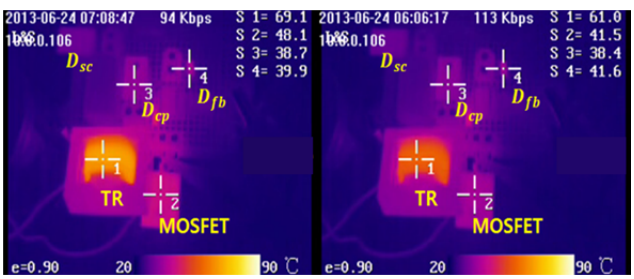


Fig. 15. Experimental result of the CSFB converter according to the variation of the input voltage.



(a) (b)

Fig. 16. Comparison of the thermal distribution of the hardware prototypes. (a) $\boldsymbol{V_{in}}$=25 V. (b) $\boldsymbol{V_{in}}$=40 V.

along with good galvanic isolation.

Fig. 16 shows a couple of the temperature distributions of a CSFB hardware with an identical operating condition, except the input voltage. The experiment was done at the ambient temperature, and the MOSFET and secondary diodes have no heat sink. The spot of main heat sources such as transformer (TR), main switch (MOSFET), and diodes (D_{CP}, D_{fb}, and D_{SC}) are indicated in the figure. The results show that the temperatures of the diodes are not significantly different, which means the loss changes in the diodes are quite small even though the voltage gain increases. The temperature of the main switch rises up to 48.1 °C from 41.5 °C, and the primary winding also rises up to 69.1 °C from 61.0 °C. The temperature measurement is explained well by the loss breakdown in Section III and efficiency measurement in Fig. 15. Based on the experimental results, a conclusion is drawn that the CSFB topology is effective for reducing the severe power stress in the extreme step-up-isolated converters.

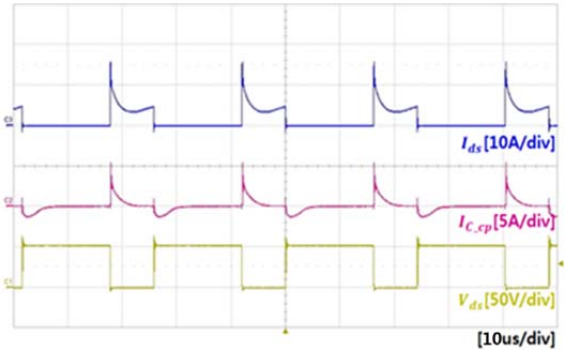


Fig. 17. Key waveforms. ($\boldsymbol{I_{C-CP}}$: charge-pump current; $\boldsymbol{I_{ds}}$: drain–source current; $\boldsymbol{V_{ds}}$: drain–source voltage).

TABLE IV
KEY PARAMETER OF CSFB TAP-INDUCTOR BOOST CONVERTER HARDWARE

Symbol	Parameter(part number)	Spec.
V_{in}	Input voltage	15–35 VDC
V_{out}	Output voltage	340 VDC
P_{out}	Output power	30–100 W
f_s	Switching frequency	40 kHz
L_m	Magnetizing inductance	400 μH
Q	Main switch (IRFP260N)	200 V, 50 A
N_p	Primary winding	13 turns
N_s	Secondary winding	91 turns
D_{sc}	Switched capacitor's diode (UF4006)	800 V, 1 A
D_{Tbst}	Boost's diode(UF4004)	400 V, 1 A

B. *Experimental Results of the CSFTI Converter*

In terms of the CSFB converter, a 100-W hardware prototype of the proposed CSFTI PWM converter has been implemented to verify the operation principles and the performance of the converter. The implemented component data concerning the prototype are listed in Table IV.

Fig. 17 shows the waveforms of the switch current, the secondary waveforms of the charge-pump current, and the MOSFET drain–source voltage without a snubber. As shown in the figure, the proposed converter operates in the CCM. From the results, the hardware waveforms agree well with the theoretical analysis shown in Section IV.

Fig. 18 shows the power efficiency according to the input voltage and the output power variation. From the experimental results, efficiency is greater than 97% in the step-up gain of almost 10 (30–35 V input). As shown in the figure, the proposed CSFTI converter maintains a high efficiency of over 94% with high step-up ratio from 10 to 22 in the entire output variation.

C. *Experimental Results of the Output Voltage Ripple*

To verify the small output ripple that allows small output capacitances, a hardware prototype of the CSFB converter was tested. Table V shows the operating condition.

Fig. 19 shows the output voltage ripple and the flyback

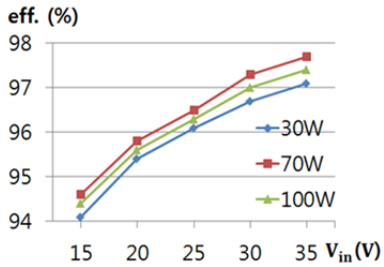


Fig. 18. Experimental result of the CSFTI converter according to the variation of the input voltage.

TABLE V
TEST CONDITION OF CSFB CONVERTER HARDWARE

Symbol	Parameter(part number)	Spec.
V_{in}	Input voltage	20 VDC
V_{out}	Output voltage	205 VDC
P_{out}	Output power	28 W

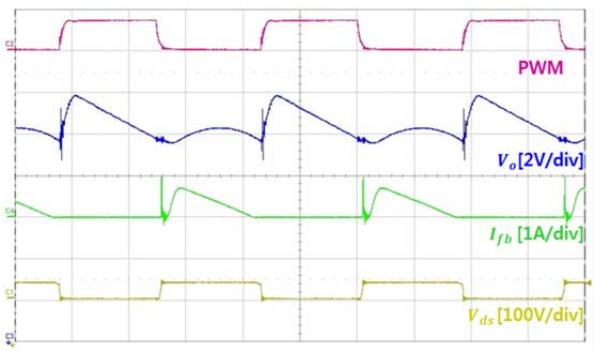


Fig. 19. Key waveforms of the hardware experiment including an output voltage ripple.

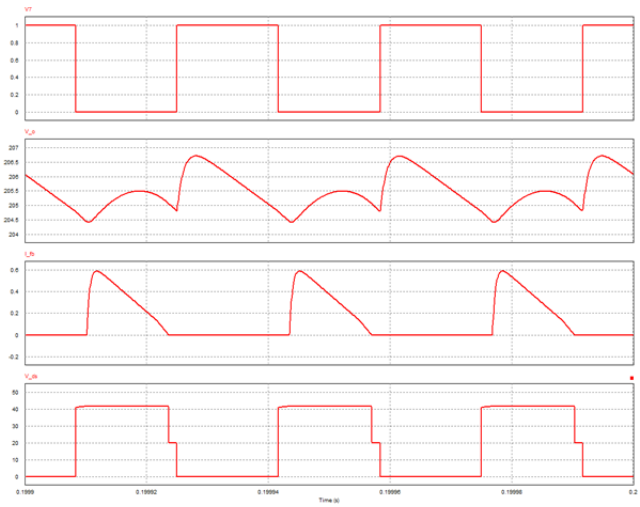


Fig. 20. Key waveforms of the simulation with the output voltage ripple. Parameters are in the same order as in Fig. 19.

current. The equivalent capacitance of the output capacitors is 0.6 μF through the use of several tens of nano-Farad ceramic capacitors. As shown in Fig. 20, the output ripple waveform (V_O) agrees well with the theoretical analysis shown in Chapter III.

VII. CONCLUSION

In this paper, a pre-regulating DC–DC converters, specifically a series-connected CSFB converter for multistage photovoltaic power conditioning systems, has been proposed. The single-ended charge-pump-flyback operation contributing to the high-density power delivery of the transformer is quite beneficial to the enhancement of the output voltage with low cost. The operational principle of the proposed converter has been presented through obtaining the equivalent transformation from load-sharing ratio in a series output. An experimental result with a 100-W hardware prototype is also included to show that the proposed converter has a high efficiency that is greater than 97% in the range of 25–40 V input to 340 V output.

For the topology extension, another novel high-step-up series-connected CSFB converter employing a tapped-inductor has been presented. The tapped inductor allows an extreme step-up voltage while maintaining a moderate duty ratio. In addition, the switching component stresses are decreased by the application of a charge-pump switched-capacitor cell. All the subconverters are integrated with a single switch and a single magnetic device, leading to increase in the converter efficiency with minimum extra cost. The experimental results of a 100-W hardware prototype verify the performance estimation of extremely high efficiency.

APPENDIX

A. Loss Analysis of the CSFB Converter

1) MOSFET Loss Analysis: The switching loss is

$$P_{Q\_sw} = \frac{f C_{sw} {V_{in}}^2}{2} \tag{42}$$

where C_{sw} is the output capacitor of the MOSFET.

To analyze the conduction loss of the MOSFET, switched-capacitor current should be performed. The switched-capacitor current is

$$i_{D_{sc}}(t) = \frac{I_o T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)} e^{\frac{-t}{\tau}}. \tag{43}$$

The switch current is

$$i_s(t) = \frac{N_{s2} I_o T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)} e^{\frac{-t}{\tau}} + \frac{V_{in}}{L_m} t. \tag{44}$$

The RMS current of the MOSFET is

$$I_{s-rms} = \sqrt{\left[\frac{1}{T}\left[\frac{1}{2\tau}\left(\frac{N_{s2} I_o T}{1-e^{\frac{-DT}{\tau}}}\right)^2\left(1-e^{\frac{-2DT}{\tau}}\right) + \frac{\left(\frac{V_{in}}{L_m}\right)^2}{3}(DT)^3 + \frac{N_{s2} I_o T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)}\left(\frac{2V_{in}}{L_m}\right)\left(\tau^2 - \tau e^{\frac{-DT}{\tau}}(DT+\tau)\right)\right]\right]}. \tag{45}$$

The conduction loss is

$$P_{Q-rDS} = r_{DS} {I_{s-rms}}^2. \tag{46}$$

The total MOSFET loss is

$$P_Q = P_{Q-rDS} + P_{Q-sw.} \quad (47)$$

2) Diode Loss Analysis: The diode loss model is divided into a constant voltage sink (V_F) and a constant resistor (R_F).

The average current of all diodes are same as the output current (I_o).

The total diode loss is

$$P_D = V_F I_o + R_F {I_{D-rms}}^2. \quad (48)$$

RMS current of the switched capacitor diode ($I_{D_{sc}-rms}$) is

$$I_{D_{sc}-rms} = \sqrt{\frac{\tau}{2T}\left(\frac{I_o T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)}\right)^2\left(1-e^{\frac{-2DT}{\tau}}\right)}. \quad (49)$$

The current of the charge-pump diode ($I_{D_{cp}}(t)$) is

$$i_{D_{cp}}(t: DT\sim(D+D_1)T) = \frac{N_{s2}V_{in}-V_o}{2(N_{s1}+2N_{s2})L_m}t + \frac{\{V_o-N_{s2}V_{in}+2(N_{s1}+2N_{s2})V_{in}\}DT}{2(N_{s1}+2N_{s2})L_m}. \quad (50)$$

The RMS current of the charge pump diode ($I_{D_{cp}-rms}$) is

$$I_{D_{cp}-rms} = \sqrt{\frac{K_{D_{cp1}}^2 T^2 D_1}{3}(3D^2+(3D+D_1)D_1) + K_{D_{cp1}}K_{D_{cp2}}T(2DD_1+D_1^2) + K_{D_{cp2}}^2 D_1}$$

where,

$$K_{D_{cp1}} = \frac{N_{s2}V_{in}-V_o}{2(N_{s1}+2N_{s2})L_m}, K_{D_{cp2}} = \frac{\{V_o-N_{s2}V_{in}+2(N_{s1}+2N_{s2})V_{in}\}DT}{2(N_{s1}+2N_{s2})L_m}. \quad (51)$$

The RMS current of the flyback is similar to the charge pump current.

3) Transformer Loss Analysis: The parasitic resistance of the winding is derived as

$$R_{N-esr} = \frac{\rho n(MLT)}{A_\omega}. \quad (52)$$

The conduction loss of the primary winding is same as MOSFET current. Thus the loos is

$$P_{N_p} = R_{N_p}{I_{s-rms}}^2. \quad (53)$$

The on-time conduction loss of the secondary winding is

$$P_{N_s-on} = R_{N_{s2}}{I_{D_{sc}-rms}}^2. \quad (54)$$

The off-time conduction loss of the secondary winding is

$$P_{N_s-on} = \left(R_{N_{s1}} + 2R_{N_{s2}}\right){I_{D_{cp}-rms}}^2. \quad (55)$$

The hysteresis energy loss can derived from

$$W_{Tr-hys} = \int v(t)i(t)dt = \int\left(nA_c\frac{dB(t)}{dt}\right)\left(\frac{H(t)l_m}{n}\right)dt = A_c l_m \int H\cdot dB. \quad (56)$$

Thus, the power loss is derived as

$$P_{Tr-hys} = f A_c l_m \int H\cdot dB \quad (57)$$

where $A_c l_m$is the volume of the core.

B. Loss Analysis of the CSFTI Converter

1) MOSFET Loss Analysis: To analyze the conduction loss of the primary winding, the on-time and off-time current of the winding should be derived. The on-time MOSFET current is

$$i_s(t: 0\sim DT) = \frac{N_{s2}I_o T}{\tau\left(1-e^{\frac{-DT}{\tau}}\right)}e^{\frac{-t}{\tau}}\frac{V_{in}}{L_m}t. \quad (58)$$

The off-time primary winding current is

$$i_s(t: DT\sim T) = \frac{N_{s2}V_{in}-V_o}{3(N_{s1}+2N_{s2}+N_{s3})L_m}t + \frac{\{V_o-N_{s2}V_{in}+2(N_{s1}+2N_{s2}+N_{s3})V_{in}\}DT}{3(N_{s1}+2N_{s2}+N_{s3})L_m}. \quad (59)$$

Then, the total RMS current of the primary is

$$I_{s-rms} = \sqrt{\frac{1}{T}\left[\int_0^{DT} i_s(t: 0\sim DT)^2 dt + \int_{DT}^{T} i_S(t: DT\sim T)^2\, dt\right]}. \quad (60)$$

2) Tapped-Inductor Boost-Diode Loss Analysis: The current of the tap-inductor boost diode ($I_{D_{Tbst}}(t)$) is same as the off-time primary current.

The RMS current of the tap-inductor boost diode is

$$I_{D_{Tbst}-rms} = \sqrt{\frac{K_{T1}^2 T^2}{3}(1-D^3) + K_{T1}K_{T2}T(1-D^2) + K_{T2}^2(1-D)}$$

$$K_{T1} = \frac{N_{s2}V_{in}-V_o}{3(N_{s1}+2N_{s2}+N_{s3})L_m}, K_{T2} = \frac{\{V_o-N_{s2}V_{in}+2(N_{s1}+2N_{s2}+N_{s3})V_{in}\}DT}{3(N_{s1}+2N_{s2}+N_{s3})L_m}. \quad (61)$$

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