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A Parallel Hybrid Soft Switching Converter with Low Circulating Current Losses and a Low Current Ripple

Bor-Ren Lin† and Jia-Sheng Chen*

†,*Department of Electrical Engineering, National Yunlin University of Science and Technology, Yunlin, Taiwan

Abstract

A new parallel hybrid soft switching converter with low circulating current losses during the freewheeling state and a low output current ripple is presented in this paper. Two circuit modules are connected in parallel using the interleaved pulse-width modulation scheme to provide more power to the output load and to reduce the output current ripple. Each circuit module includes a three-level converter and a half-bridge converter sharing the same lagging-leg switches. A resonant capacitor is adopted on the primary side of the three-level converter to reduce the circulating current to zero in the freewheeling state. Thus, the high circulating current loss in conventional three-level converters is alleviated. A half-bridge converter is adopted to extend the ZVS range. Therefore, the lagging-leg switches can be turned on under zero voltage switching from light load to full load conditions. The secondary windings of the two converters are connected in series so that the rectified voltage is positive instead of zero during the freewheeling interval. Hence, the output inductance of the three-level converter can be reduced. The circuit configuration, operation principles and circuit characteristics are presented in detail. Experiments based on a 1920W prototype are provided to verify the effectiveness of the proposed converter.

Key words: Hybrid converter, Phase-shift PWM, Soft switching, Three-level converter

I. INTRODUCTION

In medium and high power applications, three-phase AC/DC converters are usually used to provide stable DC voltages for industrial power units. Three-phase bridge or bridgeless power factor correctors (PFC) are normally adopted in the front stage to compensate the input power quality with a nearly unit power factor and low total harmonic distortion of the line current. Three-level DC/DC converters [1]-[8] are used as the second stage to provide a stable low output voltage with a high load current. Phase-shift pulse-width modulation (PSPWM) is normally used to generate gating signals and to regulate the output voltage. However, the main disadvantages of the conventional PSPWM full-bridge converter and three-level converters are a narrow ZVS range at the lagging-leg switches and high circulating current losses. Additional passives or active components added on the primary or secondary side have been presented in [9]-[14] to reduce the circulating current in the freewheeling state and to extend the ZVS range of the lagging-leg switches. The basic idea behind these techniques is to generate a positive voltage at the freewheeling state in order to reduce the primary current to zero. However, additional power losses can occur on these extra components. Thus, the total circuit efficiency cannot be improved. A large leakage inductance or low magnetizing inductance can be used on the primary side to extend the ZVS range of the lagging-leg switches. However, the large leakage inductor will also increase the duty cycle loss and decrease the effective duty cycle. Thus, the conduction losses on the primary side will be increased and the circuit efficiency is reduced.

A parallel soft switching DC/DC converter is presented in this paper. The proposed converter includes two hybrid circuit modules to reduce the current stress of the active and passive power components. Each circuit module includes a

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†Corresponding Author: linbr@yuntech.edu.tw
Tel: +886-5-534-2601 ext. 4284, Fax: +886-5-531-2065, Nat'l Yunlin Univ. of Science and Technology
*Department of Electrical Engineering, National Yunlin University of Science and Technology, Taiwan

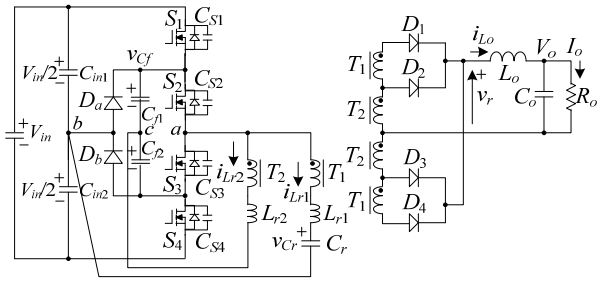


Fig. 1. The proposed hybrid converter (a) circuit diagram (b) main PWM waveforms.

three-level PWM converter and a half-bridge converter to achieve the functions of a low circulating current, a wide ZVS range and a low output inductance. The half-bridge converter shares the lagging-leg switches of the three-level converter and operates at a 0.5 duty cycle control. The primary side current of the half-bridge converter can enable the lagging-leg switches to be turned on at ZVS from a light load. Thus, the narrow ZVS range in the conventional three-level converter is overcome in the proposed converter. The secondary windings of two converters are connected in series so that a positive rectified voltage instead of zero voltage is generated on the secondary side in the freewheeling state. This positive rectified voltage is reflected to the primary side to reduce the circulating current to zero. Thus, the circulating current losses on the primary side can be reduced and the circuit efficiency is improved. Since the output inductor voltage during the freewheeling state is also reduced, the size of output filter inductor can also be reduced. Two hybrid circuit modules are operated using the interleaved PWM scheme. The input and output current ripples can be reduced. During the active mode, both the three-level converter and half-bridge converter transfer energy from the input voltage to the output load. In the freewheeling state, only the half-bridge converter transfers energy to the output load. The circuit configuration, operation principles and circuit characteristics are presented in detail. Finally, experimental results with a 1920W laboratory prototype converting 800V to 48V/40A are provided to validate the theoretical analysis and effectiveness of the proposed converter.

II. PROPOSED CONVERTER

Fig. 1(a) shows a circuit diagram of the proposed hybrid DC/DC converter. The main proposed converter includes a three-level converter and a half-bridge converter. The lagging-leg switches S_2 and S_3 are shared by the three-level converter (C_{in1}, C_{in2}, D_a, D_b, C_{f1}, C_{f2}, S_1-S_4, T_1, L_{r1}, C_r, D_1, D_4 and L_o) and the half-bridge converter (C_{f1}, C_{f2}, S_2, S_3, T_2, L_{r2}, D_2, D_3 and L_o). The energy stored in the output inductor is reflected to the primary side to achieve the ZVS operation of all of the switches instead of only the leading-leg switches in the conventional three-level converter. The resonant capacitor C_r in the three-level converter is used to reduce the primary current to zero in the freewheeling state. Therefore, the circulating current losses on the primary side can be reduced. The secondary windings of the two converters are connected in series so that the rectified voltage v_r is positive instead of zero in the freewheeling state. Hence, the inductor voltage v_{Lo} in the freewheeling state is reduced and the inductor current ripple is decreased when compared to the conventional three-level converter.

III. OPERATION PRINCIPLES

In the proposed hybrid converter, the phase-shift PWM scheme is adopted to control the necessary duty cycle on the primary side and to regulate the output voltage. The PWM signal of S_2 (S_3) is phase-shifted with respective to the PWM signal of S_1 (S_4). S_1 (S_2) and S_4 (S_3) operate complementarily with a short dead time to avoid short circuits at the high voltage side. The main PWM waveforms of the proposed converter are shown in Fig. 1(b). It is assumed that the power semiconductors including S_1-S_4, D_a-D_d and D_1-D_4 are ideal, the turns ratios of T_1 and T_2 are n_1 and n_2, respectively, $C_{S1}=C_{S2}=C_{S3}=C_{S4}=C_{oss}$, and $V_{Cin1}=V_{Cin2}=V_{Cf1}+V_{Cf2}=V_{in}/2$. Based on the on/off states of S_1-S_4, D_a-D_d and D_1-D_4, there are six operating stages in each half of a switching period. The duty cycle δ is defined as the turn-on interval of (S_1 and S_2) or (S_3 and S_4). Fig. 2 gives the topological circuits for the six operating stages during the first half of a switching period.

***Stage* 1 [t_0 - t_1]:** Prior to time t_0, switches S_1 and S_2 and diodes D_1 and D_3 are conducting. The primary currents i_{Lr1} and i_{Lr2}

are positive. At time t_0, the diode current i_{D3} decreases to zero. The voltages $v_{ab}=V_{in}/2$ and $v_{ac}=V_{Cf1}=V_{in}/4$. The primary currents can be approximately expressed as $i_{Lr1}\approx I_o/n_1$ and $i_{Lr2}\approx I_o/n_2$. The capacitor voltage v_{Cr} is given as $v_{Cr}(t)\approx v_{Cr}(t_0)+I_o(t-t_0)/(C_r n_1)$. The voltage variation Δv_{Cr} in this stage can be expressed as:

$$\Delta v_{Cr}=v_{Cr}(t_1)-v_{Cr}(t_0)\approx\frac{I_o\delta T_s}{C_r n_1} \tag{1}$$

Therefore, the rectified voltage at the transformer secondary side is given as:

$$\begin{aligned} v_r &=[\frac{V_{in}}{2}-v_{Cr}(t)]/n_1+\frac{v_{Cf1}}{n_2} \\ &\approx\frac{V_{in}}{2n_1}-\frac{I_o}{C_r n_1^2}(t-t_0)+\frac{I_o\delta T_s}{2C_r n_1^2}+\frac{V_{in}}{4n_2} \end{aligned} \tag{2}$$

The output inductor voltage $v_{Lo}=v_r-V_o>0$ so that the inductor current i_{Lo} increases in this stage.

***Stage* 2 [t_1 - t_2]:** At time t_1, switch S_1 is turned off. The energy stored in the output inductor L_o is reflected to the primary side to charge C_{S1} and discharge C_{S4}.

$$v_{CS1}=\frac{I_o}{2C_{oss}n_1}(t-t_0) \tag{3}$$

$$v_{CS4}=\frac{V_{in}}{2}-\frac{I_o}{2C_{oss}n_1}(t-t_0) \tag{4}$$

Thus, S_4 can be easily turned on under ZVS and the ZVS condition of S_4 is given as:

$$(L_{r1}+n_1^2L_o)\times i_{Lr1}^2(t_1)\ge C_{oss}V_{in}^2/2 \tag{5}$$

At t_2, capacitor C_{S4} is discharged to zero voltage and the rectified voltage v_r is decreased to $V_{in}/(4n_2)$. The time interval Δt_{12} in stage 2 can be obtained from (4) and expressed as:

$$\Delta t_{12}=t_2-t_1\approx\frac{V_{in}C_{oss}n_1}{I_o} \tag{6}$$

The dead time t_d between switches S_1 and S_4 must be greater than the time interval Δt_{12} in order to turn on S_4 under ZVS.

***Stage* 3 [t_2 - t_3]:** At time t_2, $v_{CS4}=0$. Since $i_{S4}(t_2)<0$, the anti-parallel diode of S_4 conducts. S_4 can be turned on at this moment under ZVS. The voltages $v_{ab}=0$ and $v_{ac}=V_{in}/4$ and diodes D_1 and D_2 are conducting to commutate the secondary side current of T_1. The diode current i_{D1} decreases and i_{D2} increases. In this stage, L_{r1} and C_r are resonant to reduce the primary current i_{Lr1} to zero.

***Stage* 4 [t_3 - t_4]:** At time t_3, the diode current i_{D1} is decreased to zero and only diode D_2 conducts the load current. The primary current i_{Lr1} of the three-level converter is decreases to zero so that no power is transferred through the three-level converter. The circulating current in this freewheeling state is reduced to zero and there is no circulating loss in this stage. The primary current of the half-bridge converter $i_{Lr2}=i_{Lo}/n_2$ and the energy is transferred from the input capacitor C_{f1} to the output load by the half-bridge converter in this stage. The rectified voltage $v_r\approx V_{in}/(4n_2)$. The output inductor voltage $v_{Lo}\approx V_{in}/(4n_2)-V_o<0$. Therefore, the inductor current i_{Lo} decreases in this stage.

***Stage* 5 [t_4 - t_5]:** Switch S_2 is turned off at t_4. Since $i_{Lr2}(t_4)>0$ and D_2 is conducting, the energy stored in L_o is reflected to the primary sides to charge C_{S2} and discharge C_{S3}.

$$v_{CS2}\approx\frac{I_o}{2C_{oss}n_2}(t-t_4) \tag{7}$$

$$v_{CS3}\approx\frac{V_{in}}{2}-\frac{I_o}{2C_{oss}n_2}(t-t_4) \tag{8}$$

The ZVS condition of S_3 is approximately given as:

$$(L_{r2}+n_2^2L_o)\times i_{Lr2}^2(t_4)\ge C_{oss}V_{in}^2/2 \tag{9}$$

At time t_5, C_{S3} is discharged to zero voltage. The time interval $\Delta t_{45}$is obtained as:

$$\Delta t_{45}=t_5-t_4\approx\frac{V_{in}C_{oss}n_2}{I_o} \tag{10}$$

The dead time t_d between switches S_2 and S_3 must be greater than the time interval Δt_{45} in order to turn on S_3 under ZVS.

***Stage* 6 [t_5 - t_6]:** At time t_5, C_{S3} is discharged to zero voltage. Since $i_{S3}(t_5)<0$, the anti-parallel diode of S_3 conducts. Thus, S_3 can be turned on at this moment under ZVS. The voltages $v_{ab}=-V_{in}/2$ and $v_{ac}=-V_{in}/4$. D_2 and D_4 are both conducting to commutate the output inductor current i_{Lo}. Since D_2 and D_4 are conducting, it is possible to derive that the secondary winding voltages of T_1 and T_2 are $v_{T2,s}=-0.5v_{T1,s}$. The secondary winding voltage $v_{T1,p}(t_5)$ is approximately equal to $-V_{in}/2-I_o\delta T_s/(2C_r n_1)$. Thus, the primary winding voltage of $v_{T2,p}$ at time t_5 can be given as:

$$v_{T2,p}(t_5)=\frac{n_2V_{in}}{4n_1}+\frac{n_2I_o\delta T_s}{4n_1^2C_r} \tag{11}$$

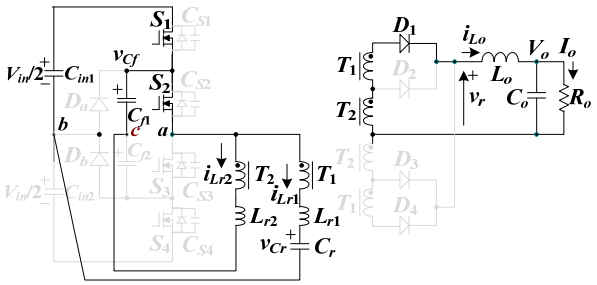
The primary current i_{Lr2} in this stage is decreased and is expressed as:

$$i_{Lr2}(t)=n_2I_o-\frac{\frac{V_{in}}{4}+\frac{n_2V_{in}}{4n_1}+\frac{n_2I_o\delta T_s}{4n_1^2C_r}}{L_{r2}}(t-t_5) \tag{12}$$

The primary current i_{Lr1} is decreased from zero to $-n_1I_o$, and the primary current i_{Lr2} is also decreased from n_2I_o to $-n_2I_o$. At time t_6, the diode current i_{D2} is decreased to zero and only diode D_4 conducts the load current. Then, the circuit operations in the first half switching period are complete.

IV. PARALLEL HYBRID CONVERTER

In order to provide more power to the output load, increase the ripple frequency and reduce the input and output current ripple, a parallel hybrid converter with the interleaved PWM scheme is proposed and its circuit diagram is shown in Fig. 3(a). There are two circuit modules in the proposed parallel hybrid converter. Each circuit module supplies one-half of



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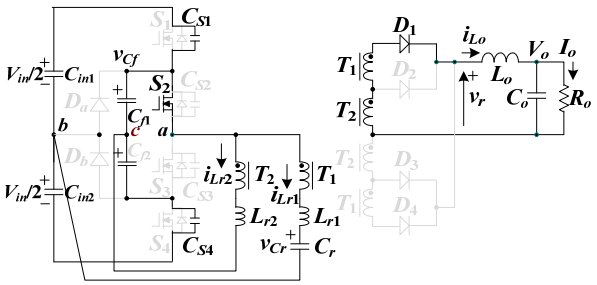

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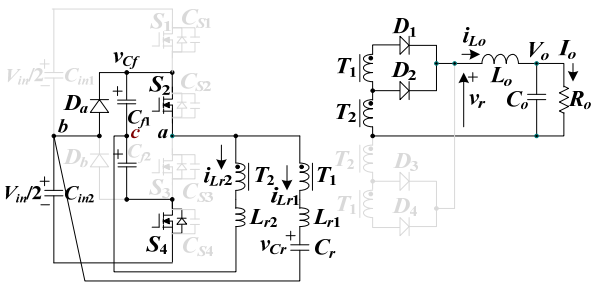

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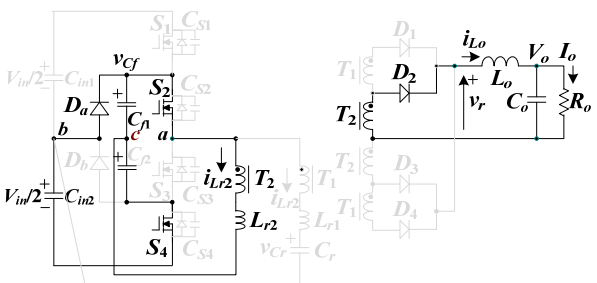

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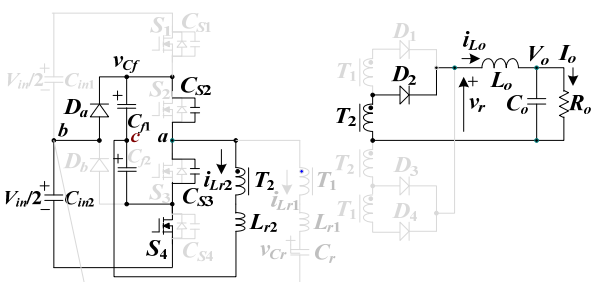

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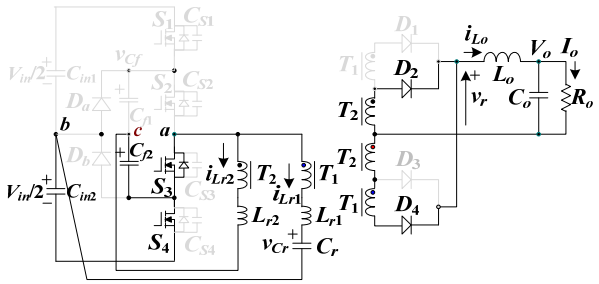


(f)

Fig. 2. Operation modes 1-6 of the proposed converter during the first half switching period (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6.

the rated power to the output load. The interleaved PWM scheme is adopted to generate the necessary gating signals for the power switches. The PWM signals of S_5~S_8 are phase-shifted by one-fourth of a switching period with respective to the PWM signals of S_1~S_4. In each of the circuit modules, the phase-shift PWM scheme is used to control the necessary duty cycle on the primary side and to regulate the output voltage. Fig. 3(b) shows the key PWM waveforms of the proposed parallel hybrid converter during one switching period. The PWM waveforms of the two circuit modules are similar and they are phase-shifted with one-fourth of a switching period. The circuit operations of each circuit module were discussed in the previous section. The main advantages of the interleaved PWM operation of the proposed parallel converter include less current ripple at the output side, double the switching frequency, and less the current stress of the passive components at the high current side. The circuit components of the two modules are identical and the duty cycle of each circuit module is the same due to the controller. Thus, current sharing of each circuit module can be achieved. Even if the circuit parameters of each module have some variation, the output inductor currents are almost balanced.

V. CONVERTER PERFORMANCE ANALYSIS

Since the duration periods of stages 2, 3 and 5 are very narrow when compared to the periods of the other stages, only stages 1, 4 and 6 are considered to derive the DC voltage gain. In stage 6, the rectified voltage $v_{r1} = v_{T2,p}(t_5)$. The duty loss in stage 6 is related to the load current and the resonant inductance L_{r2}. This duty loss δ_6 exists in the conventional three-level converter and the proposed converter. The average rectified voltage V_r in stage 1 is approximately equal to $V_{in}/(2n_1)+V_{in}/(4n_2)$ with the time interval $\delta_{eff}T_s$, where $\delta_{eff}=\delta-\delta_6$. In stage 4, the average rectified voltage V_r is equal to $V_{in}/(4n_2)$ with the time interval $(0.5-\delta_{eff})T_s$. The flux balance on the output inductor L_o can derive the output voltage V_o.

$$V_o = (\delta_{eff} + \frac{n_1}{4n_2})\frac{V_{in}}{n_1} \quad (13)$$

However, the output voltage of the conventional three-level converter is expressed as:

$$V_o = \frac{(2\delta_{eff}) \times (V_{in}/2)}{n} = \frac{\delta_{eff} V_{in}}{n} \quad (14)$$

where n is the turns ratio of the conventional three-level PWM converter. Based on (13) and (14), a comparison of the normalized voltage conversion ratios of the proposed converter and the conventional three-level converter is given as:

$$\frac{M_{proposed}(\delta_{eff})}{M_{conventioanl}(\delta_{eff})} = \frac{\frac{n_1 V_o}{V_{in}}}{\frac{n V_o}{V_{in}}} = \frac{\delta_{eff} + \frac{n_1}{4n_2}}{\delta_{eff}} \geq 1 \quad (15)$$

From (15), the proposed converter has a higher voltage gain compared to the conventional three-level converter. The turns ratio n_1 of the proposed converter can be larger than that in the conventional three-level converter with the same effective duty ratio. The larger turns ratio n_1 will decrease the conduction losses and also reduce the voltage stress of the rectifier diodes. The power ratings and power percentage of the three-level converter and half-bridge converter in the proposed circuit are given as:

$$P_{three-level} = \frac{\delta_{eff} V_{in} I_o}{n_1} \quad (16)$$

$$P_{half-bridge} = \frac{V_{in} I_o}{4n_2} \quad (17)$$

$$\eta_{three-level} = \frac{\delta_{eff}}{\delta_{eff} + n_1/4n_2} \quad (18)$$

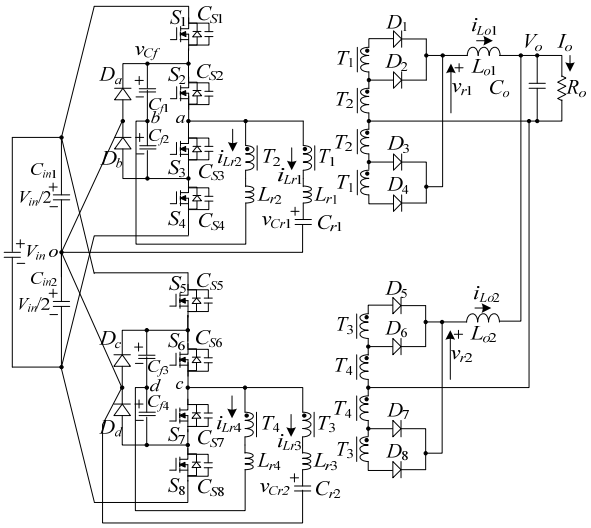
$$\eta_{half-bridge} = \frac{n_1/4n_2}{\delta_{eff} + n_1/4n_2} \quad (19)$$

It can be seen that most of the load power is delivered by the half-bridge converter at a low effective duty cycle. In Fig. 3, the voltage stress of the rectifier diodes can be approximately obtained if the voltage spike on the diodes is neglected.

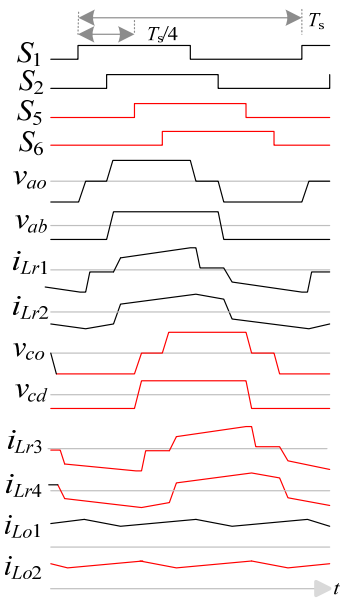
$$v_{stress,D1} = v_{stress,D4} > \frac{V_o}{\delta_{eff} + \frac{n_1}{4n_2}}(1 + \frac{n_1}{2n_2}) \quad (20)$$

$$v_{stress,D2} = v_{stress,D3} > \frac{V_o}{2(\delta_{eff} + \frac{n_1}{4n_2})}(1 + \frac{n_1}{n_2}) \quad (21)$$

In the conventional three-level converter, the voltage stress of the rectifier diodes is $v_{stress,D,conventional} > V_o/\delta_{eff}$. Therefore, the voltage stress of the rectifier diodes in the proposed converter in (20) and (21) is less than the voltage stress in the conventional three-level converter with the same duty ratio. During the freewheeling interval in stage 4, the output inductor voltage v_{Lo} is equal to $V_{in}/(4n_2)$-V_o with the duration



(a)



(b)

Fig. 3. Proposed parallel hybrid converter (a) circuit diagram (b) main PWM waveforms.

period (0.5-δ_{eff})T_s. Thus, the output inductor value can be derived as:

$$L_{o,proposed} > \frac{V_o - \frac{V_{in}}{4n_2}}{\Delta i_{Lo}}(0.5 - \delta_{eff})T_s \quad (22)$$

Based on (13) and (22), the necessary output inductance L_o is expressed as:

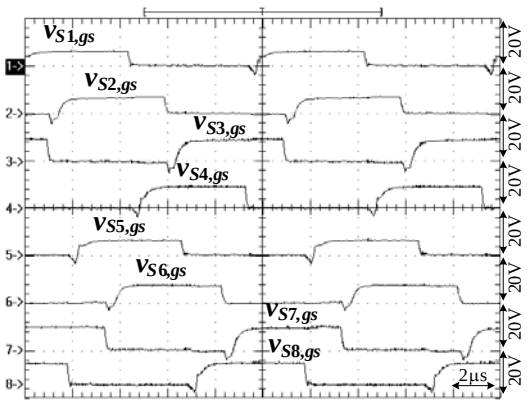
$$L_{o,proposed} > \frac{V_o}{\Delta i_{Lo}} \times \frac{4n_2\delta_{eff}}{n_1 + 4n_2\delta_{eff}}(0.5 - \delta_{eff})T_s \quad (23)$$

In the conventional three-level converter, the output inductance is given as:

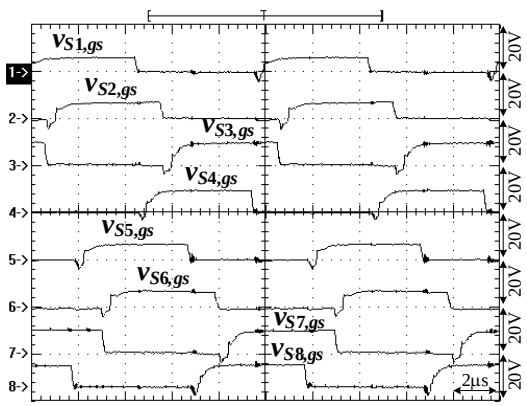
$$L_{o,conventional} > \frac{V_o}{\Delta i_{Lo}}(0.5 - \delta_{eff})T_s \quad (24)$$

(a) (b)

Fig. 4. Photograph of the prototype circuit (a) analog control board (b) main power circuit.



(a)



(b)

Fig. 5. Measured PWM waveforms of S_1~S_8) at (a) P_o=960W (50% load) (b) P_o=1920W (100% load).

The output inductance ratio between the proposed converter and the conventional three-level converter is given as:

$$\frac{L_{o,\,proposed}}{L_{o,\,conventional}} = \frac{4n_2\delta_{eff}}{n_1 + 4n_2\delta_{eff}} < 1 \qquad (25)$$

This means that the proposed converter has less output inductance based on the same current ripple and effective duty cycle.

VI. Experimental Results

The proposed parallel hybrid soft switching DC/DC converter is designed and implemented in this section to confirm the theoretical analysis and to verify the effectiveness of the proposed converter. In the proposed converter, the input voltage V_{in} is from 750V to 800V. The output voltage V_o is 48V and the rated load current $I_{o,max}$ is 40A. The switching frequency of the active switches is 100kHz. The two circuit modules are operated with the interleaved phase-shift PWM scheme. Each circuit module provides one-half of the load current to the output load, *i.e.* I_{Lo1}=I_{Lo2}=$I_{o,max}$/2=20A. IRFP460 MOSFETs were used for switches S_1~S_8. VF30200C and MUR860 fast recovery diodes were used for D_1~D_8 and D_a~D_d, respectively. The input split capacitances C_{in1} and C_{in2} are 360μF. The flying capacitances C_{f1}~C_{f4} are 1μF. The resonant capacitances C_{r1} and C_{r2} are 18nF. The output capacitance C_o is 4000μF. The turns ratios of T_1 and T_3 are 54 turns: 4 turns: 4 turns. The turns ratios of T_2 and T_4 are 27 turns: 4 turns: 4 turns. The leakage inductances L_{r1} and L_{r3} are 14μH, and the leakage inductances L_{r2} and L_{r4} are 22μH. The output inductances L_{o1} and L_{o2} are 5μH. The ZVS range for all of the switches in the proposed converter is from 25% load to full load. Fig. 4 shows a photograph of the proposed converter. The gate voltages of S_1~S_8 for different load conditions and an 800V input voltage are shown in Fig. 5. The PWM signals of S_5~S_8 are phase-shifted one-fourth of a switching period with respect to the PWM signals of S_1~S_4. Fig. 6 shows the measured gate voltage and drain voltage of switches S_1~S_8 at a 25% load. It is clear that all of the switches are turned on under ZVS from a 25% load. Figs. 7 and 8 show the primary side voltages and currents of the proposed converter at a 50% load and a 100% load, respectively. There are three voltage levels on the voltages v_{ao} and v_{co} and two voltage levels on the voltages v_{ab} and v_{cd}. The circulating currents i_{Lr1} and i_{Lr3} of the three-level converters are all reduced to zero in the freewheeling state (v_{ab}=v_{cd}=0). Therefore, the conduction losses on the primary side in the freewheeling state are reduced. The primary currents i_{Lr3} and i_{Lr4} of circuit module 2 are phase shifted with respectively to the primary currents i_{Lr1} and i_{Lr2} of circuit module 1, respectively. Fig. 9 shows the measured results of the secondary side voltage and currents of circuit module 1 at full load. It can be seen that diodes D_2 and D_3 are conducting during the freewheeling interval. Fig. 10 shows the measured waveforms of the output inductor currents at a 100% load. The output inductor current i_{Lo2} is phase shifted to the output inductor current i_{Lo1}. It is clear that the resulting output current ripple $\Delta(i_{Lo1}+i_{Lo2})$ is less than the inductor ripple currents Δi_{Lo1} and Δi_{Lo2} due to the interleaved PWM scheme. The measured circuit efficiencies of the proposed converter are 93.5%, 95.7% and 93.3% at a 25% load, a 50% load and a 100% load, respectively. However, the measured circuit efficiencies of the conventional three-level converter under the same power ratings are 91.9%, 93.4% and 92.1% at a 25% load, a 50% load and a 100% load, respectively. Based on the measured results, it is clear that the proposed converter has better circuit efficiency compared to the conventional three-level converter.

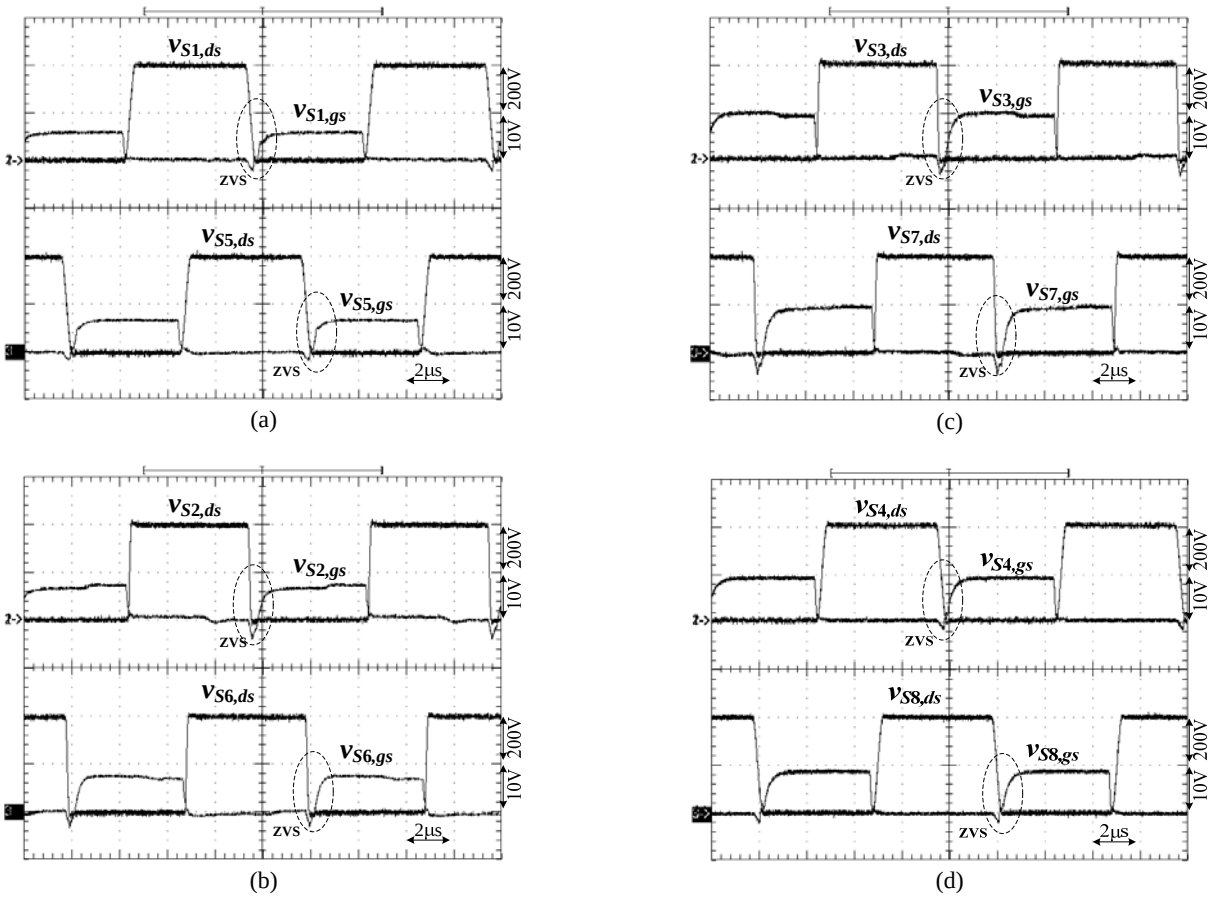


Fig. 6. Measured gate and drain voltages of S_1~S_8 at 25% load (a) S_1 and S_5 (b) S_2 and S_6 (c) S_3 and S_7 (d) S_4 and S_8.

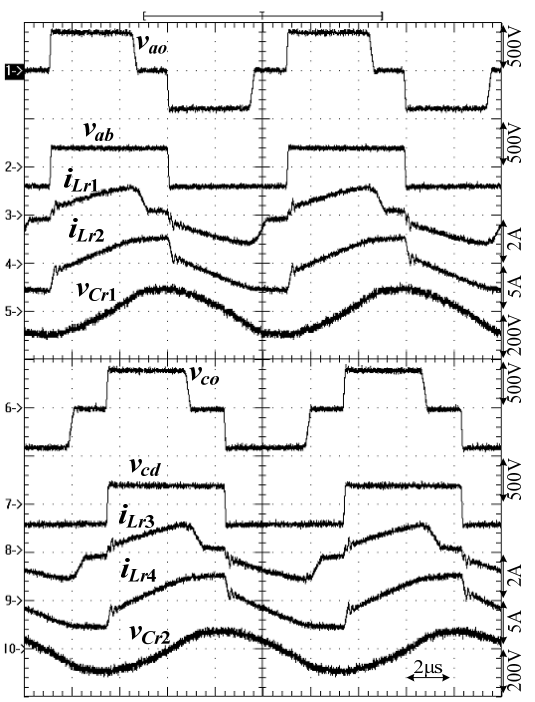


Fig. 7. Measured primary side voltage and current waveforms at 50% load (P_o=960W).

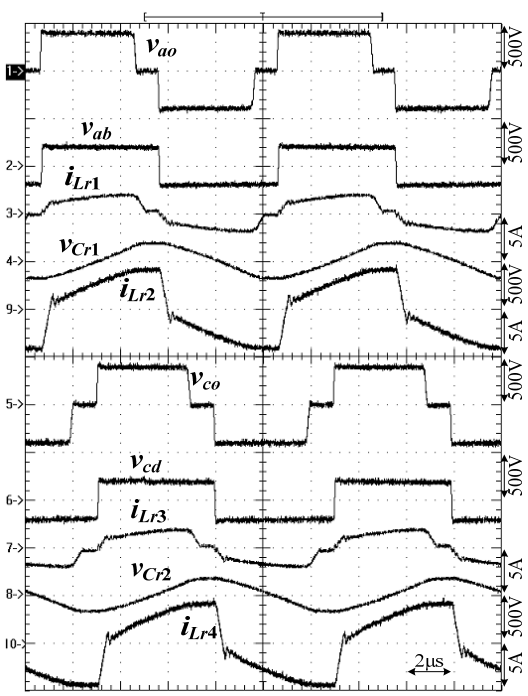


Fig. 8. Measured primary side voltage and current waveforms at full load (P_o=1920W).

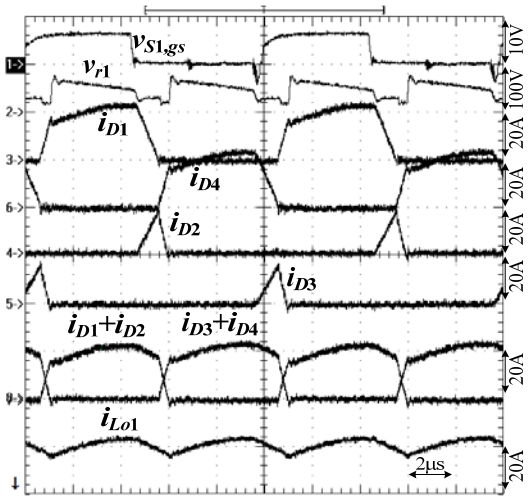


Fig. 9. Measured secondary side voltage and current waveforms of circuit module 1 at full load (P_o=1920W).

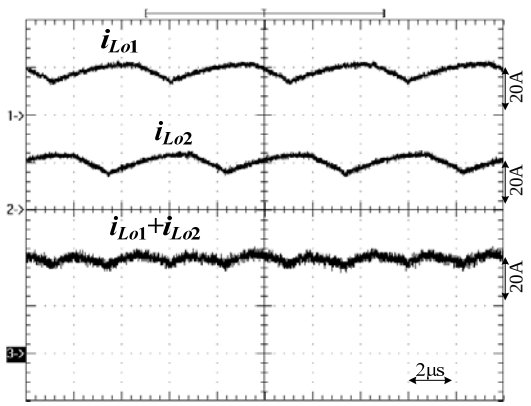


Fig. 10. Measured output inductor currents at full load (P_o=1920W).

VII. CONCLUSION

A new parallel hybrid soft switching converter is presented for medium voltage and power applications. Two circuit modules operated with the interleaved PWM scheme are used in the proposed converter to lessen the current stresses of the active and passive components and to reduce the input and output current ripples. In each circuit module, one three-level converter and one half-bridge converter sharing the lagging-leg switch are used to achieve a wide ZVS range for all of the switches, a low circulating current on the primary side, and less output inductor current ripple. Therefore, the circuit efficiency in the proposed converter is higher than the circuit efficiency in the conventional three-level converter. The circuit configuration, operation principles and circuit characteristics are discussed in detail. Experimental results based on a 1920W prototype confirm the effectiveness of the proposed converter.

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Bor-Ren Lin received his B.S. degree in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, and his M.S. and Ph.D. degrees in Electrical Engineering from the University of Missouri, Columbia, MO, USA, in 1990 and 1993, respectively. From 1991 to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Distinguished Professor. He is an Associate Editor of the *Institution of Engineering and Technology Proceedings—Power Electronics.* His current research interests include power-factor correction, multilevel converters, active power filters, and soft-switching converters. He has authored more than 200 published technical journal papers in the area of power electronics. Dr. Lin is an Associate Editor of the *IEEE Transactions on Industrial Electronics.* He was a recipient of Research Excellence Awards in 2004, 2005, 2007 and 2011 from the College of Engineering and the National Yunlin University of Science and Technology. He received Best Paper Awards from the 2007 and 2011 IEEE Conference on Industrial Electronics and Applications (ICIEA), the 2007 Taiwan Power Electronics Conference, the 2009 IEEE–Power Electronics and Drive Systems Conference (PEDS), the 2012 Taiwan Electric Power Engineering Conference, and the 2014 IEEE-International Conference on Industrial Technology (ICIT).

Jia-Sheng Chen is currently working toward his M.S. degree in Electrical Engineering at the National Yunlin University of Science and Technology, Yunlin, Taiwan (ROC). His current research interests include the design and analysis of power factor correction techniques, switching mode power supplies and soft switching converters.