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A New Symmetric Multilevel Inverter Topology Using Single and Double Source Sub-Multilevel Inverters

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Abstract

In recent years, the multilevel converters have been given more attention due to their modularity, reliability, failure management and multi stepped output waveform with less total harmonic distortion. This paper presents a novel symmetric multilevel inverter topology with reduced switching components to generate a high quality stepped sinusoidal voltage waveform. The series and parallel combinations of switches in the proposed topology reduce the total number of conducting switches in each level of output voltages. In addition, a comparison between the proposed topology with another topology from the literature is presented. To verify the proposed topology, the computer based simulation model is developed using MATLAB/Simulink and experimentally with a prototype model results are then compared.

Key words: DC-AC power conversion, Multi-level power converters, Power semiconductor devices, Renewable energy, Total Harmonic Distortion (THD)

I. INTRODUCTION

The demand for Energy keeps on increasing and the supply of non-renewable energy sources continues decreasing day-to-day. The best way to face these problems is by the use of renewable energy sources with the help of power electronics devices. Power electronic devices help to build power converters. This grabbed the attention of researchers to focus on power electronics converters to develop more topologies, especially in DC/AC power modulators with higher efficiency and a high quality output. This paved way for multilevel converters to predominant usage in medium and high power applications [1]. To improve the performance of multilevel converters, the experts are developing new converter topologies, novel modulation techniques and improved control techniques for various applications. Multilevel inverters can provide higher power handling capability while considering a high power conversion process [2]. For multilevel inverters, fault tolerance can be achieved by bypassing the faulty devices and/or modules while the switching patterns of the rest of the modules can be reconfigured to a new normal condition [3]. The conventional multilevel inverters are: (i) Diode Clamped; its required single dc source with multiple capacitors are connected parallel to equally share the dc voltage. The diode clamp is very suitable for higher voltage applications since the single dc source is divided into several dc sources via a capacitor. The main challenge of these topologies is the larger number of clamped diodes for which the capacitor balancing requires an additional circuit. (ii) Flying Capacitor (FC); a clamping capacitor is used, a larger number of storage capacitors is required, and maintaining the voltage of each capacitor is difficult. (iii) Cascaded H-Bridge (CHB); this is a series of cascaded connections of H-bridge or full bridge inverters. It does not require any clamping capacitor or diode and it has great modularity and fault tolerance. The main drawback of CHB is the requirement of isolated dc sources. However, these conventional multilevel inverter topologies are used by employing a larger number of power switches for a higher number of output voltage levels [4]. To rectify this

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problem, many topologies are presented [5]-[15]. A new asymmetric topology was proposed in [5]. In this topology, a power switch with an anti-parallel diode will create an inter-looping current circulation. To avoid this, the combination of MOSFET and IGBT is proposed. A new attempt was made [6] with reduced number of switches for both symmetric and asymmetric topologies. In this topology, the symmetric method uses different ratings of the switches which leads to different voltage capabilities and increases the maximum voltage capability of the circuit. A new converter topology presented in [7]. In this topology, the power circuit complexity is reduced with the help of auxiliary switches. In addition, this topology may require bidirectional switches. In [8], a cascaded connection of power cells proposed with a minimum number of switches when compared to conventional CHB. Even then, it requires a larger number of power switches. Some other topologies are presented in the literature which is mainly focused on reducing the power switches [9]-[11]. Even though these topologies suffer from a higher number of power diodes and capacitors. A combination of two or more conventional or new topologies can be referred to as a hybrid. Hybrid topologies have some significance advantages to reduce the switching losses and improve the converter efficiency. Hybrid modulations for cascaded converters have been proposed. This allows for the use of a lower switching frequency in higher voltage cells, and a higher switching frequency in lower voltage cells. By using hybrid modulation techniques, the medium and high power applications are strengthened. Both high and low switching frequencies are used to generate a higher number of voltage levels and to strengthen medium and high power applications. The hybrid method's drawback is the requirement of different voltage ratings of the power switches [12]. A recent topology has been introduced with an even number of dc sources in [13]. It consists of both double voltage ratings and bidirectional switches which may further increase the power electronic devices. In this paper, a new approach to reduce the number of power switches and gate driver circuits by using the double voltage ratings of power switches to obtain a synthesized stepped waveform is discussed.

II. PROPOSED TOPOLOGY

In this section, detailed explanations of two different basic structures of proposed topology are introduced and mathematical expressions for a number of voltages level (N_{level}), number of switches (N_{switch}) and number of dc source voltages (n) are presented.

A. Suggested Topology

A basic single dc source with series/parallel unit is explained in Fig.1(a). The dc source E_1 is connected in series with switch S_1 and in parallel with switch P_1. This basic unit

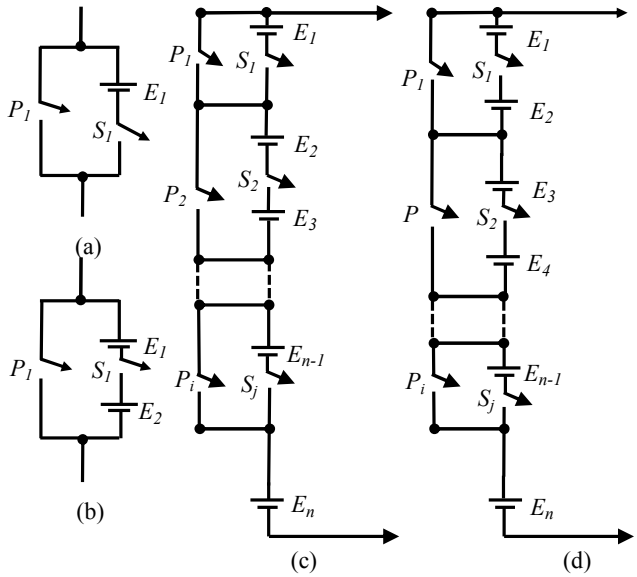

Fig. 1. Proposed Symmetric Topology. (a) Basic single source sub multilevel inverter (SSSMLI). (b) Basic double source sub multilevel inverter (DSSMLI). (c) Generalized structure for odd number of sources. (d) Generalized structure for even number of sources.

is called a Single Source Sub Multilevel Inverter (*SSSMLI*). Fig.1(b) shows the series/parallel connection of power switches along with two dc sources. The E_1 & E_2 dc sources are connected in series with S_1 and in parallel with P_1. This is often referred to as a Double Source Sub Multilevel Inverter (*DSSMLI*). In both the cases, the switches should not be turned on simultaneously to avoid a short circuit of the dc source. The proposed topology is separated into two units: (i) a combined single and double source sub multilevel inverter which is called a level generator unit and (ii) a series connection of the level generator with an H-Bridge inverter which is called a polarity changer. The series connection of dc sources with switches is called a voltage adder, and the parallel connection of switches is called a voltage subtractor. The combination of both a single source unit and a double source unit is connected in series to form a level generator as shown in Fig. 1(c) and Fig 1(d). In this proposed topology, both the even source and odd source have separate generalized structures as shown in Fig. 1.

This topology requires multiple dc sources, which may be available through renewable energy sources such as photovoltaic panels or Fuel cells or through energy storage devices such as capacitors. "n" is the number of dc source voltages, which are separated with series connected unidirectional controlled power switches (S_1, S_2, S_3....S_j). In addition, each unit has parallel switches (P_1, P_2, P_3.... P_i). The n^{th} E is represented as E_n. In the proposed method, E_n is not connected with any parallel switches. Table I illustrates the switching pattern for n dc sources. The 1's and 0's represents the turn on and turn off switches. The

corresponding switches will be fired to synthesize a positive stepped waveform in the level generator. The adder/subtractor unit is connected in sequence with the H-bridge, which is used to create a current flow in both directions at the load terminals. Fig. 1(c) and Fig. 1(d) show the generalized structure of the new symmetrical topology proposed for N_{Level} with equal magnitudes of the dc source voltages *(E)*. The proposed symmetric topology is used in order to provide a larger number of output voltage steps with a minimum number of switches. Generally, the difference is presented in [14], the proposed topology in each dc source is constructed with a pair of series/parallel switches. However, in this case, any two dc source voltages can be connected with one parallel switch, which may increase the voltage ratings of the switches. Here worth mentioning that the number of switches is getting reduced. According to Fig. 1, the IGBTs of (S_1, P_1), (S_2, P_2) · · · · · (S_j, P_i) turn on simultaneously and $E_1, E_2 \ldots E_{n-1}$ will be short circuited with the same dc source. Either one of the corresponding adder/subtractor switches will turn on or turn off as per Table I. The maximum output voltage $(E_{o,max})$ is the sum of all the dc source voltages, and it is given as below:

$$E_{o,max} = E_1 + E_2 + E_3 + \cdots\cdots + E_n \tag{1}$$

$$E_{o,max} = \sum_{i=1}^{n} E_n \tag{2}$$

Equations (1) and (2) illustrate the output level of the adder/subtraction circuit. Both the positive and negative levels are synthesized by the H-bridge circuit. At load $(V_{o,Load})$, the synthesized stepped output voltage level will be obtained as mentioned below:

$$E_{o,max} = \begin{cases} \sum_{i=1}^{n} + E_i & ,H_{S1}, H_{S4} = 1 \\ \sum_{i=1}^{n} - E_i & ,H_{S2}, H_{S3} = 1 \end{cases} \tag{3}$$

In proposed topology, the number of output voltage levels (N_{Level}), the number of IGBTs (N_{IGBT}) and the number of dc sources (n) are calculated as follows:

$$N_{level} = 2n + 1 \tag{4}$$

$$n = \frac{N_{level} + 1}{2} \tag{5}$$

The proposed topology structure varies with odd and even numbers of dc sources. Therefore, it is necessary to express the required number of IGBTs for given output levels and for a given number of dc sources. This is calculated in equation (6) and (7).

$$N_{IGBT} = \begin{cases} \frac{N_{level} + 9}{2} & ,n = odd \\ \frac{N_{level} + 7}{2} & ,n = even \end{cases} \tag{6}$$

TABLE I
GENERALIZED SWITCHING PATTERN FOR PROPOSED TOPOLOGY

State	Voltage Subtractor Switches						Voltage Adder Switches						Voltage Levels ($E_{O,MAX}$)
	P_1	P_2	P_3	…	P_{i-k}	P_i	S_1	S_2	· · ·	S_{j-k}	· · ·	S_{j-1} S_j	
1	1	1	1	…	1	1	0	0	· · ·	0	· · ·	0	0	E_n
2	0	1	1	…	1	1	1	0	· · ·	0	· · ·	1	0	E_n+E_1
3	1	0	0	…	1	0	0	1	· · ·	0	· · ·	0	1	$E_n+E_{n-1}+E_1$
4	1	1	0	…	0	0	0	0	· · ·	1	· · ·	1	1	$E_1+E_n+E_2+E_3$
…	·	·	·	…	·	·	·	·	· · ·	…	· · ·	·	·	…
n-k	1	0	0	…	0	0	1	1	· · ·	1	· · ·	1	1	$\sum_{i=1}^{n-k} E_{n-k}$
…	·	·	·	…	·	·	·	·	· · ·	…	· · ·	·	·	…
n-1	1	0	0	…	0	0	0	1	· · ·	1	· · ·	1	1	$\sum_{i=1}^{n-1} E_{n-1}$
n^{th} State	0	0	0	…	0	0	1	1	· · ·	1	· · ·	1	1	$\sum_{i=1}^{n} E_n$

$$N_{IGBT} = \begin{cases} n + 5 & ,n = odd \\ n + 4 & ,n = even \end{cases} \tag{7}$$

The determination of the required number of single and double source sub multilevel inverters is calculated based on a given n of dc sources as follows:

For even number of *n*:

$$DSSMLI = \frac{n - 2}{2} \tag{8}$$

$$SSSMLI = 1 \tag{9}$$

For Odd number of *n*:

$$DSSMLI = \frac{n - 3}{2} \tag{10}$$

$$SSSMLI = 2 \tag{11}$$

The operating modes for the 9-level inverter, explained diagrammatically for both the positive and negative cycles, is depicted in Fig.2. The switches P_1 and P_2 are turned on to produce the first level output from either (H_{S1}, H_{S4}) or (H_{S2}, H_{S3}). This is done to generate the corresponding polarity output. A similar sequence will continue to obtain the remaining levels as per the switching pattern in Table I.

B. Peak Inverse Voltage (PIV) Calculation

To choose an appropriate IGBT, the individual switch peak inverse voltages should be taken into account. Voltage stress, also known as the standing voltage of the switches, can be calculated by using the following expression:

$$E_{PIV} = \begin{cases} 2E & for\ S_2 \cdots S_{j-1}\ \&\ P_2 \cdots P_{i-1} - odd \\ 2E & for\ S_1 \cdots S_{j-1}\ \&\ P_1 \cdots P_{i-1} - even \\ E & for\ S_1, S_j\ \&\ P_1, P_i - odd \\ E & for\ S_j\ \&\ P_i - even \\ \sum_{i=1}^{n} E_i & for\ H - Bridge\ switches \\ & where\ i = 1,2,3.....n \end{cases} \tag{12}$$

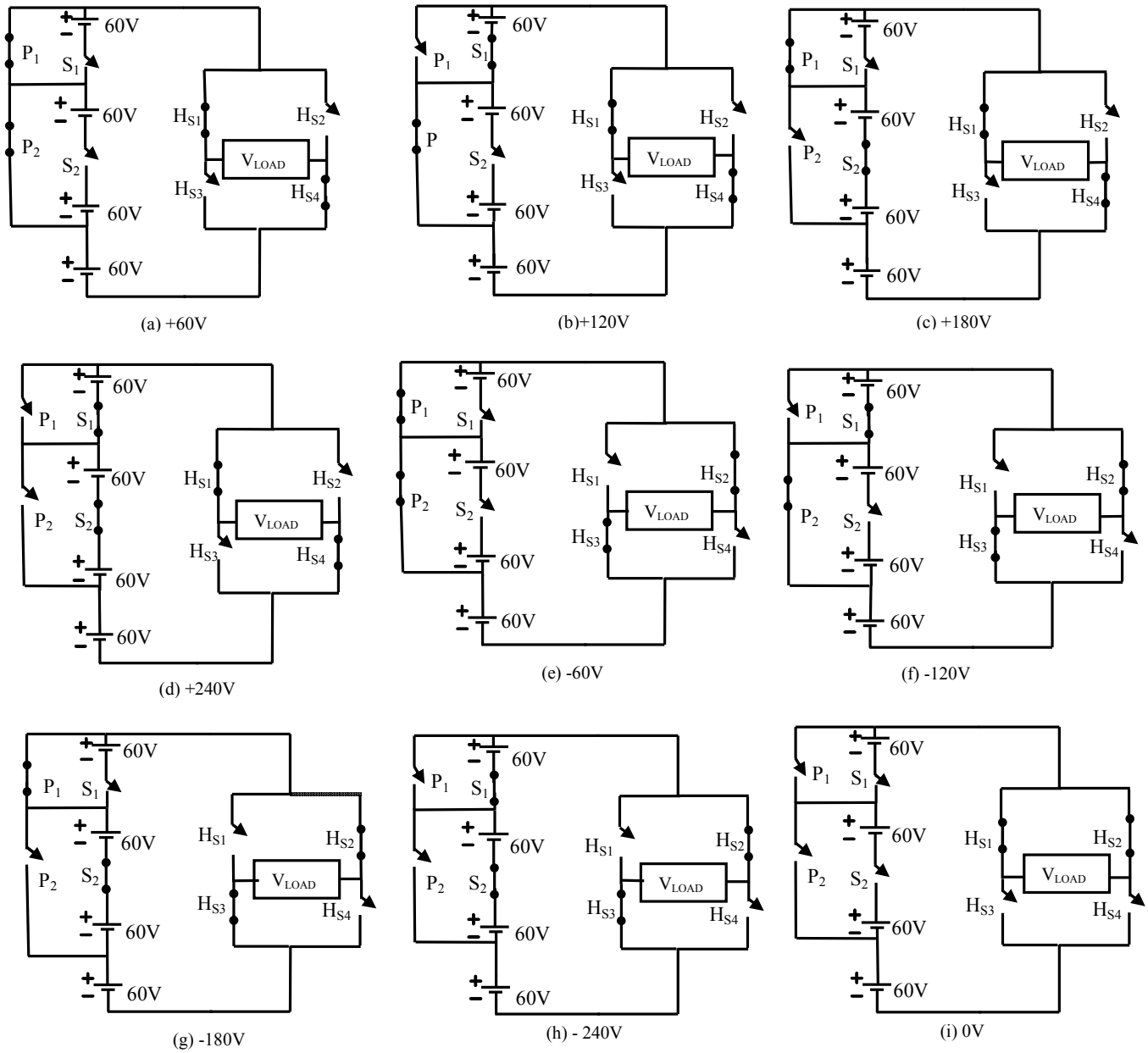

Fig. 2. Different operating mode of proposed symmetric topology for 9-level inverter.

C. Blocking Voltage Capability (E_{BLOCK})

One of the most important parameters of a multilevel inverter is to determine the maximum blocking voltage capability of the power switches. A *SSSMLI* switch requires the maximum blocking voltage of the single dc source magnitude *(E)*. In a *DSSMLI*, a maximum of two dc source magnitude switches is required *2E*. As shown in Fig. 1(c), the blocking voltages of S_1, $S_2 \ldots S_j$, and P_1, $P_2 \ldots P_i$ are calculated as follows. In the symmetric method, all of the dc source voltages are considered to be equal values so that $E=E_1=E_2=E_3 \ldots \ldots =E_n$. The different voltage ratings of the level generator switches are as follows:

$$E=\begin{cases} S_1 = S_j = P_1 = P_i & \textit{for} \text{ odd source} \\ \mathrm{S_j} = P_i & \textit{for} \text{ even source} \end{cases}$$

$$2\times E=\begin{cases} S_2 \cdots S_{j-1} = P_2 \cdots P_{i-1} & \textit{for} \text{ odd source} \\ \mathrm{S_1} \cdots S_{j-1} = P_1 \cdots P_{i-1} & \textit{for} \text{ even source} \end{cases}$$

The level generator and polarity changer blocking voltage capability are as follows:

$$E_{B1}=\begin{cases} S_1 + S_j + P_1 + P_j & \text{for odd source} \\ \mathrm{S_j} + P_i & \text{for even source} \end{cases}$$

$$E_{B2}=\begin{cases} S_2 + \cdots + S_{j-1} + P_2 + \cdots + P_{i-1} & \text{for odd sourcee} \\ \mathrm{S_1} + \cdots + S_{j-1} + P_1 + \cdots + P_{i-1} & \textit{for} \text{ even source} \end{cases}$$

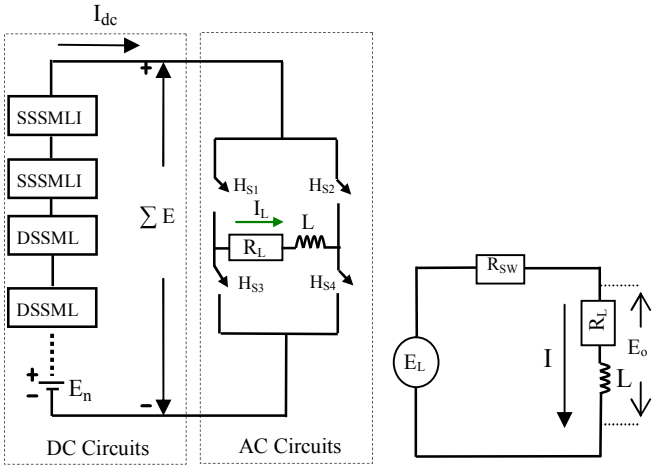

Fig. 3. (a) Topology of single Phase SDSSMLI. (b) Simplified Circuit for State space Model.

$$H_{S1} = H_{S2} = H_{S3} = H_{S4} = 4 * n$$

$$E_{BH} = H_{S1} + H_{S2} + H_{S3} + H_{S4}$$

The total blocking voltage can be calculated as follows:

$$E_{BLOCK} = E_{B1} + E_{B2} + E_{BH} \tag{13}$$

$$E_{BLOCK} = (6n - 2)\,E \tag{14}$$

Where, E_{B1}, E_{B2}, E_{BH} and E_{BLOCK} are the maximum blocking voltages of the E and $2E$ switches, the H-bridge maximum blocking voltage and the total blocking voltage of the inverter, respectively. The determination of the total blocking voltage for the proposed multilevel inverter is expressed in equation (14).

III. State Space Modeling

A state space representation is a mathematical model of a system comprising a set of input, output and state variables. The state space representation provides a convenient and flexible way to model and analyze systems with z number of inputs and outputs. Consider S_1, S_2, S_3, and S_4 be the signals for each level of output to the 9-level inverter for which the series/parallel combinations of switches are influenced. A simplified model for the state space switched modelling for each level of output is shown in Fig.3b. This circuit is applicable for both odd and even numbers of equal dc sources.

Let,

$$H = \begin{cases} 1 & \text{for positive half cycle} \\ -1 & \text{for negative half cycle} \end{cases} \tag{15}$$

The variable H is the realization of the H-Bridge in the proposed topology. Therefore, the net output E_L from the m - level inverter is given by:

$$E_L = \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} G_1H \\ G_2H \\ G_3H \\ G_4H \end{bmatrix} \begin{bmatrix} E_{dc} \end{bmatrix} \tag{16}$$

where, E_{dc} is the magnitude sum of each dc source, and G_1 to G_4 is the comparator output signals (Binary output). By applying KVL to the circuit:

$$E_L = R_{sw} i_L(t) + R_L i_L(t) + L\frac{di_L(t)}{dt} \tag{17}$$

where, $R_L = R + R_{ind}$, and R, R_{ind}, R_{SW}, and L are the total load resistance in ohms, the load resistance in ohms, the internal resistance of a load inductor in ohms, the ON state resistance of the total conducting IGBT's in each level, and the load inductance in mH, respectively. In this topology, in each level, the number of conducting components is the same. Rewriting equation (17) and substituting the value of E_L from equation (16) gives:

$$L\frac{di_L(t)}{dt} = \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} G_1H \\ G_2H \\ G_3H \\ G_4H \end{bmatrix} \begin{bmatrix} E_{dc} \end{bmatrix} - (R_{sw} + R_L) i_L(t) \tag{18}$$

Let the state variable be the current through the inductor $x = i_L(t)$ and input variable $u = E_L$:

$$\frac{di_L(t)}{dt} = \frac{\begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} G_1H \\ G_2H \\ G_3H \\ G_4H \end{bmatrix} \begin{bmatrix} E_{dc} \end{bmatrix} - (R_{sw} + R_L) i_L(t)}{L} \tag{19}$$

where, $\dot{x} = \frac{di_L(t)}{dt}$;

$$A = \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} G_1H & G_2H & G_3H & G_4H \end{bmatrix}^T \quad B = -(R_{sw} + R_L)$$

Similarly, the voltage across the load is given by the expression:

$$E_{out} = R_L i_L(t) + L\frac{di_L(t)}{dt} \tag{20}$$

where $y = E_{out}$; $C = (R_L + L\frac{d}{dt})$; and $D = 0$

In general, the state space switched model of the proposed topology is given by:

$$\frac{di_L(t)}{dt} = \frac{[A][G_1H \quad \cdots \quad G_kH]^T \, [E_{dc}] - (R_{sw} + R_L) i_L(t)}{L} \tag{21}$$

$$E_{out} = R_L i_L(t) + L\frac{di_L(t)}{dt} \tag{22}$$

Where the dimension of $[A] = 1 \times (N_{level} - 1)/2$, k varies from 1 to $(N_{level} - 1)/2$, E_{dc} is the magnitude of each dc source, and $i_L(t)$ is the current through the inductor. The generalized state space switched model is explained in equations (21) and (22) and it is applicable for proposed asymmetric topology with any number of levels. The state space switched model for the proposed topology is sculpted using MATLAB for a RL load of R=5Ω and L=100mH, and the results are as shown in Fig.4 and Fig. 5.

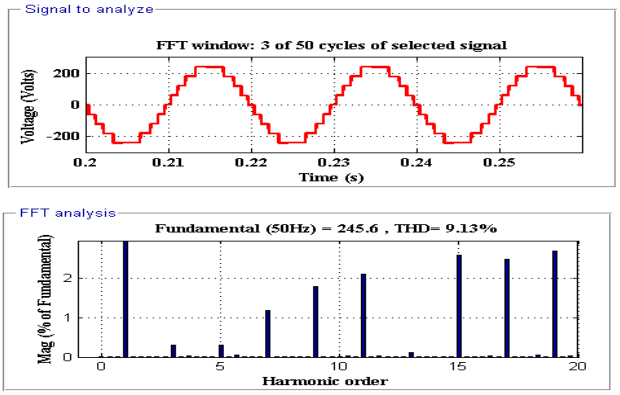

Fig. 4. Simulated State Space Model Voltage waveform.

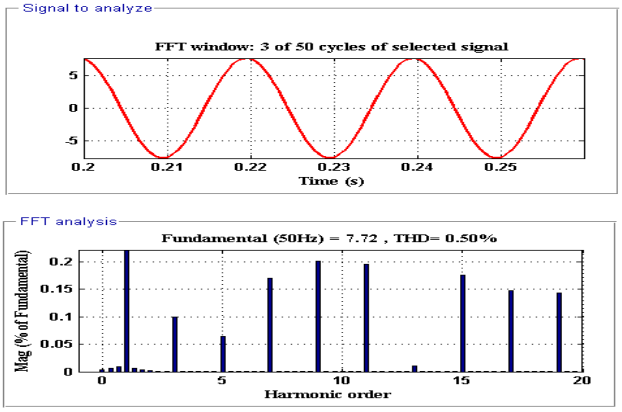

Fig. 5. Simulated State Space Model current waveform.

IV. Comparison with Other Topologies

In order to verify the performance of the proposed topology, it should be compared with other topologies discussed in the literature.

A. Comparison of the Required Number of IGBTs for Symmetric Topologies

The topologies in [6], [8], [13] and [14], generate *2n+1* levels for *n* number of dc sources with an equal magnitude. However, the required number of IGBTs varies for each topology as shown in the comparison chart in Fig.6. In [7] the delta modulation technique is used to generate a stepped waveform with a combination of unidirectional and bidirectional switches. The bidirectional switch may require a power diode or one additional switch leading to an increase in the power electronics component and a reduction in the system modularity. The topologies in [9]-[13] generate a stepped waveform by using *n* dc sources or a single dc source with a multi dc-link capacitor.

These topologies suffer from either an increased number of capacitors or an increased number of power diodes. (i) More attention paid to protect the power diode from failure. The power diode is dissipating a lot of power when conducting current. Due to the stray inductance, large voltage spikes will occur when diode is turned off and reverse recovery is most crucial in a diode with a large reverse blocking voltage rating [16]. (ii) The capacitor accounts for the largest portion of failures in most power converters. However, the useful life of a capacitor is strongly affected by the different operating conditions [17].

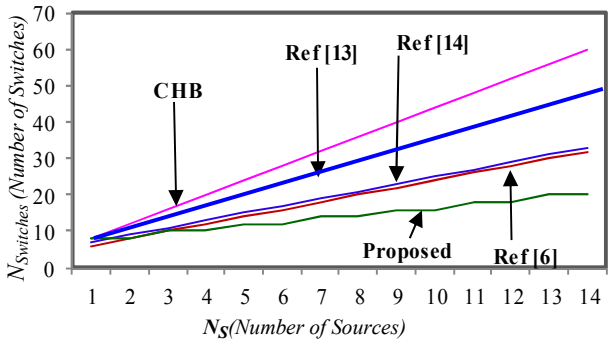

Fig. 6. Comparison with other topologies (a) N_S *vs* $N_{Switches}$.

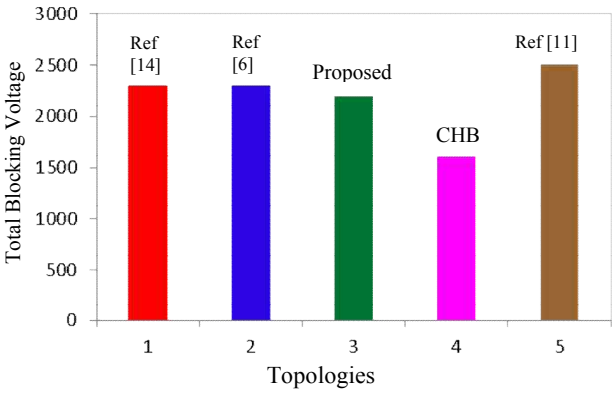

Fig. 7. Comparison of Total Blocking Voltage Capability for various Topologies.

It is obvious that the proposed inverter requires a lower number of IGBTs with a freewheeling diode and no additional diodes are required. The maximum voltage blocking capability decides the reliable operation and the overall cost of the inverter. In Fig. 7, a comparison of the maximum voltage blocking capability of the proposed topology with the other mentioned topologies is illustrated by assuming each of the dc sources is *100V*. The maximum voltage blocking capability of the proposed topology is always lower since the number of the dc source magnitude is increased when compared with the other topologies.

In medium voltage applications, a higher voltage class of H-Bridge switches (H_{S1}, H_{S2}, H_{S3} and H_{S4}) is required, which may significantly increase the blocking voltage of the proposed topology when compared with the CHB. Here it is worth mentioning that the number of power switches is reduced. Fig. 8 illustrates a comparison of the different topologies in terms of the required number power diodes for n number of dc sources.

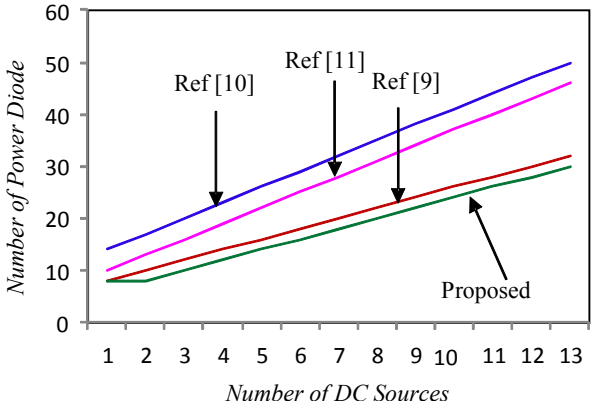

Fig. 8. Comparison of Number of Sources Vs Number of Power Diode.

B. Cost Comparison

The cost of the proposed topology is less when compared with the other topologies presented in the literature and more than the conventional topologies. The different voltage rating of the switch cost is shown in Table III.

The general cost calculation formula is given as:

$$Total\ Cost, K = N_{IGBT} + N_{driver} + N_{dc} + N_{var\,iety} + OC \quad (23)$$

Where, N_{IGBT}, N_{driver}, N_{dc}, $N_{variety,}$ and OC are the cost of the number of IGBTs used in the circuit, the cost of the driver circuits for each IGBT, the cost of 'n' dc sources, the cost of using different varieties of dc sources as in case of the asymmetric MLI and other miscellaneous costs, respectively. The cost of the proposed MLI is less than that presented in [6], [11] and [14] but higher than the CHB. This is due to the fact that the cost of the polarity generator part is significantly increased in the proposed topology. These are the biggest advantage of the CHB. It is evident from Table II that when the voltage rating is doubled with the same current, the cost of the switch is less than normal voltage rating devices. However, the current ratings become high when the double voltage rating switch cost increases. As a result, the proposed topology is very well suitable for medium voltage applications. Although the proposed topology can be cascaded to significantly reduce the cost of the inverter and to increase the high number of voltage levels with a lower number of power switches, this is most suitable for high power applications.

C. Fault Tolerances & Efficiency

The CHB topology has good modularity, which can easily bypass faulty switches [15]. In addition, the CHB topology presents many redundant states for effective fault-tolerant operation. The proposed topology has a very limited number of redundant states for a lower number of dc source voltages, and more redundant states for a higher number of levels. It is important to show the efficiency of the proposed topology because it is the prime factor when a load is considered. The

TABLE II
COST OF IGBT FOR DIFFERENT VOLTAGE AND CURRENT RATINGS

S.No	PART	Rated Voltage [V]	Rated Current [A]	ΔC_1* (USD)
1	FS10R06XL4	600	10	31.55
2	FS15R06XL4	600	15	34.43
3	BSM50GB60DLC	600	50	65.12
4	FF401R17KF6C-B2	1700	400	982.52
5	FS10R12VT3	1200	10	16.38
6	FS15R12VT3	1200	15	17.96
7	BSM50GB120DLC	1200	50	75.64
8	FF400R33KF2C	3300	400	1447.67

*as on 07/05/2014 (http://www.galco.com)

TABLE III
PERFORMANCE OF PROPOSED 9-LEVEL INVERTER ON VARIOUS LOADS

R (Ω)	L (mH)	Vrms, (V)	Irms, (A)	THD (V) %	THD (I) %	Pin (W)	Po (W)	η (%)
55	100	145.31	2.28	9.18	0.98	331.30	288.28	87.01
60	100	145.31	2.14	9.18	1.04	310.96	275.07	88.45
75	100	145.32	1.78	9.18	1.24	258.66	238.54	92.21
90	100	145.32	1.52	9.18	1.44	220.88	208.29	94.29
100	100	145.32	1.38	9.18	1.57	200.54	191.42	95.45
100	90	145.32	1.39	9.18	1.72	201.99	194.75	96.41
100	75	145.32	1.41	9.18	2.00	204.90	199.27	97.25
100	60	145.32	1.42	9.18	2.40	206.35	203.13	98.43

efficiency of any converter is determined by $\eta=(P_{out}/P_{in})*100$. The proposed topology is highly efficient even when inductive types of loads are employed. The efficiency of the proposed structure is tabulated in Table III.

V. SIMULATION AND EXPERIMENTAL RESULTS

To examine the proposed topologies and to generate the desired output voltage level waveforms, 9-Level proposed symmetric multilevel inverter is simulated using the computer simulation tool MATLAB / Simulink. The simulated output voltage and current is shown in Fig. 9 and Fig. 10. They are very much similar to the simulated output voltage and current of the state space model.

In the simulation, each dc source magnitude is 60V with load value **R=5Ω** and **L=100mH.** The nearest voltage level modulation techniques is implied as a modulation method which is preferable for a higher number of voltage steps [18], [19]. A schematic representation of the switching signal generation logic from the given sine reference and comparison constants $(C_1,C_2...C_n)$ is shown in Fig. 11.

The power quality of the proposed topology is measured

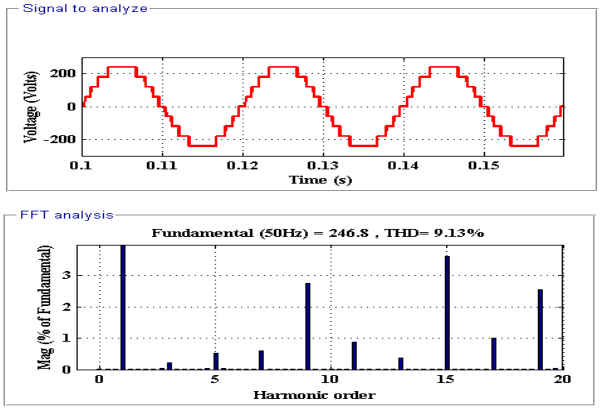

Fig. 9. Simulation output voltage waveform with harmonic spectrum.

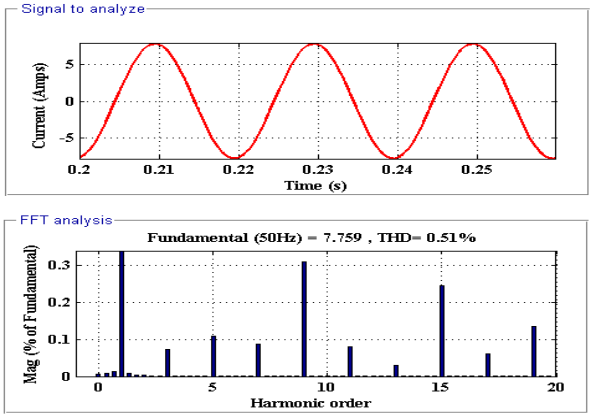

Fig. 10. Simulation output current waveform with harmonic spectrum.

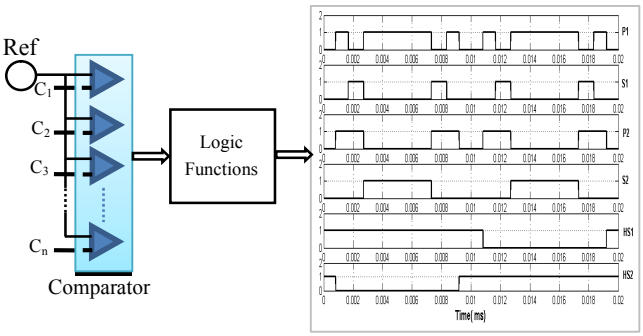

Fig. 11. Switching Signal Generation.

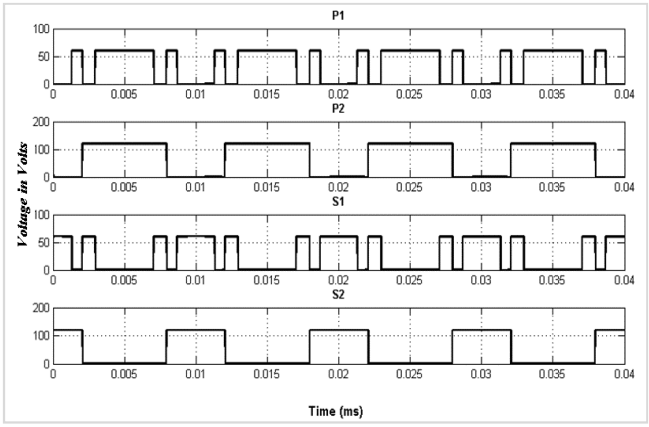

Fig. 12. Voltage across level generator switches.

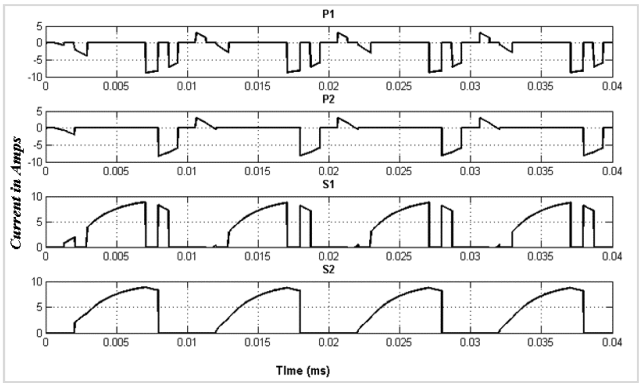

Fig. 13. Current through level generator switches.

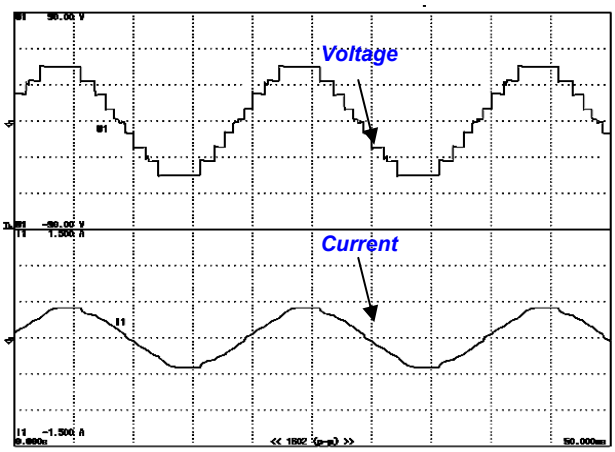

Fig. 14. Experimental output Voltage and Current waveform of 9-level Inverter.

by various parameters as listed in Table III. It is clear from Table III that the efficiency of the proposed topology is higher than the other topologies. Fig. 12 and Fig.13 show the voltage across the level generator switches and the current through the level generator switches. As shown in Fig. 12, the blocking voltage on the S_1,P_1 and S_2,P_2 switches are 60V and 120V, respectively.

In the experimental setup, each dc source has a magnitude of 15V and the load values are **R=100** and **L=100mH**. Based on the load value, the output voltage, current waveform and measured THD is shown in Fig. 14 and Fig. 15. The nearest voltage control technique is embedded into a FPGA Spartan XE3S250E controller. The gate driver circuit switches in the proposed topologies are shown in Fig. 16, which consists of an Opto-coupler, a Schmitt trigger and a buffer. To examine the simulated output voltage and current, the prototype model is developed, as shown in Fig. 17.

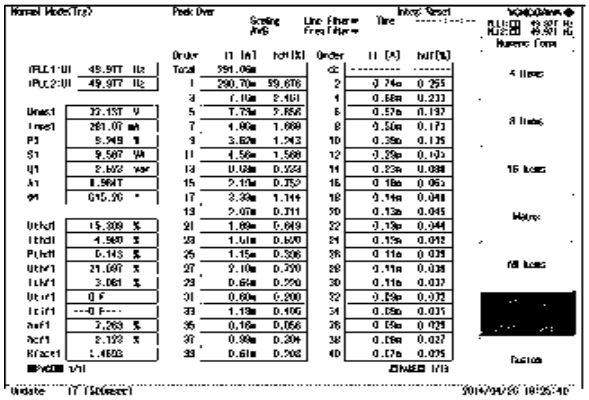

Fig. 15. Experimental Harmonic content of 9-level Proposed Inverter.

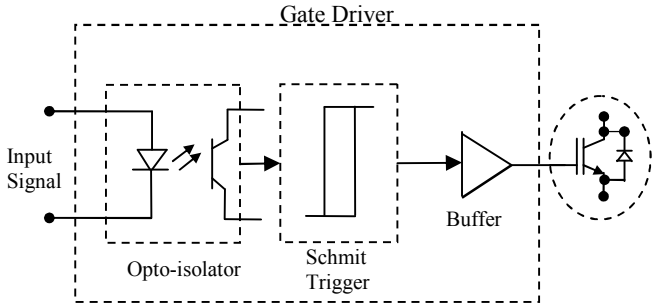

Fig. 16. Gate driver circuit for unidirectional Switch.

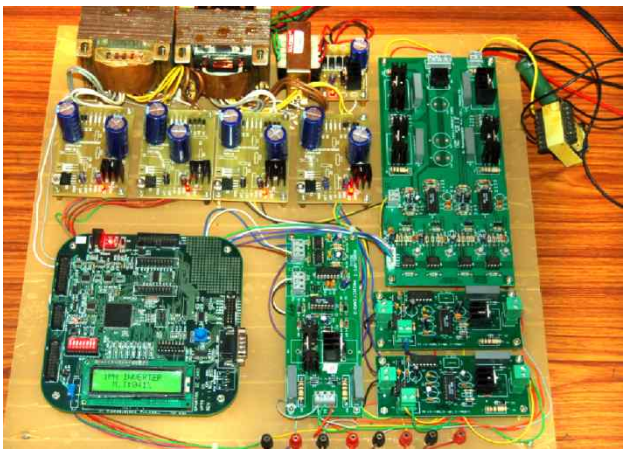

Fig. 17. Experimental Prototype Model.

VI. Conclusions

A new symmetric multilevel inverter has been proposed in this paper. It is a combination of a multi-stepped dc-dc converter (level generator) and an H- bridge inverter (polarity changer). The dc-dc conversion section consists of both single and double source sub multilevel inverters. It has been shown that the proposed inverter provides *2n+1* levels on the output voltage, using only *n* number of dc sources. It enables a simple structure with a reduced number of switches. It also provides a high quality output and a reduced THD. A comparison of the proposed topology with other topologies has been presented in this paper. In order to the performance of the proposed topology, the results of MATLAB simulations of the state space switched model, proposed circuit, and experimental outputs have been presented along with this paper. The improvements in the efficiency, power factor, and THD of the proposed topology are major breakthroughs. This proposed topology is best suited for medium power applications. Future work on this proposed topology should consider: (i). High voltage applications by cascading the proposed topology. (ii). Performance for various modulation techniques. (iii) Use in practical applications such as, induction motor drives and FACTS controllers. (iv). Protection requirements for various applications.

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