JPE 15-1-9

http://dx.doi.org/10.6113/JPE.2015.15.1.86
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

An Active Clamp High Step-Up Boost Converter with a Coupled Inductor

Quanming Luo†, Yang Zhang*, Pengju Sun*, and Luowei Zhou*

†*State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing, China

Abstract

An active clamp high step-up boost converter with a coupled inductor is proposed in this paper. In the proposed strategy, a coupled inductor is adopted to achieve a high voltage gain. The clamp circuit is included to achieve the zero-voltage-switching (ZVS) condition for both the main and clamp switches. A rectifier composed of a capacitor and a diode is added to reduce the voltage stress of the output rectifier diode. As a result, diodes with a low reverse-recovery time and forward voltage-drop can be utilized. Since the voltage stresses of the main and clamp switches are far below the output voltage, low-voltage-rated MOSFETs can be adopted to reduce conduction losses. Moreover, the reverse-recovery losses of the diodes are reduced due to the inherent leakage inductance of the coupled inductor. Therefore, high efficiency can be expected. Firstly, the derivation of the proposed converter is given and the operation analysis is described. Then, a steady-state performance analysis of the proposed converter is analyzed in detail. Finally, a 250 W prototype is built to verify the analysis. The measured maximum efficiency of the prototype is 95%.

Key words: Active clamp, Coupled inductor, High step-up, Zero-voltage-switching

I. INTRODUCTION

Non-isolated high step-up DC/DC converters are widely employed in many industrial applications, such as uninterruptable power systems, photovoltaic systems, fuel cell systems, electric vehicles, high-intensity discharge lamps, etc. [1]-[4]. Theoretically, under the ideal continuous current mode operation, the conventional boost converter can achieve a very high voltage gain with an extremely high duty cycle. However, in practice, it is difficult to design a boost converter with a very high voltage gain due to the equivalent series resistance (ESR) elements, which cause poor efficiency and a degraded voltage gain. The optimized voltage gain of the conventional boost converter is limited to approximately four times with a relative high efficiency [5], [6]. Therefore, it is not preferable for high step-up and high voltage applications.

Many isolated current-fed converters, such as current-fed push-pull converters [7], current-fed full-bridge converters [8], and dual boost converters are applied in high step-up applications [9], [10]. When compared with the voltage-fed converters, the voltage stresses of the rectifier diodes and the turns ratio of the transformer are reduced in the current-fed converters due to their boost-type configuration, which make them more suitable for obtaining a high voltage gain [11], [12]. However, at least one inductor and one transformer are required in these converters, which increases the circuit volume and reduces the power density.

When compared with an isolation transformer, a coupled inductor or tapped inductor has a simpler winding structure and lower conduction loss. Thus, a coupled-inductor-based high step-up boost converter seems to be more attractive in these high step-up applications. By introducing a coupled inductor to the conventional boost converter, the turns ratio of the coupled inductor becomes another design freedom for extending the voltage gain except for the switch duty cycle, which shows a flexibility for optimizing the efficiency and improving the utilization of the components [13]. However, the leakage inductance of the coupled inductor may cause a high voltage spike on the switch when it turns OFF. It may also induce large energy losses. In order to solve the aforementioned problems, a resistor-capacitor-diode (RCD) snubber can be employed, but the leakage energy is

Manuscript received Jun. 10, 2014; accepted Sep. 18, 2014
Recommended for publication by Associate Editor Joung-Hu Park.
†Corresponding Author: lqm394@126.com
Tel: + 86-23-65111934, Chongqing University
*State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, China

dissipated [14]. Passive lossless clamp circuits composed of diodes and capacitors are adopted to clamp the turn-off voltage spikes on the switch and to recycle the leakage inductance energy [15]-[18]. Thus, low-voltage rated switches can be employed to improve the efficiency. Meanwhile, the reverse-recovery problem of the output diode is partly solved by a reasonable design of the leakage inductance. However, the switches in these converters work under the hard switching condition. The active clamp circuit can be used to replace the role of the passive lossless clamp circuit. In addition, the main and clamp switches turn ON under the zero-voltage-switching (ZVS) condition, and the turn OFF losses can be greatly reduced with the help of parallel capacitors [19]. Unfortunately, the output rectifier diode suffers from very high voltage stress. Thus, high-voltage-rated diodes must be adopted, which may degrade the efficiency.

In this paper, an active clamp high step-up boost converter with a coupled inductor is proposed. Like the converter proposed in [19], the coupled inductor is included to extend the voltage ratio, while a boost type or buck-boost type clamp circuit can be employed to recycle the leakage inductance energy and achieve the zero voltage switching condition for the main and clamp switches. Moreover, a rectifier composed of a diode and a capacitor is adopted to reduce the voltage stress of the output rectifier diode. Since the voltage stresses of the switches and diodes are lower than the output voltage, low-voltage-rated metal-oxide-semiconductor field-effect transistors (MOSFETs) and diodes can be adopted for reductions of conduction losses and cost.

This paper is organized as follows. In Section II, the derivation of the proposed converter is presented and the operation analysis is described. The steady state performance analysis is carried out in Section III. Experimental results are given in Section IV, and Section V presents some conclusions drawn from the investigation.

II. Derivation and Operation Analysis of the Converter

A. Topology Derivation

The coupled-inductor boost converter presented in [14] is shown in Fig. 1(a), and the voltage gain is given by:

$$\frac{V_o}{V_{in}} = \frac{1+ND}{1-D} \tag{1}$$

Where D is the duty cycle of the main switch S, and N (N=n_2/n_1) is the turns ratio of the coupled-inductor.

From (1), it is clear that a higher voltage gain than that of the conventional boost converter is achieved by introducing the coupled inductor. However, the voltage stress of the output diode D_o is much higher than its output voltage when switch S is in the on state. A rectifier composed of a diode D_r and a capacitor C_r is included to reduce the voltage stress of the output diode D_o as shown in Fig. 1(b). Therefore, low-voltage-rated diodes can be adopted for a reduction of the conduction losses, and a higher efficiency can be achieved than the circuit shown in Fig. 1(a). Finally, in order to make the main switch S work under the soft switching condition, a boost type active clamp circuit composed of a clamp switch S_c and a capacitor C_c is adopted, as shown in Fig. 1(c).

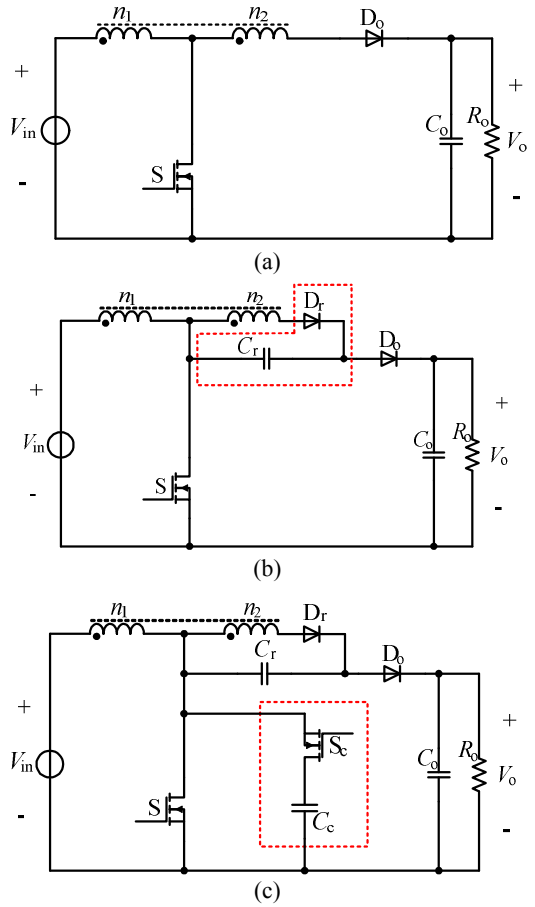


Fig. 1. The derivation of the proposed converter. (a) The coupled-inductor based boost converter presented in [14]. (b) A capacitor and a diode are added as a rectifier. (c) Active clamp circuit is included.

B. Operation Analysis

In order to perform a mode analysis of the proposed converter, several assumptions are made as follows. The coupled inductor is modeled as a magnetizing inductor L_m, a leakage inductor L_{lk}, and an ideal transformer with a turn ratio N. C_s is the extra parallel capacitor, and the parasitic capacitors of the main and clamp switches can be included in it. D_s and D_c are the body diodes of S and S_c, respectively. The capacitors C_c, C_r and C_o are large enough to assume that the voltages across them is constant. Finally, the switches and diodes are assumed to be ideal. The equivalent circuit of the converter is shown in Fig.2.

There are nine operation stages during one switching cycle.

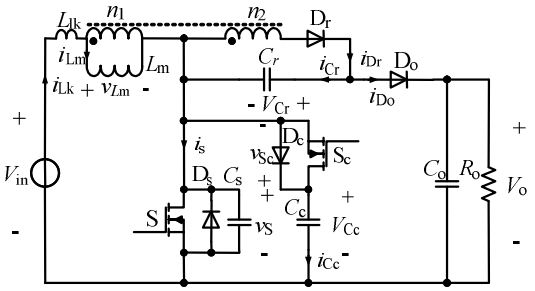


Fig. 2. The equivalent circuit of the proposed converter.

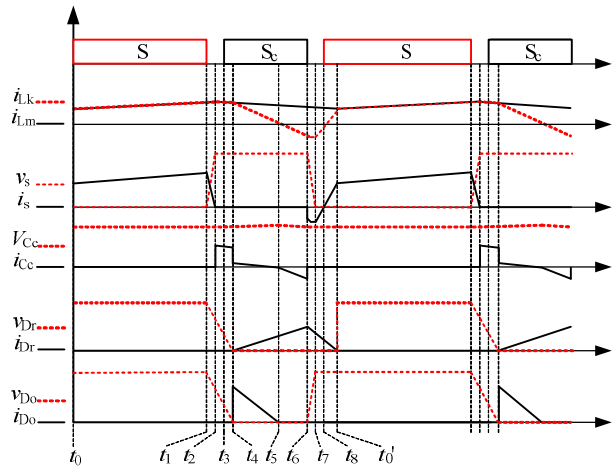


Fig. 3. Key waveforms of the proposed converter.

The key waveforms are shown in Fig.3 and the equivalent circuits for each stage are shown in Fig.4.

Stage 1 [t_0–t_1]: Before t_1, the main switch S is in the ON state while the clamp switch S_c is in the OFF state. The output diode D_o and rectifier diode D_r are reversed-biased. The magnetizing inductor L_m and leakage inductor L_{lk} are connected in series and charged by the input voltage V_{in}. Therefore, the currents through them are equal and increase gradually in a linear way. The clamp capacitor voltage V_{Cc} and rectifier capacitor voltage V_{Cr} are unchanged. The load current is provided solely by the output capacitor C_o. In this stage, the increasing rate of the magnetizing inductor current i_{Lm} and that of the leakage inductor current i_{Lk} are given by:

$$\frac{di_{Lm}}{dt}=\frac{di_{Lk}}{dt}=\frac{V_{in}}{L_m+L_{lk}} \tag{2}$$

Stage 2 [t_1–t_2]: At t_1, the main switch S turns off. Then, the parallel capacitor C_s is charged by the magnetizing current. Since C_s is small and L_m is relatively large, the drain-source voltage of the switch S increases and that of the clamp switch S_c decreases at a constant slope. The turn-off losses of the main switch S are reduced due to the existence of the parallel capacitor C_s. The increasing rate of the drain-source voltage v_s can be derived by:

$$\frac{dv_s}{dt}=\frac{I_{Lm}(t_1)}{C_s} \tag{3}$$

The transition interval of this stage is deduced by:

$$\Delta T_{t_2-t_1}=t_2-t_1=\frac{C_sV_{Cc}}{I_{Lm}(t_1)} \tag{4}$$

Stage 3 [t_2–t_3]: At t_2, the drain-source voltage of the main switch S reaches the clamp voltage, and the antiparallel diode of the clamp switch D_c is forced to conduct. Therefore, v_s is clamped to V_{Cc} by the antiparallel diode D_c. Since the clamp capacitor C_c is much larger than C_s, C_s can be neglected and almost all of the current flows through C_c. In this stage, the magnetizing inductor and leakage inductor are discharged by the voltage of V_{in}-V_{Cc}, and the currents through them decrease approximately linearly with a decreasing rate given by:

$$\frac{di_{Lm}}{dt}=\frac{di_{Lk}}{dt}=\frac{V_{in}-V_{Cc}}{L_m+L_{lk}} \tag{5}$$

Stage 4 [t_3–t_4]: The turn-on signal is applied to the clamp switch S_c at t_3. S_c is turned ON when its antiparallel diode D_c is conducting. Thus, the ZVS turn-on condition is achieved. The equivalent circuit in this stage is similar to that of stage 3.

Stage 5 [t_4–t_5]: At t_4, the rectifier diode D_r and output diode D_o are forced to conduct. The magnetizing inductor L_m and leakage inductor L_{lk} are discharged by the voltages of $-V_{Cr}/N$ and $V_{in}+V_{Cr}/N-V_{Cc}$, respectively. Since L_{lk} is much smaller than L_m, the decreasing rate of i_{lk} is much greater than that of i_{Lm}. Since the output capacitor C_o is relatively large when compared with the clamp capacitor C_c, the current through the output rectifier diode i_{Do} is approximately equal to i_{lk}. The current through the rectifier diode i_{Dr} increases linearly from zero, and the increasing rate is given by (8).

$$\frac{di_{Lm}}{dt}=-\frac{V_{Cr}}{NL_m} \tag{6}$$

$$\frac{di_{Lk}}{dt}=\frac{di_{Do}}{dt}=\frac{V_{in}+V_{Cr}/N-V_{Cc}}{L_{lk}} \tag{7}$$

$$\frac{di_{Dr}}{dt}=\frac{\frac{di_{Lm}}{dt}-\frac{di_{Lk}}{dt}}{N}=\frac{\left(V_{Cc}-V_{in}\right)}{NL_{lk}}-\frac{V_{Cr}}{N^2}\left(\frac{1}{L_{lk}}+\frac{1}{L_m}\right) \tag{8}$$

Stage 6 [t_5–t_6]: At t_5, the current through the output diode D_o decreases linearly to zero and D_o turns off. The leakage inductor current i_{Lk} begins to change its direction and it increases linearly in the reverse direction. The magnetizing inductor current i_{Lm} continues to decrease linearly and the current through the rectifier diode i_{Dr} continues to increase linearly. The change rates of i_{Lk}, i_{Lm} and i_{Dr} are the same as the ones in the previous stage.

Stage 7 [t_6–t_7]: At t_6, the clamp switch S_c turns off. The parallel capacitor C_s and the leakage inductor L_{lk} begin to resonate. Since the resonant period is relatively large and the transition interval of this stage is relatively small too, it is reasonable to assume that the leakage inductor current i_{Lk} keeps constant and that v_s decrease approximately linearly. The magnetizing inductor current i_{Lm} continues to decrease with the change rate shown in (6). The transition interval of this stage can be derived by:

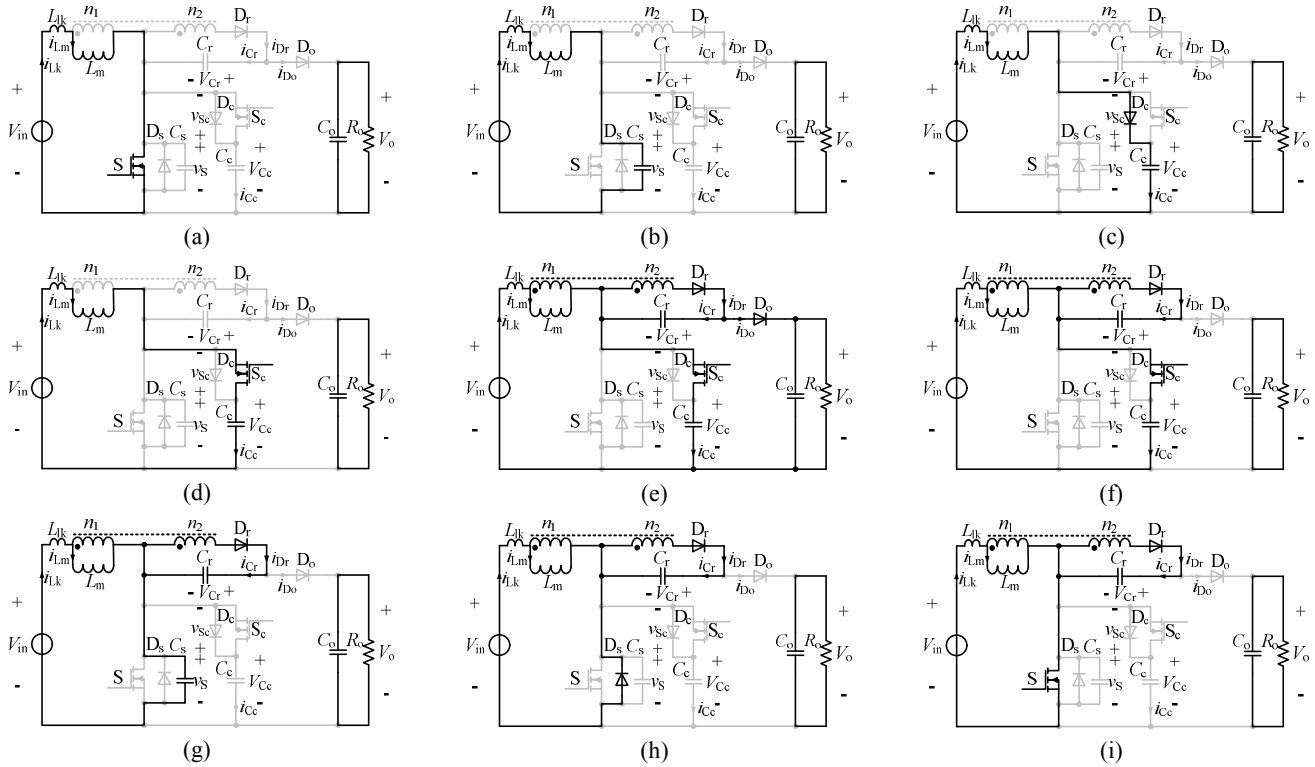


Fig. 4. Operational stages of the proposed converter. (a) Stage 1 [t_0–t_1]. (b) Stage 2 [t_1–t_2]. (c) Stage 3 [t_2–t_3]. (d) Stage 4 [t_3–t_4]. (e) Stage 5 [t_4–t_5]. (f) Stage 6 [t_5–t_6]. (g) Stage 7 [t_6–t_7]. (h) Stage 8 [t_7–t_8]. (i)Stage 9 [t_8–t_0'].

$$\Delta T_{t_7-t_6} = t_7 - t_6 = \frac{C_s V_{Cc}}{I_{Lk}(t_6)} \tag{9}$$

Stage 8 [t_7–t_8]: At t_7, the drain-source voltage of the main switch v_s decreases to zero and the parallel diode D_s is forced to conduct. The voltage across the leakage inductor is equal to $V_{in}+V_{Cr}/N$, and the change rate is derived by (10). The magnetizing inductor current i_{Lm} continues to decrease in this stage.

$$\frac{di_{Lk}}{dt} = \frac{V_{in} + V_{Cr}/N}{L_{lk}} \tag{10}$$

Stage 9 [t_8–t_0']: At t_8, the turn-on signal is applied to the main switch S when its antiparallel diode is in the ON state. Therefore, the main switch S turns ON with ZVS. The equivalent circuit of this stage is similar to that of the previous stage. At t_0', the leakage inductor current i_{Lk} increases to be equal to the magnetizing inductor current i_{Lm}, the current through the rectifier diode i_{Dr} drops to zero, and D_r turns off. After that, the magnetizing inductor L_m and leakage inductor L_{lk} are connected in series and charged by the input voltage V_{in} again. Then, a new switching period begins.

III. Steady State Performance Analysis

A. Voltage Gain

When the leakage inductor L_{Lk} is equal to zero, one switching cycle can be separated into two stages. When the main switch S is in the ON state and the clamp switch S_c is in the OFF state, the voltage across the magnetizing inductor L_m, $V_{Lm\text{-}charge}$ can be derived by:

$$V_{Lm\text{-}charge} = V_{in} \tag{11}$$

When the main switch S is in the OFF state and the clamp switch S_c is in the ON state, the magnetizing inductor is discharged by $V_{Lm\text{-}discharge}$, and $V_{Lm\text{-}discharge}$ is deduced by:

$$V_{Lm\text{-}discharge} = V_{Cc} - V_{in} \tag{12}$$

By applying the inductor volt-second balance principle to the magnetizing inductor, the voltage across the clamp capacitor V_{Cc} can be derived by:

$$V_{Cc} = \frac{V_{in}}{1-D} \tag{13}$$

Since the magnetizing inductor current i_{Lm} is continuous, the capacitor voltage V_{Cr} can de deduced by:

$$V_{Cr} = \frac{NDV_{in}}{1-D} \tag{14}$$

Apparently, the output voltage V_o is the sum of V_{Cc} and V_{Cr}. Therefore, the ideal voltage gain M_{ideal} when the leakage inductor is omitted can be obtain by:

$$M_{ideal} = \frac{V_o}{V_{in}} = \frac{1+ND}{1-D} \tag{15}$$

From the operation analysis in Section II, it can be seen that the leakage inductor L_{lk} causes little duty cycle loss. The voltage gain when considering the influence of leakage inductor L_{lk} is deduced as follows.

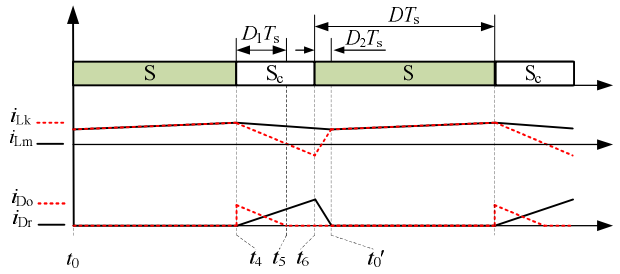


Fig. 5. The simplified waveforms.

Since the time intervals from t_1 to t_4 and from t_6 to t_8 are relatively short when compared with the switching cycle, they are excluded in the following voltage gain analysis, and there are only four stages during one switching cycle. The ideal current waveform of the leakage inductance is taken as a straight line during each subinterval due to the relatively large resonant period. Simplified waveforms are shown in Fig. 5.

During the time interval from t_0 to t_4, the main switch S is in the ON state and the clamp switch S_c is in the OFF state. Moreover, the rectifier diode D_r is reverse biased. The magnetizing inductor L_m and leakage inductor L_{lk} are series connected and charged by $V_{Lm\text{-}charge}$ and $V_{Llk\text{-}charge}$, respectively. $V_{Lm\text{-}charge}$ and $V_{Llk\text{-}charge}$ are derived by:

$$V_{Lm\text{-}charge}=\frac{L_m}{L_m+L_{lk}}V_{in} \tag{16}$$

$$V_{Llk\text{-}charge}=\frac{L_{lk}}{L_m+L_{lk}}V_{in} \tag{17}$$

During the time interval from t_4 to t_6, the main switch S is in the OFF state and the clamp switch S_c is in the ON state. At the same time, the rectifier diode D_r is forced to conduct. The magnetizing inductor L_m and leakage inductor L_{lk} are discharged by $V_{Lm\text{-}discharge}$ and $V_{Llk\text{-}discharge}$, respectively, and can be obtained by:

$$V_{Lm\text{-}discharge}=\frac{V_{Cr}}{N} \tag{18}$$

$$V_{Llk\text{-}discharge}=V_{Cc}-\frac{V_{Cr}}{N}-V_{in} \tag{19}$$

During the last time interval in one switching cycle from t_6 to t_0', the main switch S is in the ON state and the clamp switch S_c is in the OFF state. In addition, the rectifier diode D_r is forward biased in this time interval. The magnetizing inductor is discharged by $V_{Lm\text{-}discharge}$ which can be obtained by (18), while the leakage inductor is charged by $V_{Llk\text{-}charge}$ which can be derived by:

$$V_{Llk\text{-}charge}=V_{in}+\frac{V_{Cr}}{N} \tag{20}$$

By applying the volt-second balance principle to the magnetizing inductor L_m and leakage inductor L_{lk}, the following equations can be derived:

$$\frac{L_mV_{in}}{L_{lk}+L_m}(D-D_2)=\frac{V_{Cr}}{N}(1-D+D_2) \tag{21}$$

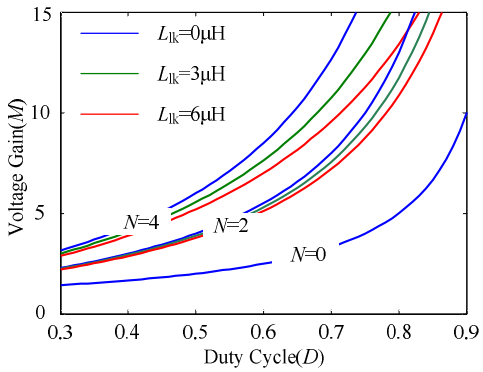


Fig. 6. The voltage gain of the proposed converter.

$$\left(V_{in}+\frac{V_{Cr}}{N}\right)D_2+\frac{L_{lk}V_{in}}{L_{lk}+L_m}(D-D_2)=\left(V_{Cc}-\frac{V_{Cr}}{N}-V_{in}\right)(1-D) \tag{22}$$

At t_6, the current through the diode D_f, i_{Dr} reaches its peak value $I_{Dr\text{-}peak}$ which can be deduced by (23), and the average value of i_{Dr}, I_{Df} can be obtained by (24):

$$I_{Dr\text{-}peak}=\frac{I_{Lm}(t_6)-I_{Lk}(t_6)}{N}=\left[\frac{(V_{Cc}-V_{in})}{NL_{lk}}-\frac{V_{Cr}}{N^2}\left(\frac{1}{L_{lk}}+\frac{1}{L_m}\right)\right](1-D)T_s \tag{23}$$

$$I_{Dr}=\frac{1}{2}(1-D+D_2)\left[\frac{(V_{Cc}-V_{in})}{NL_{lk}}-\frac{V_{Cr}}{N^2}\left(\frac{1}{L_{lk}}+\frac{1}{L_m}\right)\right](1-D)T_s \tag{24}$$

When operating at the steady state, the average currents through the capacitors C_r and C_o are zero. Therefore, I_{Dr} should be equal to the output current I_o and the following equation is obtained:

$$I_{Dr}=I_o=\frac{V_o}{R_o} \tag{25}$$

Apparently, the output voltage V_o is the sum of V_{Cc} and V_{Cr}, that is:

$$V_o=V_{Cc}+V_{Cr} \tag{26}$$

From (21), (22) and (24) to (26), the voltage gain of the proposed converter, when considering the leakage inductor, can be expressed by:

$$M=\frac{V_o}{V_{in}}=\frac{1}{2(1-D)}-\frac{N}{2(1+k_L)}-\frac{1-D}{4k_mN}+\sqrt{\left[\frac{N}{2(1+k_L)}-\frac{1}{2(1-D)}+\frac{1-D}{4k_mN}\right]^2+\frac{1}{2k_mN}\left(1+\frac{DN}{1+k_L}\right)} \tag{27}$$

Where $k_L=L_{lk}/L_m$ and $k_m=L_{lk}f_s/R_o$. f_s is the switching frequency.

The relationship between the voltage gain, the duty cycle, the leakage inductor, and the turns ratio with L_m=120 μH, f_s=100 kHz, R_o=578 Ω is shown in Fig. 6. It is concluded that the voltage gain ratio increases significantly as the turns ratio of the coupled inductor increases, which is a desirable feature in high step-up high efficiency applications because a very narrow turn-OFF period is avoided. When the turns ratio is zero, the voltage gain of the proposed converter is the same as that of the conventional boost converter. The leakage inductor has little effect on the voltage gain of the converter. As the leakage inductor increases, the voltage gain decreases.

B. Voltage and Current Stresses

Neglecting the voltage ripples on the capacitors C_c, C_r and C_o, and assuming the leakage inductor to be zero, the voltage stress of the main switch S, $V_{S\text{-stress}}$ is equal to the voltage stress of the clamp switch S_c, $V_{Sc\text{-stress}}$, which can be derived by:

$$V_{S\text{-stress}} = V_{Sc\text{-stress}} = V_{Cc} = \frac{V_{in}}{1-D} \tag{28}$$

The voltage stress of the rectifier diode D_r, $V_{Dr\text{-stress}}$ is given by:

$$V_{Dr\text{-stress}} = NV_{in} + V_{Cr} \tag{29}$$

From (14) and (29), $V_{Dr\text{-stress}}$ is obtained by:

$$V_{Dr\text{-stress}} = \frac{NV_{in}}{1-D} \tag{30}$$

The voltage stress of the output diode D_o, $V_{Do\text{-stress}}$ is given by:

$$V_{Do\text{-stress}} = V_o - V_{Cr} \tag{31}$$

From (14), (15) and (31), $V_{Do\text{-stress}}$ is obtained by:

$$V_{Do\text{-stress}} = \frac{V_{in}}{1-D} \tag{32}$$

From (15), (28) and (32), $V_{S\text{-stress}}$, $V_{Sc\text{-stress}}$, and $V_{Do\text{-stress}}$ are equivalent and they are lower than the output voltage V_o. Fig. 7(a) shows the voltage stress normalized by V_o. When the duty cycle D and the turns ratio N increase, the voltage stress decreases. Since $V_{S\text{-stress}}$ and $V_{Sc\text{-stress}}$ are much lower than the output voltage V_o, low-voltage-rated switches can be used to improve the efficiency. From (15) and (30), the voltage stress of the rectifier diode D_r $V_{Dr\text{-stress}}$ normalized by the output voltage V_o is shown in Fig. 7(b). It can be seen that the voltage stress on D_r decreases as the duty cycle D increases or as the turns ratio N decreases. Moreover, it is lower than the output voltage V_o if the following condition is satisfied:

$$N < \frac{1}{1-D} \tag{33}$$

According to the operation analysis of the proposed converter in Section II, the current stresses of the main switch S, the clamp switch S_c, and the output diode D_o, which are expressed by $I_{S\text{-stress}}$, $I_{Sc\text{-stress}}$, and $I_{Do\text{-stress}}$, respectively, are similarly equal to the peak value of the current through the output rectifier diode D_o, $I_{Do\text{-peak}}$. From Fig.5, $I_{Do\text{-peak}}$ can be deduced by:

$$I_{Do\text{-peak}} = \frac{V_{Cc} - \frac{V_{Cr}}{N} - V_{in}}{L_{lk}} D_1 T_s \tag{34}$$

Since the average value of the current through the output rectifier diode D_o, I_{Do} should be equal to the output current I_o when operating at the steady state, the following equation is obtained:

$$I_{Do} = \frac{1}{2} D_1 I_{Do\text{-peak}} = \frac{V_o}{R_o} \tag{35}$$

Additionally, the clamp capacitor voltage V_{Cc} is given by:

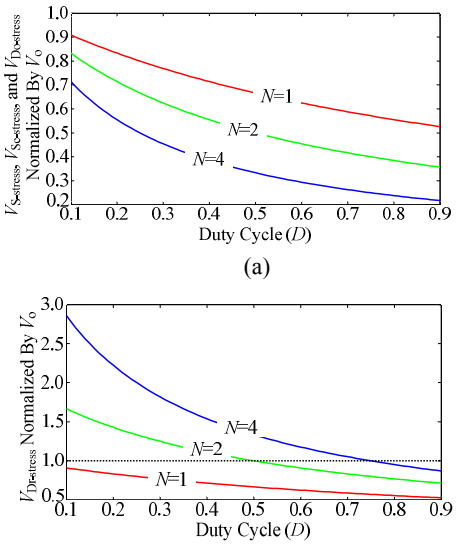


Fig. 7. The voltage stresses according to the variation of duty cycle D and turns ratio N. (a) $V_{S\text{-stress}}$, $V_{Sc\text{-stress}}$, $V_{Do\text{-stress}}$ normalized by V_o. (b) $V_{Dr\text{-stress}}$ normalized by V_o.

$$V_{Cc} = \frac{V_{in}}{1-D} \tag{36}$$

From (26), (27) and (34) to (36), D_1 can be derived by:

$$D_1 = \sqrt{\frac{2MNk_m(1-D)}{D(M+N)-M+1}} \tag{37}$$

Therefore, $I_{S\text{-stress}}$, $I_{Sc\text{-stress}}$ and $I_{Do\text{-stress}}$ can be deduced by:

$$I_{S\text{-stress}} = I_{Sc\text{-stress}} = I_{Do\text{-stress}} = I_o \sqrt{\frac{2[D(M+N)-M+1]}{k_m MN(1-D)}} \tag{38}$$

$I_{S\text{-stress}}$, $I_{Sc\text{-stress}}$ and $I_{Do\text{-stress}}$ normalized by I_o according to variations of the duty cycle D, the turns ratio N and the leakage inductor L_{lk} are shown in Fig. 8(a). It is shown that the current stress increases with an increasing duty cycle D. Additionally, as the turns ratio N decreases and the leakage inductor L_{lk} increases, the current stress decreases.

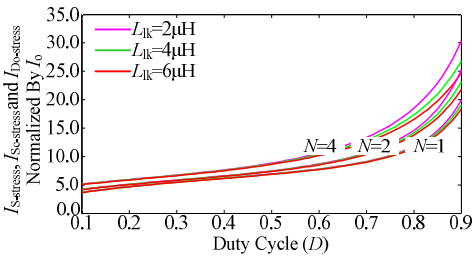
From (23), (26), (27) and (32), the current stress of the rectifier diode D_r, $I_{Dr\text{-stress}}$ can be derived by:

$$I_{Dr\text{-stress}} = I_o \frac{DN + (MD - M + 1)(1 + k_L)}{k_m MN^2} \tag{39}$$

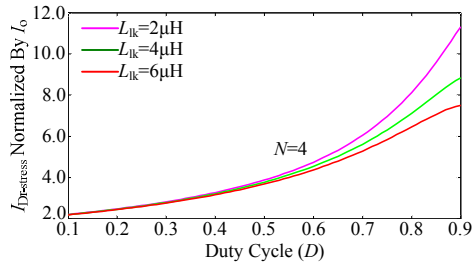
$I_{Dr\text{-stress}}$ normalized by I_o according to variations of the duty cycle D, the turns ratio N and the leakage inductor L_{lk} is shown in Fig. 8(b) to Fig. 8(d) with N=4, N=2, and N=1 respectively for clear. It is show that the current stress of the rectifier diode D_r increases with an increasing duty cycle. However, it decreases with an increasing leakage inductor. Moreover, from Fig. 8(b) to Fig. 8(d), the current stress $I_{Dr\text{-stress}}$ increases with a decreasing turns ratio N.

C. Soft Switching Condition

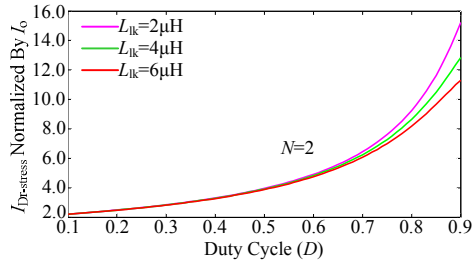
The turn-off losses of the main and clamp switches are reduced because of the parallel capacitor. The reverse-recovery losses of the diodes are negligible since the



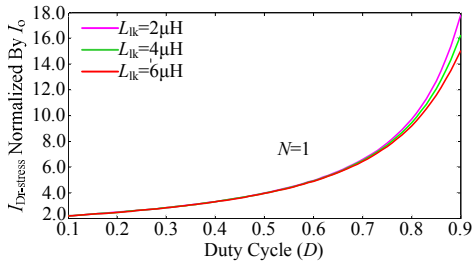
(a)



(b)



(c)



(d)

Fig. 8. The current stress of the main switch S, clamp switch S_c, output diode D_o, and rectifier diode D_r normalized by I_o. (a) $I_{S\text{-stress}}$, $I_{Sc\text{-stress}}$, $I_{Do\text{-stress}}$ normalized by I_o. (b) $I_{Dr\text{-stress}}$ normalized by I_o with N=4. (c) $I_{Dr\text{-stress}}$ normalized by I_o with N=2. (d) $I_{Dr\text{-stress}}$ normalized by I_o with N=1.

leakage inductor provides a current snubbing effect. The ZVS turn-on condition of the clamp switch can be realized by applying a turn-on signal when its antiparallel diode is in the ON state and the drain-source voltage is clamped to zero. To realize to the ZVS turn-on condition of the main switch, the energy stored in the leakage inductor should be greater than that stored in the parallel capacitor when the clamp switch turns off. Therefore, the ZVS turn-on condition of the main switch can be derived by:

$$L_{lk} I_{Lk}^2(t_6) \geq C_s V_S^2(t_6) \tag{40}$$

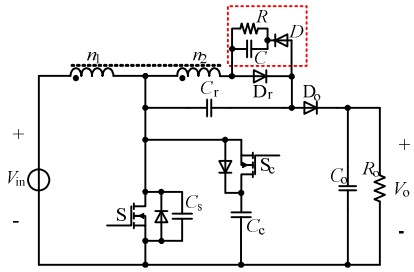


Fig. 9. The proposed converter with RCD snubber.

TABLE I
PARAMETER OF THE PROTOTYPE

Power Level P_o	250W
Input Voltage V_{in}	40V~56V
Output Voltage V_o	380V
Switching Frequency f_s	100kHz
Switches S &S_c	IRFP4227Pbf/200V
Diodes D_o	MUR820/200V
Diodes D_r&D	MUR840/400V
Clamp Capacitor C_c	1μF
Parallel Capacitor C_s	1nF
Capacitor C_r	5μF
Output Capacitor C_o	220μF
Turns Ratio N	53 :21
Leakage Inductor	5μH
Magnetizing Inductor	120μH
Resistance R	75kΩ
Capacitor C	47μF

IV. EXPERIMENTAL RESULTS AND ANALYSIS

In order to verify the performance of the proposed converter, a 250W prototype is built and tested. Due to the resonance between the leakage inductor of the coupled inductor and the junction capacitor of the rectifier diode D_r, it is necessary to add a proper resistor-capacitor-diode (RCD) snubber to reduce the voltage spike across D_r, as shown in Fig. 9. Since the current level at the high-voltage side of the coupled inductor is relatively low, even though an RCD snubber is adopted, the conversion efficiency will not drop significantly. The parameters of the converter are described in Table I and the experimental results of the proposed converter are shown in Fig. 10.

Fig. 10(a) shows the gate-source voltage of the main switch Q_S, the input voltage V_{in} and the output voltage V_o. The measured duty cycle is about 0.68 as predicted by (15), and high step-up capacity is verified. The current of the leakage inductance i_{Lk} and the voltage of the magnetizing inductance v_{Lm} are shown in Fig. 10(b). It can be seen that the experimental results are consistent with the theoretical analysis. The gate-source voltage, drain-source voltage and current experimental waveforms of the main switch S and the

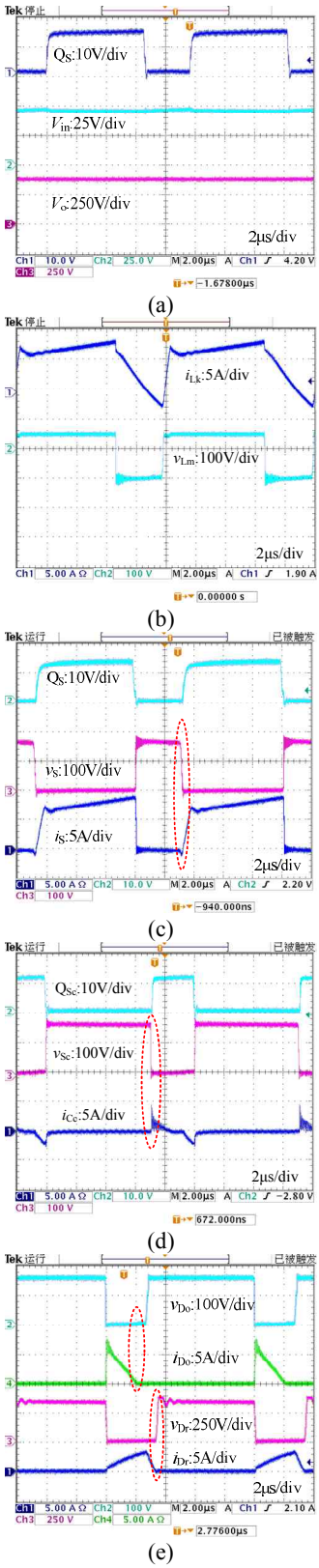


Fig.10. The experimental results of the proposed converter. (a) The measured waveforms of Q_S, V_{in} and V_o. (b) Leakage current i_{Lk} and magnetizing inductance voltage v_{Lm} (c) ZVS-on performance of main switch S. (d) ZVS-on performance of clamp switch S_c. (e) Voltage and current waveforms of rectifier diode D_r and output diode D_o.

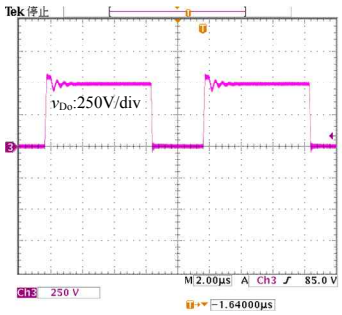


Fig. 11. Voltage waveforms of output diode in the converter proposed in [19].

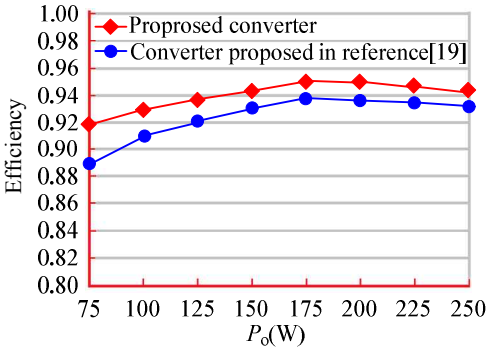


Fig. 12. The efficiency comparison between proposed converter and converter proposed in reference [19].

clamp switch S_c are shown in Fig. 10(c) and Fig. 10(d) respectively. It is shown that both the main switch and the clamp switch are turned ON and OFF under the ZVS condition. This reduces the switching losses greatly. Moreover, the voltage stresses of the main switch and clamp switch is about 160V. Thus, low-voltage-rated MOSFETs can be adopted and the conduction losses can be reduced. Fig. 10(e) shows voltage and current waveforms of the rectifier diode D_r and the output rectifier diode D_o. Clearly, the reverse-recovery current of the rectifier diode D_r and output rectifier diode D_o is small because the reverse-recovery problem is alleviated by the leakage inductance of the coupled inductor. As a result, the reverse-recovery losses are minimized. The voltage waveform of the output diode in the converter proposed in [19] is illustrated in Fig. 11. It shows that the voltage stress of the diode is 550V, which is much higher than the 380V of the rectifier diode D_r and the 160V of the output rectifier diode D_o in the proposed converter. Therefore, a low forward voltage drop diode can be used to improve the efficiency of the proposed converter. An efficiency comparison between the proposed converter and the converter proposed in reference [19] is plotted in Fig. 12. It can be seen that the maximum efficiency of the proposed converter is 95% with a 48V input and a 380V output conversion when operating at 100kHz. When compared with the converter proposed in reference [19], there is about a 1% efficiency improvement under full load and about a 3% efficiency improvement under light load.

V. CONCLUSIONS

An active clamp high step-up boost converter with a coupled inductor has been proposed in this paper. A coupled inductor is included to extent the voltage gain. By applying an active clamp circuit, the main and clamp switches operate under the ZVS condition and the switching losses are minimized. The reverse-recovery problems of the diodes are solved due to the inherent leakage inductor of the coupled inductor. Additionally, the voltage stress of the output diode is reduced by adopting a rectifier composed of a diode and a capacitor. The derivation of the proposed converter is presented. A steady-state operational analysis and the main circuit performance are discussed to explore the advantages of the proposed converter. Finally, a 250W prototype has been built and experimental results have been presented to verify the analysis.

ACKNOWLEDGMENT

This project is supported by The National High Technology Research and Development of China 863 Program (2011AA05A110),the National Natural Science Foundation of China (51207172), and the Scientific Research Foundation of the SKL of Power Transmission Equipment & System Security and New Technology (2007DA10512713204).

REFERENCES

[1] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc-dc converters," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 65-73, Jan. 2003.

[2] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 50, No. 8, pp. 1098-1102, Aug. 2003.

[3] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 55, No. 4, pp. 1159-1171, May. 2008.

[4] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron*., Vol. 58, No. 4, pp. 1239-1250, Apr. 2011.

[5] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, Kluwer Academic Publisher Group, 2001.

[6] A. Davoudi and J. Jatskevich, "Parasitics realization in state-space average-value modeling of PWM DC-DC converters using an equal area method," *IEEE Trans. Circuits Syst. I, Reg. Papers,* Vol. 54, No. 9, pp. 1960-1967, Sep.2007.

[7] J. M. Kwon, E. H. Kim, B. H. Kwon, and K. H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction," *IEEE Trans. Ind. Appl.*, Vol. 56, No. 3, pp. 826-834, Mar. 2009.

[8] H. Zhou, A. M. Khambadkone, and X. Kong, "Passivity-based control for an interleaved current-fed full-bridge converter with a wide operating range using the Brayton–Moser form," *IEEE Trans. Power Electron.*, Vol. 24, No. 9, pp. 2047-2056, Sep. 2009.

[9] Q. Li and P. Wolfs, "A current fed two-inductor boost converter with an in-tegrated magnetic structure and passive lossless snubbers for photovoltaic module integrated converter applications," *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp. 309-321, Jan. 2007.

[10] J. M. Kwon and B. H. Kwon, "High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems," *IEEE Trans. Power Electron.*, Vol. 24, No.1, pp. 108-115, Jan.2009.

[11] C. Leu and M. Li, "A novel current-fed boost converter with ripple reduction for high-voltage conversion applications," *IEEE Trans. Ind. Electron.* , Vol. 57, No. 6, pp. 2018-2023, Jun. 2010.

[12] V. Vaisanen, T. Riipinen, and P. Silventoinen, "Effects of switching asymmetry on an isolated full-bridge boost converter," *IEEE Trans. Power Electron.* , Vol. 25, No. 8, pp. 2033-3044, Aug. 2010.

[13] F. A. Himmelstoss and P. H. Wurm, "Low-loss converters with high step-up conversion ratio working at the border between continuous and discontinuous mode," in *Proc. IEEE Int. Conf. Electron., Circuits, Systems (ICECS)*, pp. 734-737, 2000.

[14] N.Vazquez, L. Estrada, C. Hernandez, and E. Rodriguez, "The tapped-inductor boost converter," *IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 538-543, 2007.

[15] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *IEE Proc. Electric Power Appl.*, Vol. 151, No. 2, pp. 182-190, Mar. 2004.

[16] R. J. Wai and R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," *IEE Proc. Electric Power Appl.* , Vol. 152, No. 4, pp. 793-802, Jul. 2005.

[17] R. J. Wai and R. Y. Duan, "High step-up converter with coupled-inductor," *IEEE Trans. Power Electron.*, Vol. 20, No. 5, pp. 1025-1035, Sep. 2005.

[18] J. W. Baek, M. H. Ryoo, T. J. Kim, D. W. Yoo, and J. S. Kim, "High boost converter using voltage multiplier," in *Proc. IEEE 31st Ann. Conf. Ind. Electron Soc. (IECON)*, pp. 567-572, 2005.

[19] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, "Boost converter with coupled inductors and buck–boost type of active clamp," *IEEE Trans. Ind. Electron.* , Vol. 55, No. 1, pp. 154-162, Jan. 2008.

Quanming Luo was born in Chongqing, China, in 1976. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Chongqing University, Chongqing, China, in 1999, 2002, and 2008, respectively. He was with the Emerson Network Power Co. Ltd., Shenzhen, China, as a Research and Development Engineer, from 2002 to 2005. Since 2005, he has been with the College of Electrical Engineering, Chongqing University, where he is presently an Associate Professor. He is the author or coauthor of more than 30 papers in journal or conference proceedings. His current research interests include LED driving systems, communication power

systems, power harmonic suppression, and power conversion systems in electrical vehicles.

Yang Zhang was born in Hubei, China, in 1989. He received his B.S. degree in Electrical Engineering from the Wuhan Polytechnic University, Wuhan, China, in 2012. He is presently working toward his M.S. degree in Electrical Engineering at Chongqing University, Chongqing, China. His current research interests include high-efficiency power converters and photovoltaic power systems.

Pengju Sun was born in Henan, China. She received her B.S. and Ph.D. degrees in Electrical Engineering from Chongqing University, Chongqing, China, in 2005 and 2011, respectively. Since 2011, she has been with the College of Electrical Engineering, Chongqing University. She was a Visiting Student with the University of California, Irvine, CA, USA, from September 2009 to August 2010. Her current research interests include wide output range DC/DC converters, digital control techniques, high power high performance power converters and power factor correction.

Luowei Zhou was born in Dujiangyan, China. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Chongqing University, Chongqing, China, in 1982, 1988, and 2000, respectively. Since 1982, he has been with the College of Electrical Engineering, Chongqing University, where he is presently a Full Professor. He was a Visiting Professor with the University of California, Irvine, CA, USA, from September 1998 to August 1999. He is the Vice Director of the China Society of Power Supply. His current research interests include the analysis and control of power electronics circuits, the realization of active power filters, power factor correction techniques, and high frequency power conversion.