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Phase Locked Loop based Pulse Density Modulation Scheme for the Power Control of Induction Heating Applications

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Abstract

Resonant converters are well suited for induction heating (IH) applications due to their advantages such as efficiency and power density. The control systems of these appliances should provide smooth and wide power control with fewer losses. In this paper, a simple phase locked loop (PLL) based variable duty cycle (VDC) pulse density modulation (PDM) power control scheme for use in class-D inverters for IH loads is proposed. This VDC PDM control method provides a wide power control range. This control scheme also achieves stable and efficient Zero-Voltage-Switching (ZVS) operation over a wide load range. Analysis and modeling of an IH load is done to perform a time domain simulation. The design and output power analysis of a class-D inverter are done for both the conventional pulse width modulation (PWM) and the proposed PLL based VDC PDM methods. The control principles of the proposed method are described in detail. The validity of the proposed control scheme is verified through MATLAB simulations. The PLL loop maintains operation closer to the resonant frequency irrespective of variations in the load parameters. The proposed control scheme provides a linear output power variation to simplify the control logic. A prototype of the class-D inverter system is implemented to validate the simulation results.

Key words: Class-D inverter, Induction heating, Phase locked loop, Pulse density modulation, Zero voltage switching

I. INTRODUCTION

IH systems are used in many industrial, domestic and medical applications due to their high performance. IH technology takes advantage of contactless energy transfer to the work piece to obtain faster heating, improved safety, and higher efficiency than conventional heating methods. The core component of an IH system is the power supply. An IH power supply system is usually composed of a rectifier stage and a resonant inverter. Series resonant inverters (SRIs) are widely used as a high frequency source [1], [2]. In SRIs, the resonant tank circuit is formed by a work coil and a capacitor. A SRI fed with a voltage source represents a simple and cost-effective solution [3]-[5]. However, the output power of such an inverter is controlled by adjusting the DC input voltage. A controlled rectifier with a DC-link capacitor has been conventionally used to provide a variable DC voltage so that the output power of the inverter gets adjusted. However, the size and cost of this conventional arrangement is large [5]-[8]. To overcome these problems, the power control of an inverter, fed by an uncontrolled rectifier using frequency modulation, phase-shift variation and asymmetrical voltage cancellation control is discussed in many studies to regulate the output power. An important goal of power control is to achieve an efficient and useful product. Inverters with the above modulation schemes result in increased switching losses because it is impossible for the switching devices to be always turned on and off at zero current or zero voltage instants.

Generally, IH applications use a frequency modulation scheme to control the output power. Variable frequency control is a basic method which is used for variable load conditions. Variable frequency control is used for half bridge and full bridge SRIs [9]. However, pulse frequency modulation control causes many problems since the switching frequency has to be varied over a wide range to accommodate the worst combinations of loads. The

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efficiency of an inverter decreases significantly with an increase in the switching frequency to lower the output power. The major disadvantage of this method is the large frequency range requirement for a wide range of output power control. For a frequency below resonance, the filter components are bulky because they must be designed for the low frequency range. For operation above resonant frequency, fast switching devices are required to maintain control in the higher frequency range. In addition, the soft switching range of a frequency modulated high frequency inverter is relatively narrow. The control of a SRI with a constant switching frequency with a variable pulse width is one of the ways to avoid the problems of variable frequency control [10], [11].

Therefore, class-D inverter topologies using PWM control, phase-shift control and asymmetrical voltage control have been proposed. In fixed frequency operation, the inverter is operated at a constant frequency and control of the output power without variations in the frequency. However, these control requirements and operating characteristics increase the complexity of the design due to the fixed frequency switching requirement which limits their performance. Phase shifted PWM control was used for full bridge inverters to adjust the output power [12]-[14]. In a IH power supply system using a phase-shift PWM control, zero voltage switching (ZVS) operation is not possible under light load conditions. This control strategy cannot be used for half bridge inverters. Asymmetrical voltage control strategy is also used for the control of output power. It gives improved efficiency due to its constant switching frequency and ZVS operation [15].This method results in high turn on losses under low load conditions due to the NON-ZVS operation of the switches. A discontinuous mode power control scheme for loss minimization is also discussed in the literatures [15]-[18].

In the above papers, a power control scheme of IH loads with the ZVS operating condition in the whole load range is not discussed. This paper discusses a simple PLL based VDC PDM power control scheme of the variable power ZVS class-D inverters for IH applications. The aim of this study is to control the power over a wide load range under the ZVS condition to improve the output power of IH systems. In this paper, the power supply for induction heating (IH) systems based on a class-D SRI is described. The output power of the inverter is controlled using a VDC based PDM. When the inverter is operated at a switching frequency higher than its resonant frequency; it can maintain ZVS operation in the whole load range [19]-[21]. The effective parameters for the equivalent resistance and inductance of an IH load vary throughout the heating cycle [22], [23]. Thus, it becomes necessary to change the operating frequency of the inverter in order to maintain the resonance condition according to load variations. The presented control circuit employs a frequency tracking system to monitor load variations. The control circuit also employs a PDM pulse generation logic circuit which provides modulated gate signals to the gate drive circuitry at the tracked load resonant frequency. Under PDM, the switching losses are fixed and the total output power of the inverter gets increased. In the proposed scheme, the inverter operation at resonance is maintained such that the losses are at a minimum. This improves the efficiency of the IH system over a wide range of power. The proposed modulation technique with a frequency tracking system can achieve a linear output power variation which simplifies the control algorithm.

II. System Description

A block diagram of an IH power supply system is shown in Fig. 1. The class-D inverter takes energy from the 50Hz AC input source through an uncontrolled rectifier. The DC voltage is converted into a high-frequency AC voltage by using the class-D inverter. Then, the inverter supplies a high-frequency current to the induction coil. To track the resonant frequency of the load, a phase locked loop (PLL) is used. At the tracked load frequency, PDM gate pulses are generated and applied to the switches.

A. Characteristics and Modeling of an IH Load

An IH load consists of a work-coil and a work-piece. In IH systems, most of the work-pieces have a cylindrical shape. They are heated by being placed inside the work coil with one or more turns. In IH applications, a magnetic field is induced in the work coil. This causes eddy currents in the work piece. These eddy currents give rise to a heating effect. Most of the heat in the work-piece is generated by eddy currents. Basically, an IH load is a transformer representation of the electromagnetic induction action between the work coil (primary) and the load (secondary) as shown in Fig. 2(a). The transformer parameters are difficult to measure. Therefore, it is better to represent the IH load using a simplified model. The IH load can be modeled by means of a series combination of its equivalent resistance R_{eq} and inductance L_{eq} as shown in Fig. 2(b). These parameters depend on several variables, including the shape of the heating coil, the distance between the work-piece and the IH coil, the temperature, the electrical conductivity and magnetic permeability, and the frequency.

In the transformer equivalent of an IH load, L_1 is the self inductance of the work coil. L_2 is the inductance in the secondary side of the IH load, M is the mutual inductance of the transformer, and R_2 is the resistance of the IH load. The equivalent values of the IH system R_{eq} and L_{eq} change with the geometry, load materials, temperature, and excitation frequency. A change in the parameters makes the output power control harder. For this reason, a complete analysis of the equivalent parameters R_{eq} and L_{eq} of the IH system is

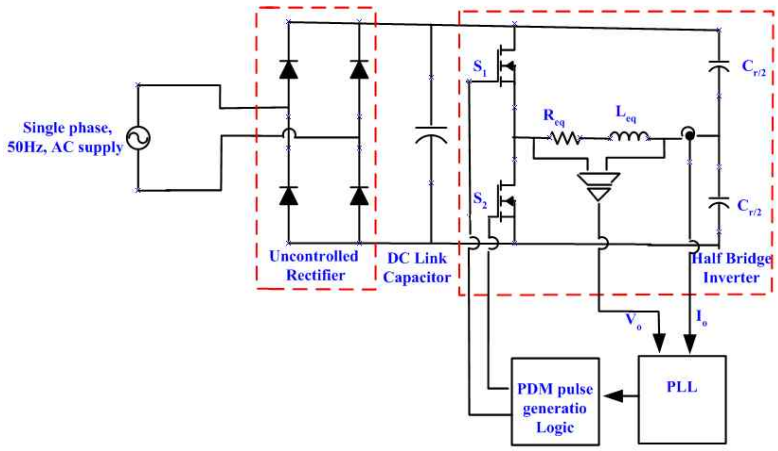
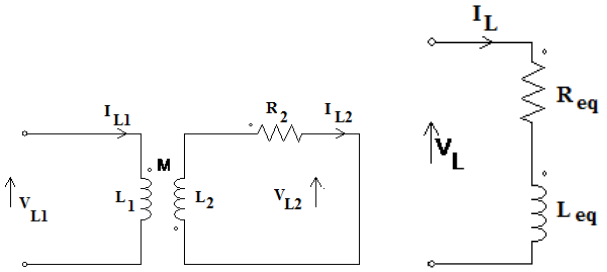


Fig. 1. Block diagram of IH power supply system.



(a) (b)

Fig. 2. (a) Transformer equivalent circuit of IH load. (b) Equivalent series RL circuit of IH load.

provided here. The voltage equations of the transformer model of the IH load are given below:

$$V_{L1} = j\omega_S L_1 I_{L1} + jM\omega_S I_{L2} \quad (1)$$

$$0 = j\omega_S M I_{L1} + (R_2 + j\omega_S L_2) I_{L2} \quad (2)$$

where, $\omega_S = 2\pi f_S$

f_s is the switching frequency, and ω_S is the angular switching frequency. I_{L1} and V_{L1} are the current and voltage in the work coil, respectively.

The load current I_{L2} can be obtained from (2) which is given as:

$$I_{L2} = \frac{-j\omega_S M I_{L1}}{R_2 + j\omega_S L_2} \quad (3)$$

Equations (1) and (3) give the following expression:

$$V_{L1} = \frac{\omega_S^2 M^2 R_2}{R_2^2 + \omega_S^2 L_2^2} + j\omega_S \left[\frac{L_1 R_2^2 + \omega_S^2 L_2 (L_1 L_2 - M^2)}{R_2^2 + \omega_S^2 L_2^2} \right] \quad (4)$$

The real and imaginary parts of the above equation are represented as R_{eq} and L_{eq} as given in the following equations (5) and (6):

$$R_{eq} = \frac{\omega_S^2 M^2 R_2}{R_2^2 + \omega_S^2 L_2^2} \quad (5)$$

$$L_{eq} = L_1 - \frac{\omega_S^2 L_2 M^2}{R_2^2 + \omega_S^2 L_2^2} \quad (6)$$

The general time constant of the load (τ) is defined as:

$$\tau = \frac{L_2}{R_2} \quad (7)$$

Equation (7) can be estimated using equations (5) and (6) as:

$$\tau = \frac{L_1 - L_{eq}}{R_{eq}} \quad (8)$$

since:

$$M^2 = \frac{R_{eq}(R_2^2 + \omega_S^2 L_2^2)}{R_2 \omega_S^2} \quad (9)$$

The mutual coupling co-efficient (K) for a coupled circuit is generally defined as:

$$K = \frac{M}{\sqrt{L_1 L_2}} \quad (10)$$

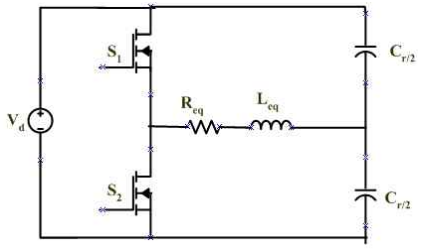
Solving (6) and (10) yields the following expression:

$$K = \sqrt{\frac{R_{eq}^2 + \omega_S^2 (L_1 - L_{eq})^2}{\omega_S^2 L_1 (L_1 - L_{eq})}} \quad (11)$$

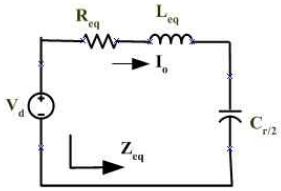
In equation (11), K is expressed with R_{eq} , L_{eq} and L_1.

B. Analysis of a Class-D Inverter

Fig. 3(a) shows the configuration of the class-D inverter system for an IH load. The class-D inverter consists of two switches S_1 and S_2 and two resonant capacitors with a capacitance of $C_r/2$ and an IH load. When the inverter is fed with the DC input voltage S_1 and S_2 are alternately used to allow a high-frequency AC current to the IH coil. Fig. 3(b) shows the equivalent circuit model of the class-D inverter. The switches of the class-D inverter are operated at above the resonant frequency in order to achieve ZVS during turn off [24], [25]. Conventionally, class-D inverter switches are operated with pulse width modulated gate pulses. In this paper power control using PDM is discussed. The PDM inverter repeats “run and stop” in accordance with a control sequence to adjust its output voltage.



(a)



(b)

Fig. 3. (a) Circuit configuration of class-D inverter. (b) Equivalent circuit of class-D inverter.

For simulation study, an IH load is considered with an equivalent circuit of a series combination of resistance R_{eq} and inductance L_{eq}. This series branch with R_{eq} and L_{eq} in combination with C_r forms the resonant circuit. The output power analysis of the resonant circuit under the conventional PWM method for the class-D inverter can be described by the following parameters. The angular resonant frequency (ω_r) of the series resonant circuit is given by:

$$\omega_r = \frac{1}{\sqrt{L_{eq}C_r}} \tag{12}$$

where C_r is the capacitance of the resonant capacitor. The normalized angular switching frequency (ω_n) is expressed as:

$$\omega_n = \frac{\omega_s}{\omega_r} \tag{13}$$

The characteristic impedance (Z_o) of the IH load is:

$$Z_0 = \sqrt{\frac{L_{eq}}{C_r}} = \frac{1}{\omega_r C_r} = \omega_r L_{eq} \tag{14}$$

The quality factor (Q_L) of the IH coil is given by:

$$Q_L = \frac{\omega_r L_{eq}}{R_{eq}} = \frac{1}{\omega_r R_{eq} C_r} = \frac{Z_0}{R_{eq}} \tag{15}$$

The equivalent impedance (Z_{eq}) of the resonant tank circuit is given by the following equations:

$$Z_{eq} = R_{eq} + j\left(\omega_s L_{eq} - \frac{1}{\omega_s C_r}\right) \tag{16}$$

$$\left|Z_{eq}\right| = R_{eq}\sqrt{1 + Q_L^2\left(\omega_n - \frac{1}{\omega_n}\right)} \tag{17}$$

The output voltage of the class-D inverter connected to the IH load is V_o:

$$V_o = \begin{cases} V_d & \text{for } 0 < \omega_s t \le \pi \\ 0 & \text{for } \pi < \omega_s t \le 2\pi \end{cases} \tag{18}$$

The fundamental component (V_{o1}) of the output voltage can be found from the Fourier analysis:

$$V_{01} = V_m \mathrm{Sin}\omega_s t \qquad \text{for } 0 < \omega_s t \le 2\pi \tag{19}$$

Where, the peak value of the output load voltage (V_m) is:

$$V_m = \frac{2V_d}{\pi} \simeq 0.637V_d \tag{20}$$

The load current (I_o) through the resonant tank circuit is described by the following equation:

$$I_0 = I_m \mathrm{Sin}(\omega_s t - \phi) \tag{21}$$

The phase angle (Ø) of the load current is:

$$Ø = \tan^{-1} Q_L\left(\omega_n - \frac{1}{\omega_n}\right) \tag{22}$$

Where, the peak value of the output load current (I_m) is:

$$I_m = \frac{V_m}{\left|Z_{eq}\right|} = \frac{2V_d \mathrm{Cos}\phi}{\pi . R_{eq}\sqrt{1 + Q_L^2\left(\omega_n - \frac{1}{\omega_n}\right)^2}} \tag{23}$$

The conventional output power (P_o) of the class-D inverter is given in the following equations:

$$P_o = I_m^2 \frac{R_{eq}}{2} = \frac{2V_d^2}{\pi^2 R_{eq}\left(1 + Q_L^2\right)\left(\omega_n - \frac{1}{\omega_n}\right)^2} \tag{24}$$

$$= \frac{2V_d^2 \mathrm{Cos}^2\phi}{\pi^2 R_{eq}}$$

$$= \frac{V_{eff}\mathrm{Cos}^2\phi}{R_{eq}} \tag{25}$$

In the conventional PWM method the output power is varied by varying duty cycle of the power switches. A desired output power ($P_{desired}$) can be obtained by variation of the PWM control duty ratio (D_{PWM}).

$$P_{desired} = P_o D_{PWM} \tag{26}$$

The D_{PWM} is given by the following equation:

$$D_{PWM} = \frac{T_{ON}}{T} \tag{27}$$

Where T_{ON} is the turn on time of the switch and T is the total time period. In the PWM control the soft switching range is very narrow since T_{ON} is varied to control the output power.

C. Design Procedure of the Circuit Constraints

The design of the class-D inverter and the IH load parameters are described in this section. For the output power P_o, the equivalent resistance of the IH load is given by the following equation:

$$R_{eq} = \frac{V_{eff}^2}{P_o}\mathrm{Cos}^2\theta \tag{28}$$

By the definition of the quality factor of the resonant circuit given in equation (15), the equivalent inductance L_{eq} of the heating coil with Q_L of 1.28 is given by:

$$L_{eq} = \frac{Q_L R_{eq}}{\omega_r} \quad (29)$$

Finally, the calculation of the value of the resonant capacitor can be done as per equation (12), by the definition of the resonant frequency.

$$C_r = \frac{1}{\omega_r^2 L_{eq}} \quad (30)$$

To reduce the switching losses during the turn off condition, a lossless snubber capacitor (C_s) is used with the switch. Typically, the class-D operation mode implies that C_s is much lower than C_r [25]-[28]. As a result, the switching waveforms in the inverter have a direct impact on all of the inverter losses. During the charge intervals, the output current can be considered constant, due to the small snubber capacitors used in the class-D inverter.

D. Power Consumption in the MOSFET Switches of the Class-D Inverter

Power losses in the power electronic switches include the conduction and switching losses. The switching losses can also be classified into turn-on and turn-off losses. The class-D inverter uses two MOSFETs with anti parallel diodes. The conduction and switching losses for the MOSFET and diode are analyzed below. The total power loss in the MOSFET (P_M) is determined using the following equation:

$$P_M = P_{CM} + P_{SWM} \quad (31)$$

P_{CM} is the conduction loss in the MOSFET, and P_{SWM} is the switching loss in the MOSFET. P_{CM} is given by:

$$P_{CM} = R_D S_{ON} I_{Drms}^2 \quad (32)$$

R_D is the ON state resistance of the switch, S_{ON} is the on/off state of the switch, and I_{Drms} is the rms value of the current through the MOSFET. The P_{SWM} in the MOSFET is:

$$P_{SWM} = \frac{V_S I_d t_{off} f_s}{6} \quad (33)$$

V_s is the on state voltage of the switch, I_d is the instantaneous value of the switch current at the time of switching, t_{off} is the turn off time of the switch, and f_s is the switching frequency.

The total power loss (P_D) in the anti parallel diode is:

$$P_D = P_{CD} + P_{SWD} \quad (34)$$

P_{CD} is the conduction loss in the diode, and P_{SWD} is the switching losses in the diode. P_{CD} is defined as:

$$P_{CD} = V_{DO} I_F \quad (35)$$

V_{DO} is the ON state voltage across the diode, and I_F is average value of the forward current through the diode.

P_{SWD} in the diode is given by:

$$P_{SWD} = R_D I_{frms}^2 \quad (36)$$

where R_D is the ON state resistance of the switch, and I_{frms} is the rms value of the forward current through the diode. The total losses in the inverter module include the MOSFET and diode losses.

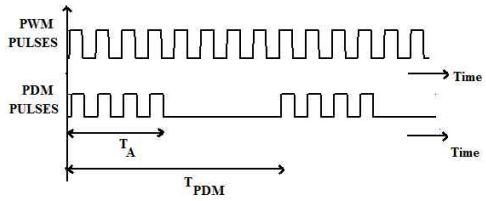


Fig. 4. Theoritical waveforms of gate pulses.

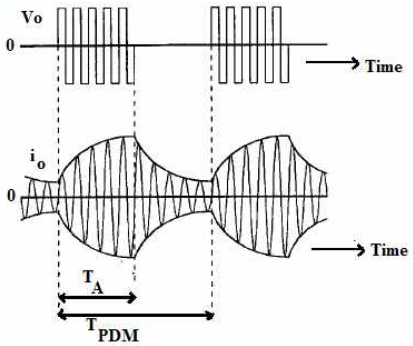


Fig. 5. Theoritical waveforms of output voltage and current with PDM control.

E. Analysis of the PDM Control Algorithm

Power control is an important goal to be achieved in an IH load to maintain a required temperature. The power input to the working coil of an IH load has to be controlled to control the heating of the work piece. Conventionally, this is achieved by the control of the class-D inverter using the PWM technique. In the conventional PWM based power control, the output power is controlled through D_{PWM}. In the PWM scheme, D_{PWM} is the control variable for continuous power regulation. A variation of D_{PWM} causes a violation in the soft switching operation which leads to higher switching losses and reduced output power. A pulse modulation technique called VDC PDM with frequency tracking using a PLL for power control is proposed in this paper. The principle of the PDM is to control the switching of the inverter by the pulse density control method, in which the output power control is done through controlling the ratio of the continuous pulse-on signal and the continuous pulse-off signal.

The main advantage of PDM is its linear dependency on the on-time of the output power. The basic idea of the proposed PDM control is that, by assuming a control cycle of time (T_{PDM}), the inverter transmits power to the load in T_A time and it stops working in the remaining (T_{PDM}-T_A) time. Thus the output power is related to the impulse density. In this way the output power can be changed by changing the pulse density. The PDM based gate signals for switches S_1 and S_2 are shown in Fig.4. When compared with conventional PWM control operation, the PDM operation reduces the switching losses because the MOSFET is always turned on and off under zero voltage during resonant operation.

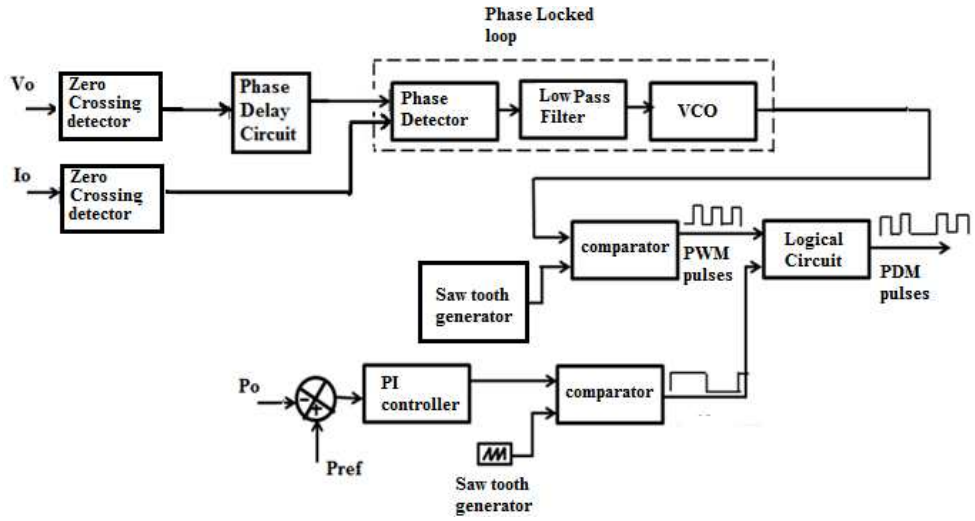


Fig. 6. Block diagram of control scheme for class-D inverter.

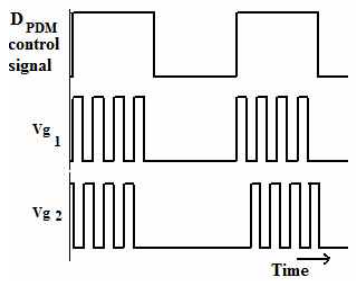


Fig.7. D_{PDM} control signal and gate pulses to S_1 and S_2.

The output voltage and current waveforms of the class-D inverter with the PDM control are described in Fig.5 with the assumption that the quality factor of the resonant circuit is finite. Here, the T_{PDM} of the PDM pattern is long enough to make the amplitude of the resonant current fluctuate. The envelope of the resonant current shows that the first-order response though the series resonant circuit is of a second-order system.

A power analysis of the class-D inverter with the PDM control is given below. The envelope of the resonant current (i_E) is given by:

$$i_E(t) = I_m\left(1 - e^{\frac{T_A}{\tau}}\right) + I e^{-\frac{t}{\tau}} (0 \le t \le T_A) \tag{37}$$

$$i_E(t) = i_1(T_A) e^{-\frac{t-T_A}{\tau}} (T_A \le t \le T_{PDM})$$

$$I = I_m \frac{1 - e^{-\frac{T_A}{\tau}}}{1 - e^{-\frac{T_{PDM}}{\tau}}} \tag{38}$$

I_m is the maximum current in full-power operation, and I is the initial value of the envelope i_E. If Q_L is infinite, the amplitude of the resonant current is in proportion to the pulse density.

$$\lim_{\tau \to \infty} i_E = I_m\left(\frac{T_A}{T_{PDM}}\right) \tag{39}$$

In the PDM, the average output power (P) is obtained by multiplying V_d and i_E as, follows:

$$P = \frac{1}{T_{PDM}} \int_0^{T_A} \frac{2}{\pi} V_d i_E(t) dt$$

$$= \frac{2}{\pi} V_d I_M \frac{T_A + \tau_e^{-\frac{T_A}{\tau}} - \tau}{T_{PDM}}$$

$$+ \frac{2}{\pi} V_d I_m \frac{\tau}{T_{PDM}} \frac{e^{\frac{T_A}{\tau}} - 1}{e^{\frac{T_{PDM}}{\tau}} - 1} \left(1 - e^{-\frac{T_A}{\tau}}\right) \tag{40}$$

If the total time T_{PDM} of the PDM operation is much smaller than the time constant (τ), the amplitude of the resonant current is in proportion to the pulse density. As a result, no fluctuation occurs in the amplitude of the resonant current. Thus, the output power is in proportion to the square of the pulse density, as given by:

$$\lim_{\tau \to \infty} P = \frac{2}{\pi} V_d I_m \left(\frac{T_A}{T_{PDM}}\right)^2 \tag{41}$$

When $T_{PDM} >> \tau$, the output power is in proportion to the pulse density because the resonant current becomes a discontinuous waveform.

$$\lim_{\tau \to \infty} P = \frac{2}{\pi} V_d I_m \left(\frac{T_A}{T_{PDM}}\right) \tag{42}$$

The effective IH load power is adjusted by controlling the ratio between the "on" and "off" periods. The PDM duty cycle (D_{PDM}) is given by the following equation:

$$D_{PDM} = \frac{T_A}{T_{PDM}} \tag{43}$$

A desired output power can be obtained by a variation of D_{PDM}. The term D_{PDM} is also called a modulation index or

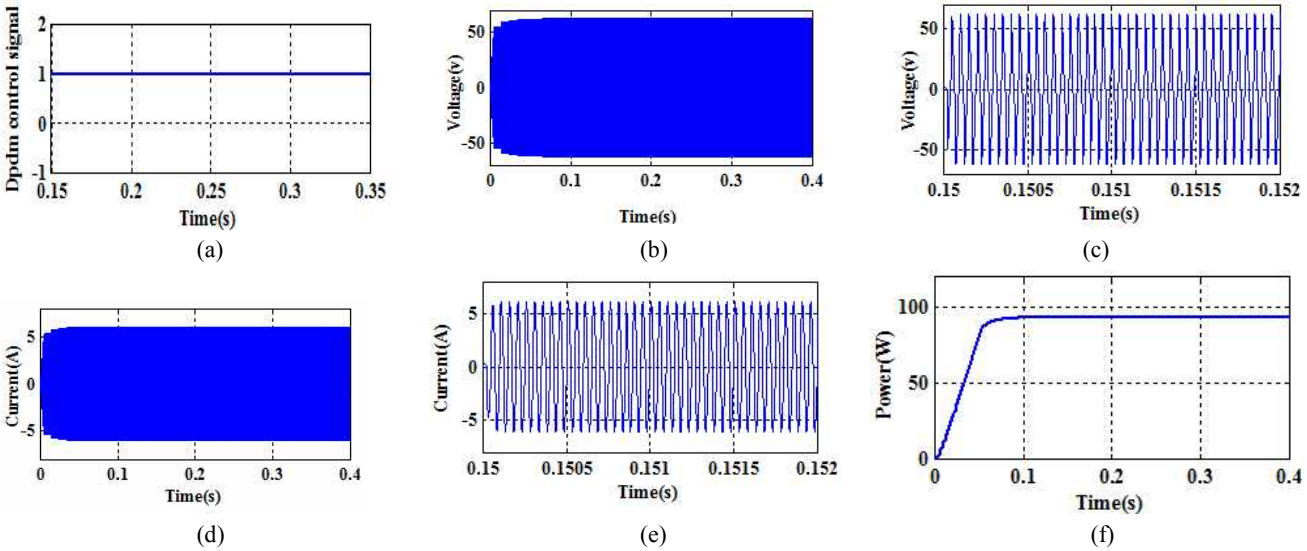


Fig. 8. (a) D_{PDM} control signal for 100% $D_{PDM.}$ (b) Output voltage with 100% $D_{PDM.}$ (c) Zoomed view of the output voltage with 100% $D_{PDM.}$ (d) Output current with 100% $D_{PDM.}$ (e) Zoomed view of the output current with 100% $D_{PDM.}$ (f) Output power with 100% $D_{PDM.}$

pulse density, and its value determines the output power. In this paper D_{PDM} is considered as a control variable. The desired power ($P_{desired}$) for different load conditions can be obtained as follows:

$$P_{desired} = P_o D_{PDM} \tag{44}$$

$$= \frac{2V_d^2 \cdot \mathrm{Cos}^2\phi}{\pi^2 \cdot R_{eq}} \cdot D_{PDM} \tag{45}$$

In this paper, the maximum output power of the high frequency inverter is obtained for a modulation index value equal to one.

III. Control Scheme

It is necessary to operate an inverter close to the resonant frequency to achieve a reduction in the switching losses. An IH load is modeled by means of a series combination of its equivalent resistance R_{eq} and inductance L_{eq}. These parameters depend on several variables, including the shape of the heating coil, the distance between the work-piece and the IH coil, the temperature, the electrical conductivity, the magnetic permeability, and the frequency. When the load parameters change, there is a change in the resonant condition. It becomes necessary to vary the inverter switching frequency during operation due to changes in the parameters which depend on the resonant frequency of the load circuit. Therefore, the control circuit should employ a frequency tracking system to track the resonant frequency of the newly changed parameters. A tuned frequency tracking system using a phase locked loop (PLL) is used to accomplish the above performance. When a work piece of a different metal is inserted into the IH coil, its geometry, conductivity and permeability cause the inductance of the heating coil to change. Considering the fact that the resonant capacitance is fixed, the tank circuit is driven to its new resonant frequency by tracking the switching frequency of the inverter. The PLL circuit can track the resonant frequency due to its fast dynamic response. Fig. 6 shows a block diagram of the PLL based control circuit developed for the PDM inverter. The proposed control circuit and its detailed operation are explained here. There are three parts that make up the control circuit.

1. A PLL circuit is used for the phase lock control between Io and V_o. A PLL is a device which causes one signal to track another signal. This keeps the output signal synchronized with a reference input signal in terms of frequency and phase. It maintains a switching frequency close to the resonance frequency in order to achieve the ZVS condition. It consists of a phase detector (PD), a low-pass filter (LPF), and a voltage-controlled oscillator (VCO). The zero crossing of the output current signal was compared with the zero crossing of the output voltage signal in order to detect the difference in the phase using the exclusive-OR gate, which is used as the PD. The output signal from the exclusive-OR gate was filtered by an RC low pass filter which is basically a PI compensator to get the average value of the voltage. The average voltage confirms the phase difference between the voltage and the current at load. The output of the PI compensator is the average value of the error voltage which changes the VCOs output frequency of oscillation in order to maintain the phase angle when the parameters of the IH load are varied. When the frequency of I_o and V_o are unequal, the PD gives an output signal which indicates the frequency difference, and when locked it indicates a phase difference. The output signal of the PD is used to shift the VCO toward the lock before capture, and then it holds the frequency in the lock condition. Under the

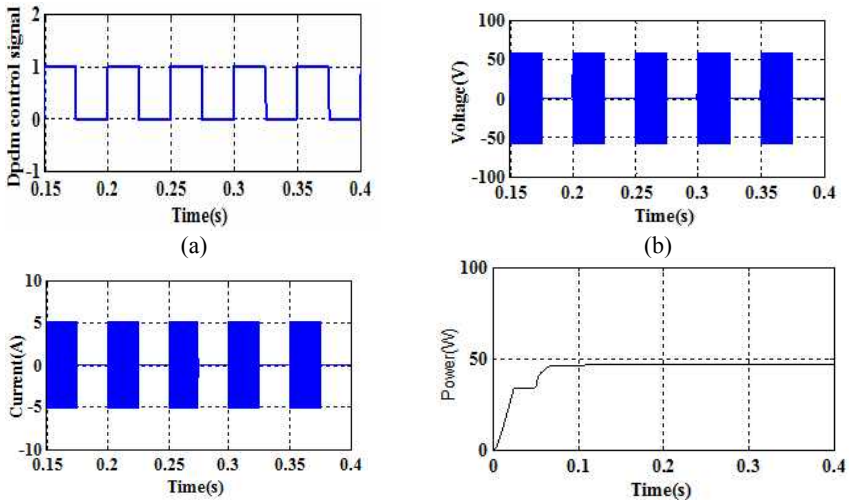


Fig. 9. (a) Control signal for 50% $D_{PDM.}$ (b) Output voltage with 50% $D_{PDM.}$ (c) Output current with 50% $D_{PDM.}$ (d) Output power with 50% $D_{PDM.}$

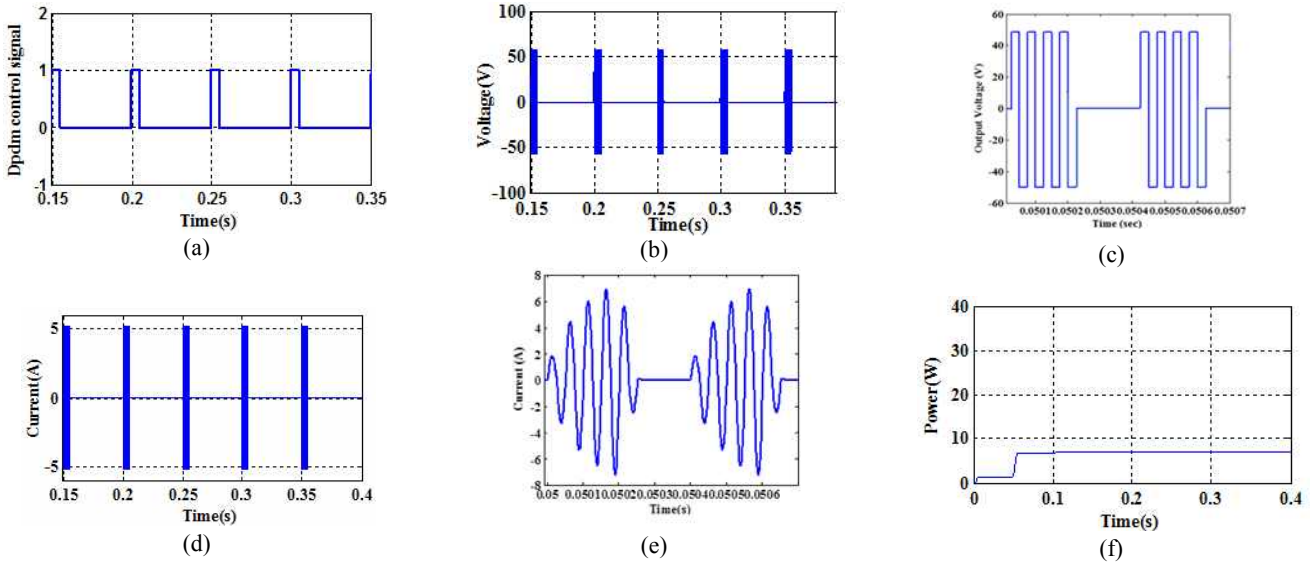
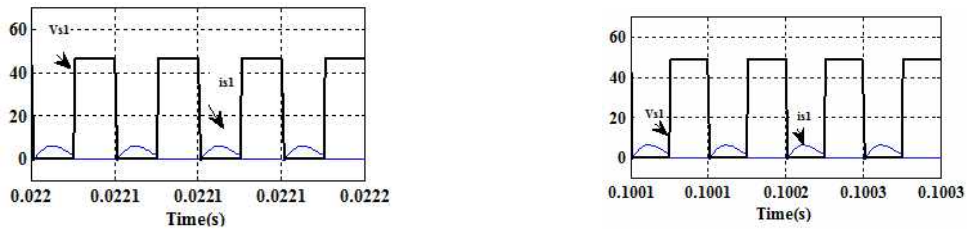


Fig. 10. (a) Control signal for 10% $D_{PDM.}$ (b) Output voltage with 10% $D_{PDM.}$ (c) Zoomed view of output voltage with 10% $D_{PDM.}$ (d) Output current with 10% $D_{PDM.}$ (e) Zoomed view of output current with 10% $D_{PDM.}$ (f) Average output power with 10% $D_{PDM.}$

2. locked condition the I_o and V_o signals have the same frequency. The VCO output signal is directly fed back to the logical circuit to produce PDM pulses.
3. A PDM pulse generating circuit for output power control is the second part of the control circuit. The difference between the reference output power (P_{ref}) and the actual output power (P_o) generates an error signal which is processed through the PI controller and a comparator to obtain a PDM control signal that controls the D_{PDM} of the PDM circuit.

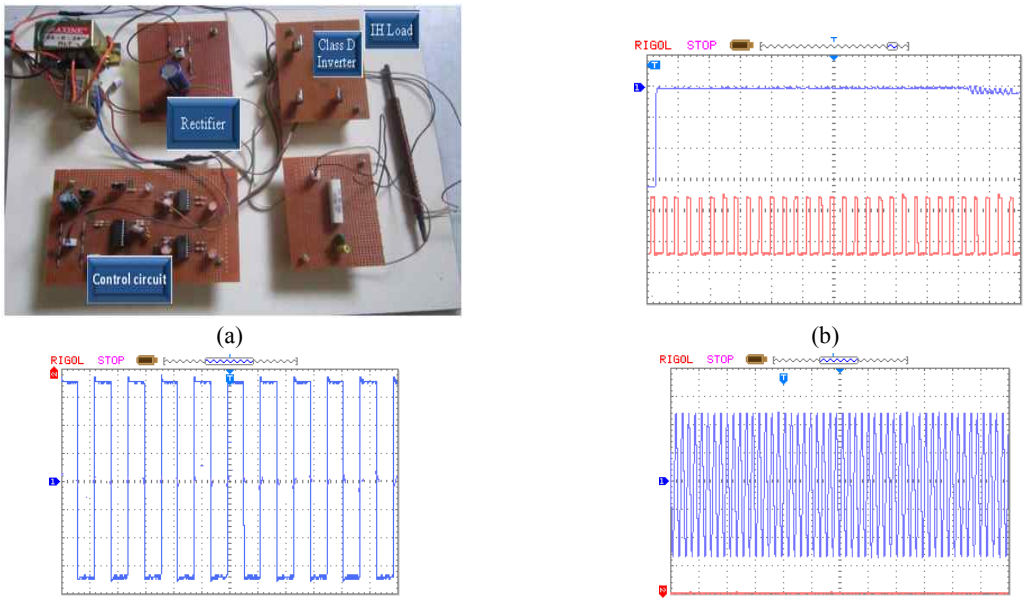
   Based on the control signal D_{PDM}, the PDM gate signals for switches S_1 and S_2 are generated. When the D_{PDM} control signal is high, high frequency switching signals are applied to the switches. On the other hand, when D_{PDM} is low, the gate signals are not applied to the switches as shown in Fig. 7. The low frequency D_{PDM} control signal and the high frequency signal simultaneously undergo zero crossing at the on-off time of the switches. This shows the synchronization between the two frequency signals. The PDM circuit, in combination with the PLL circuit, achieves ZVS operation.

At start up the D_{PDM} is set to unity. Under that condition, the VCO which defines the working frequency of the inverter generates a frequency above the resonant frequency of the load. After this, the control voltage of the VCO gets changed until the working frequency of the inverter is close to the resonant frequency of the new load. The PDM modulation is performed continuously by the feedback loop. As the ZVS condition is guaranteed by the VCO loop, the PDM modulator adjusts the output power.



(a) (b)

Fig.11.(a) Switch voltage (V_{s1}) and switch current (i_{s1}) at 100% D_{PDM} (b) Switch voltage (V_{s1}) and switch current (i_{s1}) at 10% D_{PDM}.



(a) (b)

(c) (d)

Fig. 12. (a) Hardware layout of the prototype. (b) D_{PDM} control signal(100%) and high frequency PWM pulses (0.5v/div,0.01s/div). (c) Experimental output voltage at 100% D_{PDM} (20V/div,0.05µs/div). (d) Experimental output current at 100% D_{PDM} (2A/div,1µs/div).

IV. Discussions of the Simulation and Experimental Results

The validity of the proposed scheme was verified by the simulation and experimental results obtained on a prototype of an IH system. For the simulation a schematic of a class-D inverter and the control circuit have been implemented for time domain simulation using MATLAB. Since the inverter output power depends on the pulse density of the gate signals, a study of the efficiency of the PDM inverter for different values of D_{PDM} must be made.

The design specifications and circuit parameters used for the class-D inverter for an IH load using commercial MOSFET and diode modules are listed in Table I. The parameters are designed according to the considerations given in the previous sections. In Table I it is shown that the switching frequency is greater than the resonant frequency to achieve the ZVS condition. A simulation of a class-D inverter using the proposed scheme is performed with a variation of the load power from 10% to 100% by varying D_{PDM} from 10% to 100%. A high switching frequency (f_s) of 25 kHz is chosen and a low frequency (f_{PDM}) of 25 Hz is chosen to avoid acoustic noise. The simulation is carried out for different values of D_{PDM}.

TABLE I
Specifications of Class-D Inverter and IH Load System

Components	Symbol	Values
Power	P	100 W-500W
Switching frequency	f_s	25 kHz-32kHz
DC-link capacitor	C_f	200 e-6
Resistance	R_{eq}	5-7 ohms
Inductance	L_{eq}	0.0397e-3-0.05 e-3H
Resonant Frequency	f_r	20 kHz-27kHz
PDM frequency	f_{PDM}	25 Hz
Resonant Capacitor	C_r	1.59 e-6F

For verification of the rated output power, the D_{PDM} control signal is generated at 100% of the duty cycle as shown in Fig. 8(a). The simulated result of the output voltage under a full load is shown in Fig. 8(b). A zoomed view of the output voltage is given in Fig. 8(c). Under the full load condition,

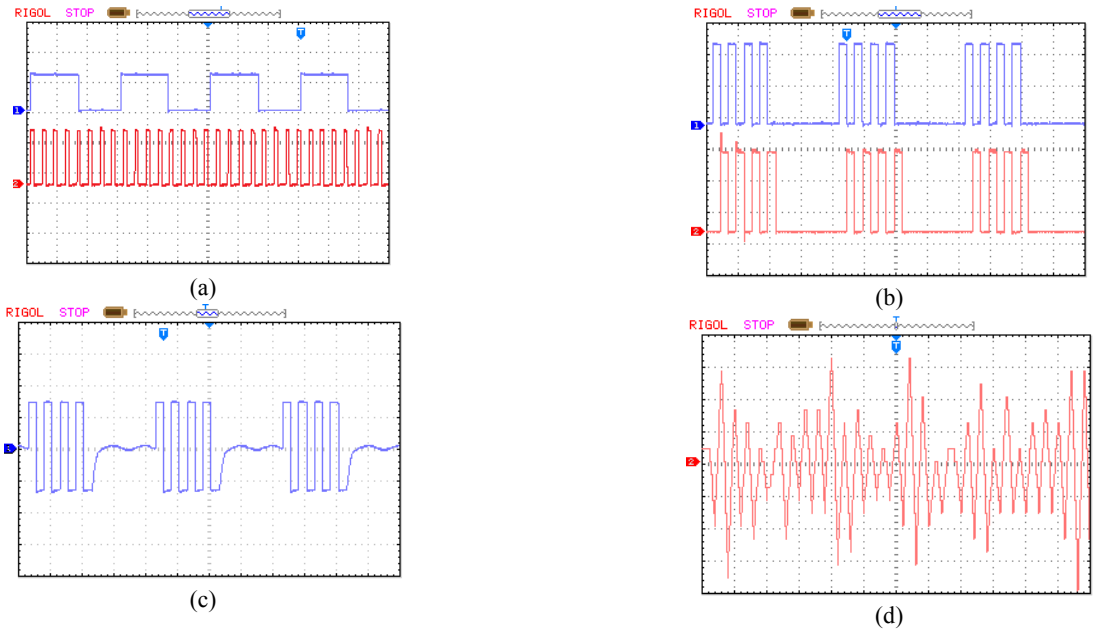


Fig. 13. Experimental results at 10% $D_{PDM.}$ (a) D_{PDM} control signal and high frequency switching signal (1V/div, 0.01s/div) (b) PDM gate signals to S_1 and S_2 (2V/div, 50μs/div) (c) Output voltage at 10% D_{PDM} (40V/div,50μs/div) (d) Output current at 10% D_{PDM} (2A/div,25μs)

the output current flows continuously due to the 100% D_{PDM} as shown in Fig. 8(d). A zoomed view of I_o is given in Fig. 8(e). The output power corresponding to the 100% D_{PDM} is shown in Fig. 8(f). It can be observed that for a modulation index value equal to one, the maximum output power of the inverter is obtained. Gate pulses are generated with a D_{PDM} of 50% of the duty cycle. The corresponding control signal is shown in Fig. 9(a). The simulated results of V_o and I_o at a 50% D_{PDM} are shown in Figs. 9(b) and 9(c), respectively. It can be observed from the waveforms that

V_o and I_o are discontinuous in nature. When D_{PDM} is 50%, the average current gets lower due to the discontinuous flow of I_o. This causes a decrement in the average output power as shown in Fig. 9(d). There are no current spikes because the high frequency and low frequency PDM switching signals are synchronized at the on and off time.

The D_{PDM} control signal at 10% is shown in Fig. 10(a). The simulated results of V_o and a zoomed view of V_o at a 10% D_{PDM} are shown in Figs. 10(b) and 10(c), respectively. The corresponding output current I_o and a zoomed view are shown in Figs. 10(d) and 10(e), respectively. With a 10% D_{PDM}, the average output power still gets decreased due to the discontinuous flow of I_o.

Since the switchting frequency is maintained closer to the resonant frequency of the load by the PLL, even with the change in D_{PDM} from 10% to 100%, ZVS of the switch can be achieved during the turn off condition. This can be observed from Figs. 11(a) and 11(b). In both of the waveforms, the rise in the switch current takes place during the zero state of the switch voltage. These waveforms ensure the ZVS turn off operating condition under any power level achieved with variations of the control variable D_{PDM}. Due to the ZVS condition, the switching losses are reduced. This validates the proposed PLL based VDC PDM control strategy applied to a IH system.

To validate the proposed scheme in a class-D inverter circuit, an experimental laboratory setup was fabricated. The class-D inverter is supplied using a full bridge diode rectifier. The rectifier was constructed using four IN5408 diode switches. The class-D inverter was constructed using two power switches for DC-AC conversion. The power switches were MOSFETs (IRF840) which can withstand a maximum voltage and current of 500V and 8A, respectively.

An IH load was built by using a coil having an outer diameter of 110mm and a thickness of 8mm. A work-piece of 100*45mm has been chosen as the heating load. The control circuit for the IH system is implemented with the PDM control strategy using a PIC16F877A micro controller. The hardware layout of the system is shown in Fig. 12(a). The VDC PDM scheme is validated with this hardware setup for a D_{PDM} of 100% and 10%. For a 100% $D_{PDM,}$ high frequency pulses are allowed to the switches without modulation as shown in Fig. 12(b).

The experimental output voltage and output current at a 100% D_{PDM} are shown in Figs. 12(c) and 12(d), respectively, where V_o and I_o continuously deliver the rated output power. The D_{PDM} control signal at 10% and the high frequency signals are shown in Fig 13(a). The switching pulses for switches S_1 and S_2 are shown in Fig 13(b). These pulses are driven through a gate driver circuit (IR2110) to the switches. With the same PDM control signal, the experimental output voltage is shown in Fig. 13(c). The experimental output

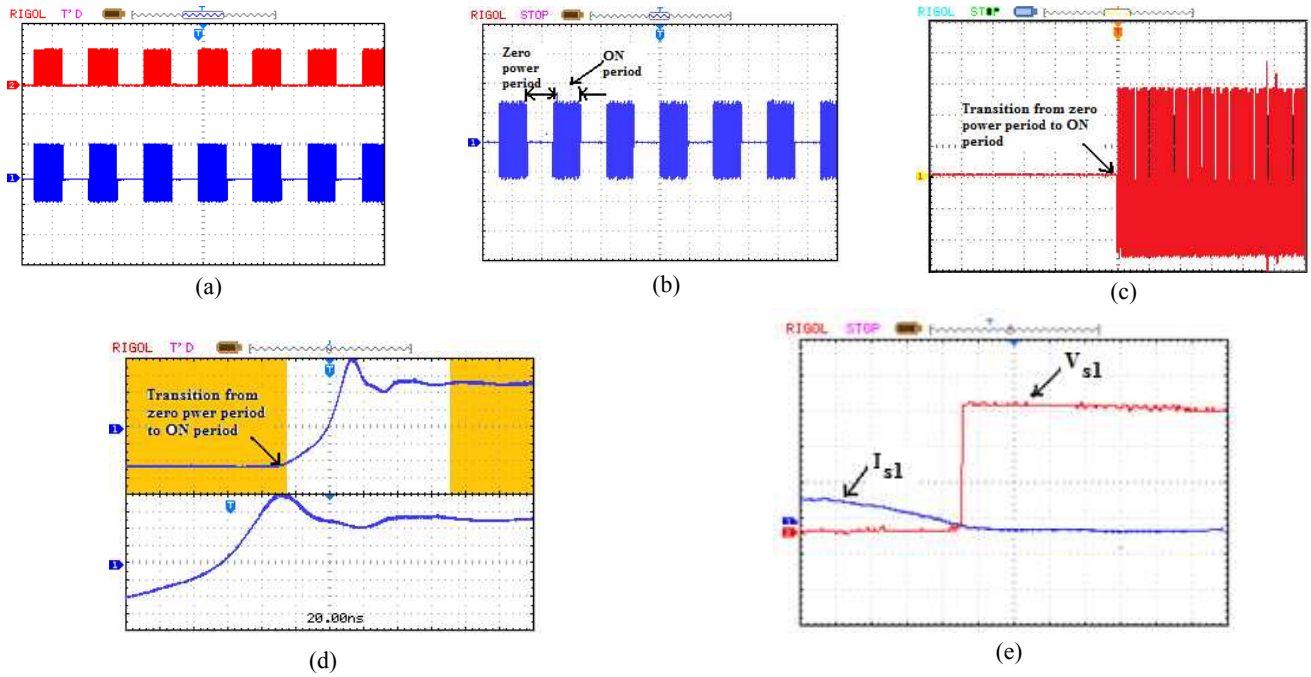


Fig. 14. (a) Gate pulses to the switches $S_1$and the output voltage (32kHz with D_{PDM} of 50%) (5V/div,50V/div,100µs/div). (b) Output voltage of the inverter with 32kHz frequency (40V/div,100µs/div). (c) Zoomed view of the output voltage shown in (20V/div,10µs/div). (d) Transient period for the rise in output voltage shown in (5V/div,1µs/div). (e) Voltage across the switch S_1 (V_{s1}) and Current through the switch S_1 (I_{s1}) (20V/div,5A/div,10µs/div).

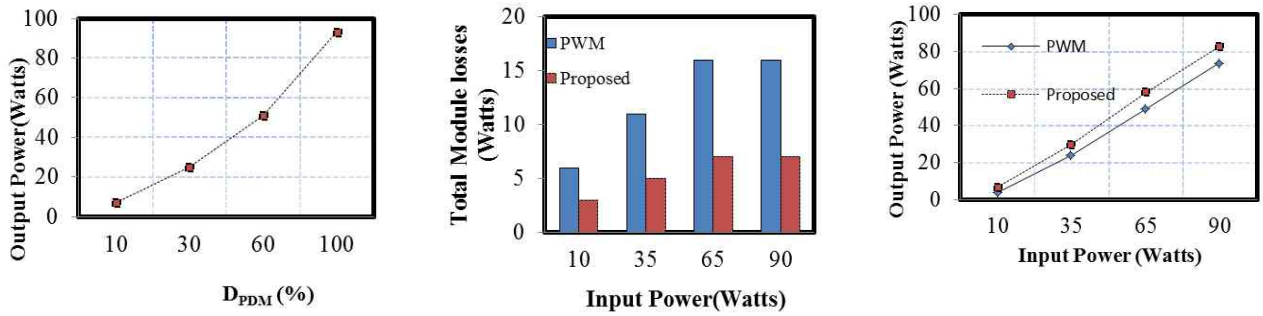


Fig. 15. (a) Variation of output power for different values of $D_{PDM.}$ (b) Variation of inverter module losses for different values of input power. (c) Variation of output power for different values of input power.

current at a 10% D_{PDM} is shown in Fig. 13(d).

The operation of the inverter circuit under a 32 kHz operating frequency with a increased load of 500W has been performed. The corresponding hardware results of the gate pulses and the output voltage are shown in Figs. 14(a) and 14(b), respectively. Fig. 14(c) shows the transition of the output from the zero power period to the power injection period. The transient period for the rise in the output voltage of the inverter can be seen better in Fig. 14(d). It takes 20ns to get settled to the steady state value. The voltage across switch S_1 (V_{s1}) and the current through switch S_1 (I_{s1}) during the turning off condition are shown in Fig. 14(e). It can be observed from the waveform that the switches undergo the ZVS condition at the turn off instant.

Under the fixed frequency operating condition, the presented VDC PDM control ensures a wide power variation with a variation of the control variable D_{PDM} as shown in Fig. 15(a). There is a linear relationship between D_{PDM} and the output power. The variation of the inverter module losses for different values of the input power is shown in Fig. 15(b). With a constant switching frequency, the soft switching condition is maintained at different values of the load power. Since the ZVS condition is maintained in the proposed technique, the inverter losses are reduced when compared to the PWM method. For different input powers, the output power of the conventional PWM and the proposed VDC PDM control are compared in Fig. 15(c). It can be observed that the proposed control scheme improves the output power more than conventional one due to the reduction in switching losses.

The claims of the proposed study compared to the studies discussed in other papers are as follows: 1. The proposed

study analyzes the PLL based VDC PDM control for the widely used half bridge inverter circuit. This paper compares the conventional PLL based PWM and the PDM control logic with respect to losses and output power. 2. In the hardware, the D_{PDM} control signal is generated by a PIC microcontroller. The transient time taken by the control circuit to lock the resonant frequency at start-up duration is less due to the use of the microcontroller. When the locking time is less, the switching losses are also less during the start-up duration. The cost of the microcontroller is also less. 3. In the proposed study, the PDM control circuit adjusts the output power by varying the PDM duty cycle instead of by varying the PDM switching frequency. i.e. The time period of the low frequency signal (T_{PDM}) is not varied. This avoids the problems due to acoustic noise.

V. CONCLUSIONS

This paper presented a PLL based VDC PDM power control scheme in a class-D inverter for an IH load. The design and analysis of the inverter for IH applications are presented. The principle of the proposed control scheme for power control is also discussed in detail. The performance of the proposed control scheme is verified through simulation results. Experimental verification of the VDC PDM scheme is also done with a prototype module. From the simulation and experimental results it can be concluded that the control scheme has the following advantages: a simple configuration, a wide load power control range, reduced switching losses and high efficiency when compared to the conventional PWM scheme. The ZVS operating condition is guaranteed in the load range of 10% to 100%. It has been observed that with a D_{PDM} below 10%, the load current is pulsating and causes the NON-ZVS condition.

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