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An Efficient Control Strategy Based Multi Converter UPQC using with Fuzzy Logic Controller for Power Quality Problems

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Abstract – A custom power device provides an integrated solution to the present problems that are faced by the utilities and power distribution. In this paper, a new controller is designed which is connected to a multiconverter unified power quality conditioner (MC-UPQC) for improving the power quality issues adopted modified synchronous reference frame (MSRF) theory with Fuzzy logic control (FLC) technique. This newly designed controller is connected to a source in order to compensate voltage and current in two feeders. The expanded concept of UPQC is multi converter-UPQC; this system has a two-series voltage source inverter and one shunt voltage source inverter connected back to back. This configuration will helps mitigate any type of voltage / current fluctuations and power factor correction in power distribution network to improve power quality issues. In the proposed system the power can be conveyed from one feeder to another in order to mitigate the voltage sag, swell, interruption and transient response of the system. The control strategies of multi converter-UPQC are designed based on the modified synchronous reference frame theory with fuzzy logic controller. The fast dynamics response of dc link capacitor is achieved with the help of Fuzzy logic controller. Different types of fault conditions are taken and simulated for the analysis and the results are compared with the conventional method. The relevant simulation and compensation performance analysis of the proposed multi converter-UPQC with fuzzy logic controller is performed.

Keywords: UPQC, Fuzzy logic controller, VSC, voltage sag/swell, MSRF theory

1. Introduction

The Flexible AC Transmission System (FACTS) is generally being used for faster damping of power swing, to control the power flow and to securely load the transmission line within their thermal limits. In the distribution system the power electronic devices were used to increase the reliability and quality of the power supplied to consumers. A new technology with the application of power electronics devices in the power distribution system for the benefit of a consumer or a group of consumers is called "Custom Power Devices (CPD)". The use of power electronics devices such as UPQC is connected in combination with both shunt and series in transmission system. The mitigation of the problems such as frequent power interruption, over/under voltages of magnitude and duration within limits; low harmonic distortion and low voltage flicker in the supply side according to IEEE 1159-1995 standard is a challenging issue in power system.

A custom power device provides an integrated solution to the present problems that are faced by the utilities and power distribution. The various compensating devices are Distribution STATCOM (DSTATCOM), Dynamic Voltage Restorer (DVR), and Unified Power Quality Conditioner (UPQC); among these, the UPQC provides good solutions when compared to the other devices. It is a very versatile device that can inject current in shunt side and voltage in series side simultaneously in a dual control mode; hence it can perform both the functions in load compensations. Power quality variations are classified as disturbances or steady state variations. Disturbances pertain to abnormalities in the system voltage/currents due to a fault or some abnormal operations [1].

The Multi-Converter UPQC (MC-UPQC) system has three Voltage Source Converter (VSC) connected to two feeder lines, to compensate the voltage and current imperfection in both feeders [2] that were reported. The shunt and series Active Power Filter (APF) control part is proposed based on Synchronous Reference Frame (SRF) theory with Proportional Integral (PI) controller. A new dynamic proposed model of SRF based control in three phase system under different load consideration are used to improve the Power Quality (PQ) by using multiconverter with power conditioner [3]. The Interline Unified Power Quality Conditioner (IUPQC) consists of series VSC and shunt VSC both joined together by a common dc bus. It can also be used to demonstrate how it is connected between two independent feeders in regulating the voltage

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across a sensitive load from the other feeder [4]. The Generalized Unified Power Quality Conditioner (GUPQC) is a combination of one shunt and two series VSC to compensate current imperfections in one feeder and voltage imperfection in the other two feeders [5].

In the study of reference current generation techniques using VSC based DSTATCOM for reactive power compensation, source current balancing and harmonic mitigation in delta connected for different control techniques such as IRP, SRF and SC theory have been used [6]. The Convertible Unified Power Quality conditioner (CUPQC) is connected to multi-bus/multi-feeder distribution system to mitigate current and voltage interruptions [7]. The control strategy of the UPQC is to focus on the flow of instantaneous active and reactive powers inside the UPQC [8]. The comparison of Unified Power Flow Controller (UPFC) and UPQC are studied [9]. A four wire capacitor midpoint shunt APF with a predictive control technique is used to mitigate the supply current harmonics and the neutral current, thus balanced supply current is achieved [10]. A different type of controller method exists to improve the power quality problems based on the PI control [11-19].

In all the above mentioned techniques PI controller is designed for UPQC. In order to regulate the dc-link capacitor voltage, a conventional PI controller is used to maintain the dc-link voltage at the reference value. The transient response of the PI controller in dc-link voltage is very slow.

This paper proposes the MSRF theory based controller for two feeder 3P3W system fed MC-UPQC. To overcome this problem a better controller is proposed to improve the transient response of the dc-link voltage. The conventional MC-UPQC isalso modified; with the new control techniques to overcome the power quality problems such as voltage / current unbalance, harmonics, voltage sag, swell and interruptions. The effect of series converter is to eliminate the distortions on the supply side voltages due to unbalanced load conditions. The effect of shunt converter is not only to compensate the neutral current but also to make the current balanced on the source side.

2. Proposed MC-UPQC

The MC-UPQC is connected in front of the load to make load voltage and current free from any distortions. A two feeder system is designed to interconnect with MC-UPQC as shown in Fig. 1.

The reactive current drawn from the source will be in such a way that it is in-phase with the feeder voltages. The schematic structure of the proposed MC-UPQC is given in Fig. 2. In this configuration, 'feeder one' is connected to a non-linear load and 'feeder two' is connected to a linear load with MC-UPQC. The MC-UPQC operation is the combination of two series voltage converter and one shunt voltage converter which are connected back-to-back with a

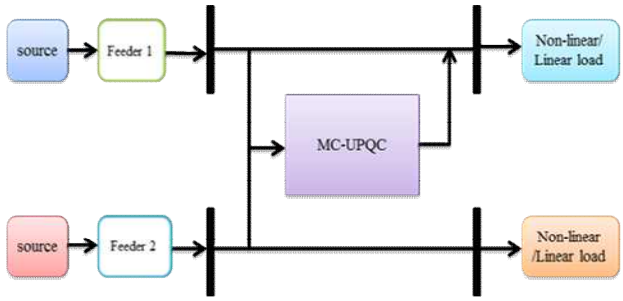

Fig. 1. Configuration of MC-UPQC

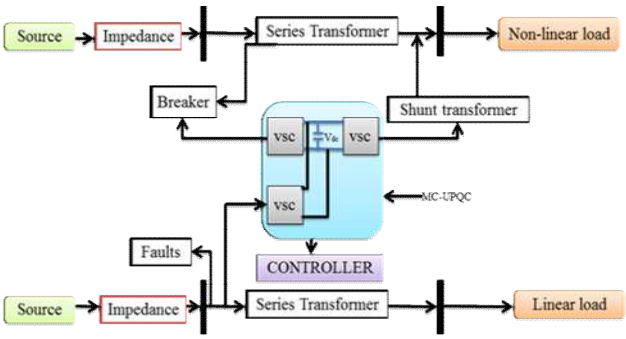

Fig. 2. Schematic structure of the proposed MC-UPQC

common dc-link capacitor, by which it can be controlled independently to compensate the power quality problems. Due to non-linear load in 'feeder one', the system is affected by unbalanced voltage / currents, harmonic distortions in source as well as in load sides of the both feeders.

As per 'feeder two' the load is a linear load hence it has no harmonic distortion, sag, swell, interruption, voltage/ current unbalance, hence it has no effect in both the feeders. The two series VSCs are connected in series between the two feeders through a series transformer, the shunt VSC is connected to 'feeder one' through a shunt transformer in the load side. To avoid the flow of switching harmonics in MC-UPQC the power RC high pass filter with commutation reactor (L) is connected to all VSCs. To achieve this, we examine one suitable structure of the MC-UPQC with Fuzzy Logic Controller (FLC).

3. Proposed Control Strategy

The proposed control strategy aims to generate reference signals for both shunt and series voltage source converter of the MC-UPQC. The control technique is capable of extracting most of the load currents, source voltage distortions, voltage sags, swell and harmonics, voltage and current unbalance, reactive and harmonic component of the both feeders.

3.1 Shunt VSC control scheme

The control algorithm for the shunt VSC block is shown in Fig. 3. The shunt VSC used in simulation is designed by

using MSRF theory with FLC technique. When compared to conventional method [2], the designed system of shunt VSC gives the better compensating of harmonics, reactive components of 'feeder one' load current as well as regulates the common dc-link capacitor voltage. When the supply voltage is distorted, a phase-locked loop (PLL) is used to achieve synchronization with the supply voltage. The distorted supply voltage is sensed and given to PLL to generate two quadrature unit vectors, namely sine and cosine outputs from the PLL in order to compute the 120º phase displacement for each phase. The shunt VSC is based on the unit vector template, based on the concept of MSRF theory. According to this theory, the phase angle of each phase voltage and currents can be extracted as a three independent two-phase system usually given by Π/2 lead or lag. This theory can be applied for three phase balanced system as well as unbalanced of each phase system independently.

The three phase load currents for 'feeder one' is transformed into load synchronous reference currents using Eq. (1).

$$\begin{bmatrix} i_{l\_d} \\ i_{l\_q} \\ i_{l\_o} \end{bmatrix} = \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} \begin{bmatrix} i_{l\_a} \\ i_{l\_b} \\ i_{l\_c} \end{bmatrix} \tag{1}$$

Where,

$$\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \frac{2}{3} \begin{pmatrix} \sin wt & \sin(\text{wt}-\frac{2\pi}{3}) & \sin(\text{wt}+\frac{2\pi}{3}) \\ \cos wt & \cos(\text{wt}-\frac{2\pi}{3}) & \cos(\text{wt}+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2}$$

The fundamental direct axis component current is transferred into dc quantities using 2nd order low-pass-filter and it is added to the fuzzy logic output to generate a new reference shunt feeder currents in Eqs. (3) & (4).

$$i_{f-d}^{ref} = \overrightarrow{i_{ld}} + \Delta I_{dc} \tag{3}$$

$$i_{f-d}^{ref} = i_{l\_q} \tag{4}$$

The power received from the dc link capacitor through the series inverter and switching losses can be used to decrease the average value of dc bus voltage. All other distortions like unbalance conditions and sudden change in load current can also result in oscillations in dc bus voltage.

In order to overcome the error between the desired capacitor voltage and measured values, both are applied to fuzzy logic controllers. The output controlling signal is applied to the current control system of shunt VSC which stabilizes the dc capacitor voltage by receiving required

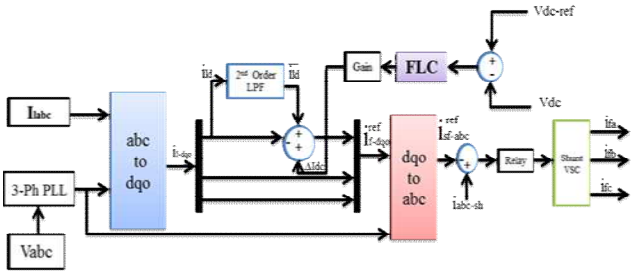

Fig. 3. SRF based control strategy of the shunt VSC

power from the source. The direct component of the feeder current is subjected to load direct dc components and quadrature components of the feeder current is subjected to zero, it means there is no harmonic current and reactive component in 'feeder one'. The new reference shunt feeder currents in Eqs. (3) & (4) are transformed back to the 'abc' reference currents.

$$\begin{bmatrix} i_{f-a}^{ref} \\ i_{f-b}^{ref} \\ i_{f-c}^{ref} \end{bmatrix} = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \begin{bmatrix} i_{f-d}^{ref} \\ i_{f-q}^{ref} \\ i_{f-0}^{ref} \end{bmatrix} \tag{5}$$

The shunt currents are added to the abc reference frame currents and it is sensed by the relay to control the currents. The compensation currents of shunt VSC are directly given to controller part is shown in Fig. 3.

3.2 Series VSC control scheme

The control algorithm for the series VSC block is shown in Fig. 4. The series VSC is proposed using MSRF theory with the improved PWM generator are proposed in this paper.

Compared to conventional method [2], the proposed system of series VSCs gives the better compensation of voltage sag, swell and interruptions in 'feeder two' alone, voltage distortions, harmonic distortions and load voltage unbalance in both feeders. The series VSC block is based on the unit vector template by the new MSRF theory. The distorted three-phase supply voltages were sensed by PLL to generate two quadrate unit vectors. The three phase load voltages are transformed into load synchronous reference voltages using Eq. (6).

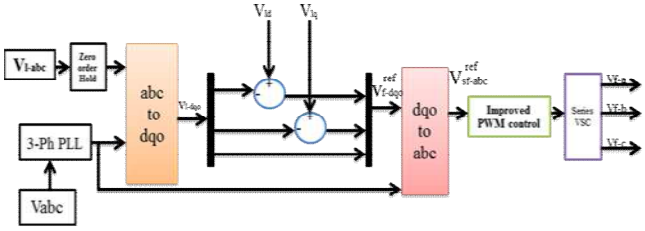

Fig. 4. SRF based control strategy of the series VSC

$$\begin{bmatrix} v_{l\_d} \\ v_{l\_q} \\ v_{l\_o} \end{bmatrix} = \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} \begin{bmatrix} v_{l\_a} \\ v_{l\_b} \\ v_{l\_c} \end{bmatrix} \quad (6)$$

Where, $$\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \frac{2}{3} \begin{pmatrix} \sin wt & \sin(\text{wt}-\frac{2\pi}{3}) & \sin(\text{wt}+\frac{2\pi}{3}) \\ \cos wt & \cos(\text{wt}-\frac{2\pi}{3}) & \cos(\text{wt}+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (7)$$

According to series control objective, where the supply voltage is concerned the load voltage must be kept sinusoidal with constant amplitude. So, the expected load synchronous reference 'dqo' voltages is subtracted to the $V_{l\text{-}dqo}$ in Eq. (8) and its compensation reference feeder dqo voltages is transformed back to the synchronous reference feeder voltages using Eq. (9).

$$\begin{bmatrix} v_{f-d}^{ref} \\ v_{f-q}^{ref} \\ v_{f-o}^{ref} \end{bmatrix} = \begin{bmatrix} v_{l\_d} \\ v_{l\_q} \\ v_{l\_o} \end{bmatrix} - \begin{bmatrix} v_{l-d}^{\exp} \\ v_{l-q}^{\exp} \\ v_{l-0}^{\exp} \end{bmatrix} \quad (8)$$

$$\begin{bmatrix} v_{f-a}^{ref} \\ v_{f-b}^{ref} \\ v_{f-c}^{ref} \end{bmatrix} = \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} - \begin{bmatrix} v_{f-d}^{ref} \\ v_{f-q}^{ref} \\ v_{f-o}^{ref} \end{bmatrix} \quad (9)$$

The compensation synchronous reference abc voltages are forwarded to the improved PWM generator. The output of the PWM generator compensation voltage is directly given to control part of series VSC as shown in Fig. 4.

3.3 New source controller

The design of the new source controller which gives the supply voltage to the system block diagram is shown in Fig. 5. In this controller six sine waveforms (SW) are considered in continuous mode operation, it is modified by the change of amplitude; angular frequency and phase sequence to get the discrete sine waveform. The sine wave determines the computational technique used the parameters in the two types are related Eqs. (10) & (11).

$$S_p = 2\Pi/(\text{ft}+\Phi)+B \quad (10)$$

$$N_{os} = (\text{P}*\text{S}_\text{p})/2\Pi \quad (11)$$

$$S_o = V_{in}(\text{ft}+\Phi)+B \quad (12)$$

Where,

S_p = Samples per period; f = Frequency
t = Time period; B = Bias; Φ = phase angle

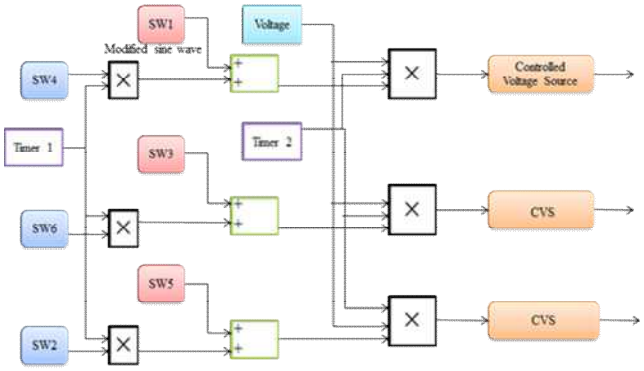

Fig. 5. Block diagram of Source controller

N_{os} = Number of offset samples
P = Phase sequence; S_0 = Signal output
V = sine wave amplitude.

The signal output equation of the sine wave is given in Eq. (12). The bias value is considered as zero, with phase degree of 120º phase shift. The modified SW1, SW 3, SW5 is connected with timer 2 (t_2). Similarly the SW4, SW 6, SW2 is connected with timer 1 (t_1). The SW1, SW4 are added and the output of the signals is multiplied by phase voltage and it is sensed signal to CVS. The three phase source voltage is generated by using below Eqs. (13), (14) & (15).

$$S_a = V_p[\text{SW}1+(\text{SW}4*\text{t}_1)]*\text{t}_2 \quad (13)$$

$$S_b = V_p[\text{SW}3+(\text{SW}6*\text{t}_1)]*\text{t}_2 \quad (14)$$

$$S_c = V_p[\text{SW}5+(\text{SW}2*\text{t}_1)]*\text{t}_2 \quad (15)$$

Where, V_p is the phase-phase rms voltages, t_1 and t_2 are the timers to generate a signal changing at a specified time. Assume SW1, SW3, SW5 are upper switches and SW4, SW6, SW2 are lower switches.

In this paper, controlled voltage source converts the simulink input signal into an equivalent voltage source. The generated voltage is driven by the input signal of the block, and then it initializes the circuit with a specific AC to DC voltage [20]. To start the simulation in steady state, the block input must be connected to a signal starting as a sinusoidal or dc waveform corresponding to the initial values.

4. Fuzzy logic controller Scheme

The FLC usually embeds the intuition, human operator, sometimes those of a designer and researcher. The output from the database and the rules of the knowledge base were used to get the inference relation B mentioned in Eq. (16). The fuzzy memberships are designed based on this equation.

$$B^{(p)} = IF\ X_1\ is\ F_1\ AND\ X_2\ is\ F_2\ .....X_n\ is\ F_n\ THEN\ Y\ is\ C^{(p)} \quad (16)$$

Where,

$X_1, X_2.....X_n$ is the input variables vector
Y is the output or control variable
n is the no. of fuzzy variables (N=5)
$F_1, F_2.....F_n$ is the fuzzy sets
P =1, 2, 3....N
N is the number of rules (N=5).

From the given rule base the fuzzy controller has to compute necessary specific input signal conditions that can determine its effective control action. The need of de-fuzzification methods generally depends on the available processing power; that can be performed by several methods in which center of gravity or centroid and height methods are common [21-25].

To design an FLC, the plant control is inferred from the two input state variables, namely error dc capacitor voltage (V_{dc}) and change in reference dc capacitor voltage error (ΔV_{dc})

$$v_{efuzzy} = v_{dc} - v_{dc}^{ref} \quad (17)$$

The proposed structure of a complete FLC is given in Fig. 6. Actual crisp input values and its approximate are nearly closer to respective universes of its course. If the fuzzified inputs are described by singleton fuzzy sets, then the elaboration of this controller is based on the phase plan. The Fuzzy control rules are designed for a fuzzy set of the control input in each combination of fuzzy sets for V_{dc} and ΔV_{dc} through which a very small amount of real loss is required for voltage regulation taken as the output from the FLC. The input and output variables are converted into linguistic variables.

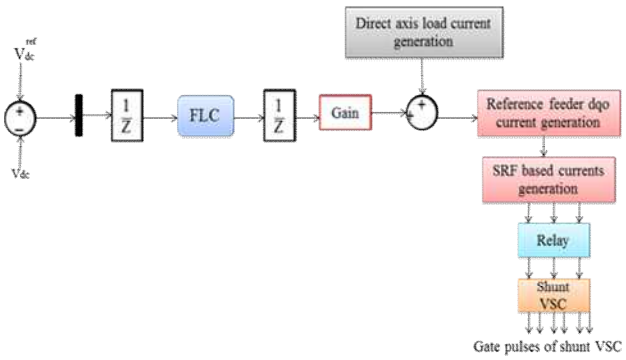

Fig. 6. Proposed structure of a complete fuzzy logic controller

Table 1. Rule based for voltage control

ΔVdc → / Vdc ↓		INPUT 2				
		NL	NM	ZR	PM	PL
INPUT 1	NL	NL	NL	NM	NM	ZR
	NM	NL	NM	NM	ZR	PM
	ZR	NM	NM	ZR	PM	PM
	PM	NM	ZR	PM	PM	PL
	PL	ZR	PM	PM	PL	PL

The direct axis load current is added to the fuzzy logic output and it is forwarded to reference feeder dqo current. The MSRF based currents are directly given to relay and it is senses a control signal to shunt VSC control circuit.

In this paper, instead of using conventional (PI) controller mentioned in references a FLC is being used for its transient response to make MC-UPQC very fast in reducing the total harmonic distortions on source and load side voltages as well as currents on both the feeders. Here five labels of fuzzy subsets; negative large (NL), negative medium (NM), zero (ZR), positive medium (PM), positive large (PL). The control rule base table is shown in Table 1. In which the row and column represents the error and its changes respectively.

5. Results and Discussion

The performance of the proposed system with new control strategy has been analysed and compared with the conventional system. The proposed control system gives better simulation results, as expected. The same model is re-defined with some modifications and also incorporated with FLC and this is realized using the MATLAB/Simulink software. The MC-UPQC along with MSRF theory is connected with two feeder system to compensate in terms of voltage sags, swell, interruptions. To reduce the total harmonic distortion and load current is performed effectively. Design of new source controller simulation circuit diagram is shown in Fig. 7.

5.1 MC-UPQC when connected to feeder 1

The performance of the MC-UPQC which is connected to ‘‘feeder one’’ with proposed control techniques is analyzed and the simulation results are shown in Figs. 8 - 10. The MC-UPQC is turned on at time t=0.02 sec. The

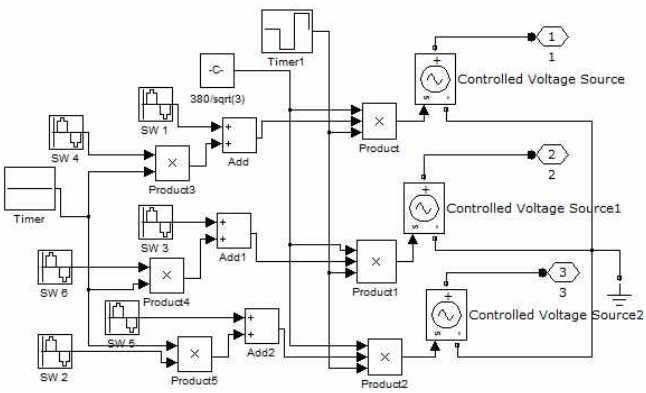

Fig. 7. Simulink model of new source controller

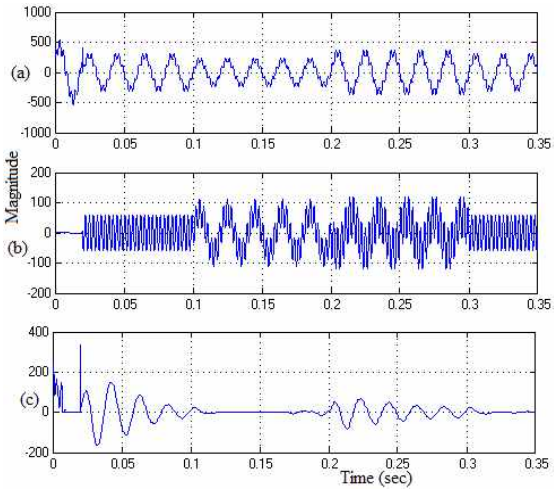

Fig. 8. Simulation results of (a) BUS 1, (b) series compensation, and (c) load 1 voltage in Feeder 1.

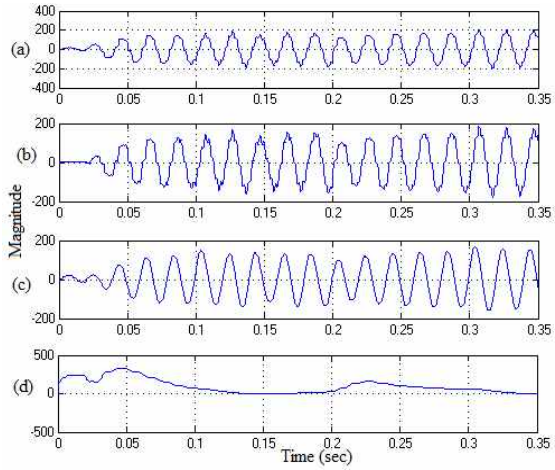

Fig. 9. Simulation results of (a) non-linear; (b) shunt filter (c) feeder 1 currents and (d) dc capacitor voltage.

'feeder one' bus voltage has voltage sag between 0.1 to 0.2 sec duration. Bus1 voltages contain 24.9% sag in the above mentioned time, voltage swell between 0.2 to 0.3 sec duration it contains 119.9% swell. To compensate this voltage sag, swell using MSRF based series and shunt VSC controller with FLC is presented.

THD is reduced in bus 1 voltage from 22.01% to 21.98% and series compensation voltage from 65.91% to 65.80% simultaneously load 1 voltage from 38.90% to 24.46%. The simulation results of bus 1, series compensation and load 1 voltage in 'feeder one' is shown in Fig. 8. The simulation results for 'feeder one' with shunt current, non-linear current, dc-capacitor voltages are shown in Fig. 9. The THD is reduced in 'feeder one' current from 2.73% to 1.89% and shunt filter current from 15.92% to 13.96% simultaneously non-linear current from 13.61% to 12.07%. The harmonic spectrum of 'feeder one', shunt filter, non-linear currents in ''feeder one'' is shown in Fig. 10, these currents are improving very well when compared to

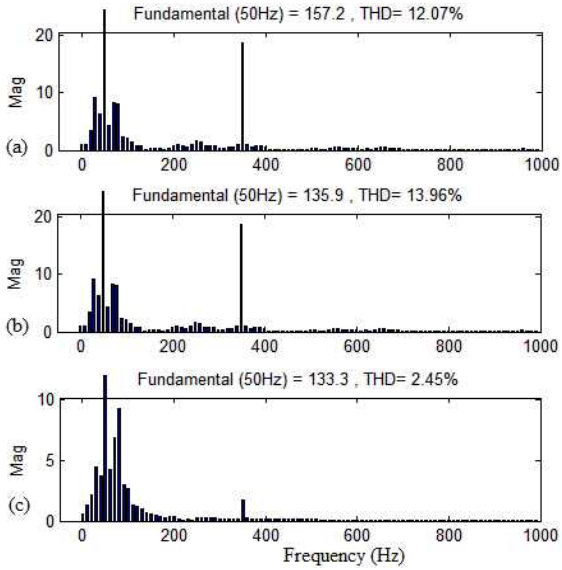

Fig. 10. Harmonic spectrum of (a) non-linear; (b) shunt filter and (c) feeder 1 currents.

conventional system during the power quality problems in between 0.1 to 0.3 sec.

5.2 MC-UPQC when connected to feeder 2

The performance of the MC-UPQC connected to ''feeder two'' with proposed control technique is analyzed and the simulation results are shown in Fig. 11 - 13. At the same time, the 'feeder two' bus voltage having voltage sag between 0.15 to 0.25 sec duration equal to 34.09% is compensated using same proposed control system itself. Bus 2 having a voltage swell between 0.25 to 0.3 sec duration equal to 130%, THD was reduced in bus 2 voltage from 34.97% to 34.96% and series compensation voltage from 64.92% to 65.04% along with load 2 voltage from 4.30% to 3.92%.

The simulation results of bus 2, series compensation and load voltages are shown in Fig. 11. If any type of fault occurred in 'feeder two', the voltage across the linear load will be affected with sag, swell and interruptions. In order to compensate the above problems a shunt VSC is used. In this paper, the system is tested with different types of faults like L-G, L-L and L-L-G faults.

The L-L-L-G fault is applied to 'feeder two' between the 0.3 to 0.4 sec duration. It is observed that the bus 2 voltage is affected between 0.15 to 0.25 sec duration with sag, 0.25 to 0.3 sec duration with swell and 0.3 to 0.4 sec duration momentary interruptions.

The bus 2, series compensation, loads 1 and 2 voltages during the upstream fault conditions simulation results were shown in Fig. 12. The non-linear, 'feeder two' and shunt currents in 'feeder two' simulation results are also shown in Fig. 13. It is founded that THD are reduced in 'feeder two' current from 8.92% to 7.62% and shunt filter current from 8.00% to 7.59% simultaneously non-linear

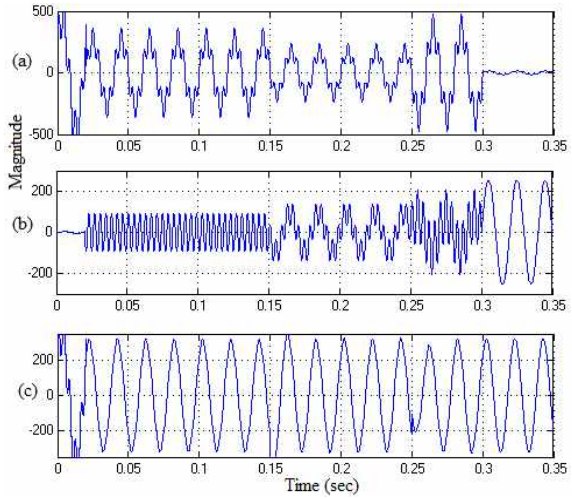

Fig. 11. Simulation results of bus 2, series compensation, load 2 voltages in feeder 2.

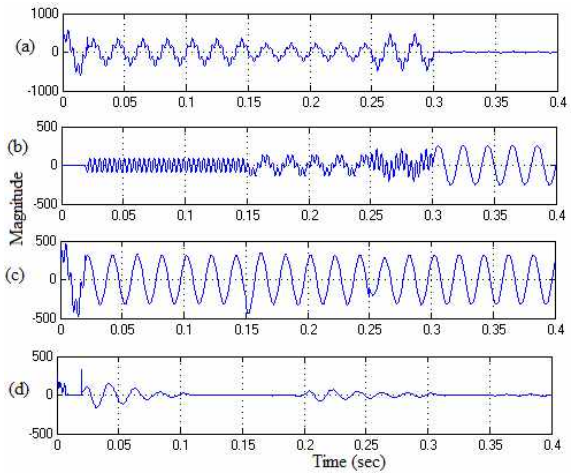

Fig. 12. Simulation results of (a) bus 2; (b) series compensation; (c) load 1 and (d) load 2 voltages during upstream fault.

Table 2. Result of THD in percentage

System voltage/current	Without MC-UPQC	PI controller	FLC
Bus1 voltage(Ut1)	21.92	22.01	**21.98**
Compensation voltage	21.92	65.91	**65.80**
Load 1 voltage	21.95	38.90	**24.96**
Feeder 1 current	15.64	2.73	**1.89**
Shunt filter current	31.05	15.92	**13.96**
Non-linear current	15.64	13.61	**12.07**
Bus2 voltage	35.08	34.97	**34.96**
Compensation voltage	14.11	64.92	**65.04**
Load 2 Voltage	46.49	4.30	**3.92**
Feeder 2 current	9.70	8.92	**7.62**
Shunt filter current	Undefined	8.00	**7.59**
Non-linear current	9.70	8.00	**7.59**

currents from 8.00% to 7.59%.

During the 0.3 to 0.4 sec, the bus 2 voltage has interruption up to 4.2%. The above results are compared

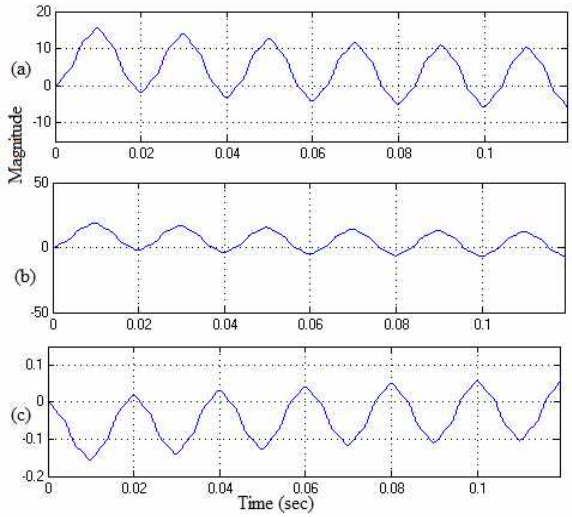

Fig. 13. Simulation results of (a) non-linear, (b) feeder 2 and (c) shunt filter current in feeder 2.

Table 3. Results of power quality issues

Issues	Without MC-UPQC		PI controller		FLC	
	Bus 1	Bus2	Bus 1	Bus 2	Bus1	Bus 2
%Sag	25.01	35.01	25	35	**24.9**	**34.09**
%Swell	119.96	130.5	120	130	**119.9**	**130**
%Interruption	…..	9.3	.....	5	**...**	**4.2**

Table 4. Real and reactive power on load and source side

Power	Without MC-UPQC		PI controller		FLC	
	Load	Source	Load	Source	Load	Source
P(W)	13.82	1.745	466.6	45.23	**1479**	**53.42**
Q(VAR)	13.58	13.58	1170	-4.827	**1792**	**-22.96**

with the conventional and proposed control system. THD results are shown in Table 2 and voltage sags, swell, interruption is calculated according to IEEE 1159-1995 standards as shown in Table 3. The active and reactive powers are calculated for both load and source side as given in Table 4. During the load changes, at time t=0.5 the load 1 voltage is doubled and is reduced to half, remaining load is unchanged and dc bus voltage, non-linear current is compensated.

6. Conclusion

The proposed control structure for two feeders 3P4W operating with MC-UPQC is effectively simulated and the results are compared. This scheme efficiently compensates the voltage sag and reduces the total harmonics distortion. The proposed novel control strategy for a three phase three wire system utilizing the MC-UPQC is validated and compared with conventional controller. The Fuzzy logic controller scheme effectively improved the dynamic response of dc link voltage. The MSRF theory has been used in shunt and series VSC part of the proposed control

scheme and helps to compensate the power quality issues.

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