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Cost-Effective APF/UPS System with Seamless Mode Transfer

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Abstract – In this paper, the development of a cost-effective active power filter/uninterruptible power supply (APF/UPS) system with seamless mode transfer is described. The proposed scheme employs a pulse-width-modulation (PWM) voltage-source inverter and has two operational modes. First, when the source voltage is normal, the system operates as an APF, which compensates for the harmonics and power factor while boosting the DC-link voltage to be ready for the disturbance, without an additional DC charging circuit. A simple algorithm to detect the load current harmonics is also proposed. Second, when the source voltage is out of the normal range (owing to sag, swell, or outage), it operates a UPS, which controls the output voltage constantly by discharging the DC-link capacitor. Furthermore, a seamless transfer method for the single-phase inverter between the APF mode and the UPS mode is also proposed, in which an IGBT switch with diodes is used as a static bypass switch. Dissimilar to a conventional SCR switch, the IGBT switch can implement a seamless mode transfer. During the UPS operation, when the source voltage returns to the normal range, the system operates as an APF. The proposed system has good transient and steady-state response characteristics. The APF, charging circuit, and UPS systems are implemented in one inverter system. Finally, the validity of the proposed scheme is investigated with simulated and experimental results for a prototype APF/UPS system rated at 3 kVA.

Keywords: APF, UPS, Voltage sag, Outages, Compensation, Harmonics, Seamless mode transfer

1. Introduction

Owing to the widespread automation of critical processes throughout industry, the importance of precise voltage control and voltage stability has increased dramatically. Sensitive loads are greatly affected by power quality disturbances in electric systems. Supplying an unreliable input power to these devices causes severe losses to customers. Types of input power disturbance include voltage sag / swell and outage caused by a fault in the interconnected power system [1, 2].

The traditional approach has been to use an on-line uninterrupted power supply (UPS) and a dynamic voltage restorer (DVR), possibly with a back-up generator [3]. This is an expensive solution considering that the UPS battery has a lifetime of 2-5 years and is less reliable than the incoming utility power. Generally, if the maximum temperature rating of a capacitor is 85 °C or 105 °C, the lifetime of the capacitor is approximately 5-7 years or 8-10 years, respectively [4, 5]. A DVR for voltage sag does not require an energy storage unit, whereas a DVR for voltage interruption does. One disadvantage is the compensation delay time between the point at which the disturbance begins and that at which the disturbance is compensated for, which is critical to system performance [6]. The major parts of this compensation delay are the detection delay of the voltage sag or interruption and the turn-off time of the thyristor switch. In most cases, an anti parallel thyristor switch has been used as a static bypasses switch (SBS), which requires time to turn off. Therefore, it is impossible to implement seamless transfer from the grid-tied mode to the off-grid mode when a fault (sag, swell, or outage) occurs [7, 8]. The transition between the grid-tied mode and the off-grid mode is achieved only when a grid voltage is normal and during zero-crossing of the source voltage or output voltage. If a fault is detected, the thyristor switch will open at the positive zero-crossing. The time needed to transition from the grid-tied mode to the off-grid mode is no more than one utility period [7]. In the proposed paper, an IGBT switch with diodes, instead of the conventional SCR switch, was used to implement the seamless mode transfer.

The majority of power disturbances are voltage sags that occur because of lightning strikes, accidents, and equipment failure in the distribution grid feeding the plant [9-11]. Therefore, several voltage sag immunity standards such as SEMI F47, CEBMA Curve, and IEC 61000-4-11, -34 were created to improve equipment reliability [12-14]. The existing standards and recommendations provide guide lines to limit the maximum magnitude and duration of the voltage sag.

Fig. 1 shows SEMI F47, a more recent specification developed for the semiconductor industry without using batteries. This standard recommends that semiconductor equipment be designed to operate during a 50% voltage sag for 0.2 s, a 30% voltage sag for 0.5 s, and a 20%

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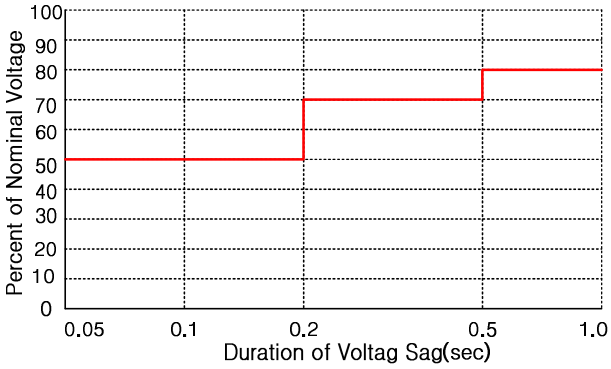


Fig. 1. SEMI F47 voltage sag curve.

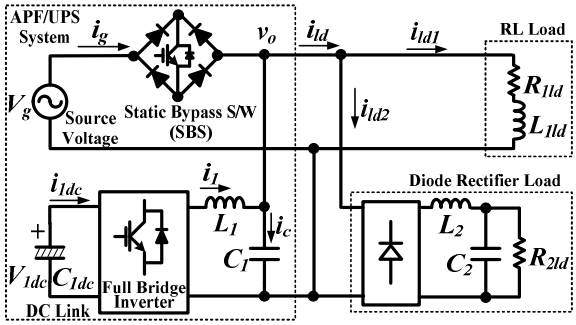


Fig. 2. Circuit diagram of single-phase APF/UPS system with LC filter and static bypass switch.

voltage sag for 1 s. However, the CBEMA standard only recommends that they operate during a 30% voltage sag for 0.5 s. Most sag problems consist of voltage drops of 20-50% and sag duration times of 0.2 s [12].

In this paper, a cost-effective APF/UPS system with seamless mode transfer, which can compensate for voltage drop/swell and outage during a short period of time as well as compensate for the power factor and harmonics of the load current, is proposed.

Compared with conventional APF and UPS systems, the proposed APF/UPS system has the following advantages.

1) When the source voltage is normal, it operates as an APF that controls the power factor, compensates for the harmonics of the load current, and charges the DC-link capacitor to be ready for the disturbance, without an additional DC charging circuit and batteries. Moreover, the system employs a newly proposed and simple algorithm to detect the load current harmonics.
2) When the source voltage is out of range (sag, swell, or outage), the system operates as a UPS that controls the output voltage constantly by discharging the DC-link capacitor. When the source voltage returns to the normal range, the system resumes its operation as an APF.
3) The APF, UPS, and charging circuit can be implemented in an integrated inverter system.
4) A seamless transfer method of a single-phase inverter between the APF mode and the UPS mode is possible. Furthermore, an IGBT switch with diodes, instead of a conventional SCR switch, was used as the SBS. This improves the seamless mode transfer.
5) The proposed seamless transfer algorithm is applicable to single-phase grid-interactive inverters between the grid-connected and stand alone modes.
6) Therefore, a cost-effective method to compensate for the harmonics and power factor of the load current as well as the voltage drop is proposed.

2. System Control

Fig. 2 shows a circuit diagram of a single-phase APF/UPS system with an LC filter and an SBS. The conventional UPS system has an anti parallel thyristor switch as the SBS; however, it requires at most a half cycle to turn off the switch. Therefore, it is impossible to implement seamless transfer between the APF and UPS systems.

In the proposed APF/UPS system, an IGBT switch with diodes is used as the SBS, meaning that the IGBT switch is turned on and off according to the current gate signal.

The APF mode of the system controls the harmonics, charges the DC-link capacitor, and controls the power factor through current injection. The basic theory of the boost converter is the same as that of a single-phase PWM converter. The hardware of a single-phase PWM converter is the same as that of the APF. Therefore, there is no need for an additional DC charging circuit.

In the UPS mode, the system compensates for the output voltage when the source voltage is out of range by discharging the DC-link capacitor. The capacitor (C_1) is needed to make the output voltage a sinusoidal waveform.

2.1 Control of APF and boost converter

The notations used in Figs. 3 and 4 are as follows:

Vg, ig : Source voltage and current
Vo, ild : Output voltage and load current
ild1, ild2 : RL load and diode rectifier load
V1dc, i1dc : DC-link voltage and current
i1, ic : Inverter and capacitor current
ild_ds, *ild_qs*: Load current in the stationary reference frame
ild_de, *ild_qe*: Load current in the synchronous reference frame
ild_de_Hflt, *ild_qe_Hflt*: Harmonic load current in the synchronous reference frame
ild_Hflt : Detected harmonic load current
Vdc_ref : Reference DC voltage
I1_ref : Reference AC current
V1_ref : Reference AC voltage
G_{ioloop} : Open-loop Transfer function of the current controller in the APF mode
Gicloop : Closed-loop transfer function of the current controller in the APF mode

Go(s): Transfer function of the load and the filter capacitor

$\Phi(s)_{IN}$: Closed loop transfer function of the current controller in the grid-tied mode

Gvoloop: Open-loop transfer function of the controller in the grid-tied mode

Gvcloop: Closed loop transfer function of the controller in the grid-tied mode

Vgrms: rms value of the grid voltage

The block diagram of the APF in grid-tied mode is shown in Fig. 3. Fig. 3(a) shows the detection block of the harmonics of the load current, which uses a d-q transformation with an all-pass filter. The system generates a virtual phase with a phase lag of 90° from the measured load current [15]. The virtual phase *ild_qs* is obtained from the measured load current *ild_ds* = -*ild* by using the all-pass filter in the discrete-time domain as follows:

$$I_{ld\_qs}(k) = -cI_{ld\_qs}(k-1) + cI_{ld\_ds}(k) + I_{ld\_ds}(k-1) \quad (1)$$

where

$$c = \frac{T_c\omega - 2}{T_c\omega + 2}$$

The load current i_{ld} is measured and processed in the synchronous d^e-q^e reference frame. Given that the to-be-extracted currents are dc on both the d^e and q^e axes, filtering of the signal with the synchronous d^e-q^e reference is insensitive to any phase errors introduced by low-pass filters. To extract the load current harmonics from the synchronous d^e-q^e reference, implementation of a high-pass filter is realized as (1-LPF). Implementation of the low-pass filter used in the controller is realized with a cutoff frequency of 20 Hz [16]. Detection of the source voltage also requires the use of a d-q transformation with an all-pass filter. The all-pass filter generates a virtual phase with a 90° phase lag from the measured source voltage.

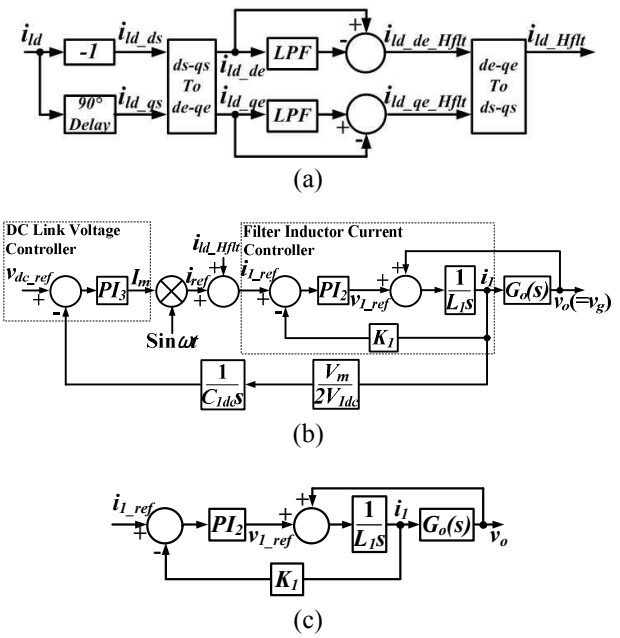


Fig. 3. Block diagram of active power filter in grid-tied mode: (a) Detection block of harmonics of load current; (b) Control block diagram of APF; (c) Filter inductor current controller

The control block diagram of the APF in the grid-tied mode is shown in Fig. 3(b). The figure shows the double-loop feedback control system, which consists of an inner AC-current loop and an outer DC-voltage loop. The filter inductor current controller and DC-link voltage controller are used to force the input current to follow the referenced current waveform and to regulate the output voltage, even under the condition of a sudden load change. In general, the current controller is designed so that the power factor at the supply terminal is close to one. That is, the supply voltage *vg* and current *ig* are required to be as closely in-phase as possible. Furthermore, a detected harmonic load current *ild_Hflt* is added to the current controller to compensate for the harmonic load current.

Fig. 3(c) shows the filter inductor current controller [7, 17]. The closed loop transfer function of the current controller in the grid-tied mode is described as follows:

$$\left(i_{1\_ref} - \frac{v_o}{G_o(s)}\right) \cdot \frac{\left(k_{P2} + \frac{k_{I2}}{s}\right) \cdot \left(\frac{1}{L_1 s}\right) \cdot G_o(s)}{1 - \left(\frac{1}{L_1 s}\right) \cdot G_o(s)} = v_o \quad (2)$$

$$\Phi(s)_{IN} = \frac{\left(k_{P2} + \frac{k_{I2}}{s}\right) \cdot \left(\frac{1}{L_1 s}\right) \cdot G_o(s)}{1 - \left(\frac{1}{L_1 s}\right) \cdot G_o(s) + \left(k_{P2} + \frac{k_{I2}}{s}\right) \cdot \left(\frac{1}{L_1 s}\right)} \quad (3)$$

where *kp2* and *kI2* are the integral and proportional coefficients, respectively, of the current controller (PI_2). The transfer function of the load and the filter capacitor impedance of the inverter, $G_0(s)$, is described as

$$G_0(s) = \frac{R_L}{1 + R_L C_1 s} \quad (4)$$

where R_L is the equivalent resistance of the load. The parameters are as follows: R_L = 14.2 Ω and C_1 = 100 μF.

Substituting (4) into (3) yields

$$\Phi(s)_{IN} = \frac{\left(k_{P2} + \frac{k_{I2}}{s}\right) \cdot R_L}{s^2 L_1 C_1 R_L + s\left(L_1 + \left(k_{P2} + \frac{k_{I2}}{s}\right) \cdot C_1 R_L\right) + k_{P2} + \frac{k_{I2}}{s} - R_L} \quad (5)$$

If the PI gain is adequate, Eq. (5) shows that the inverter in the APF mode is stable. The open loop transfer function of the current controller in the APF mode is obtained as

$$G_{ioloop} = \frac{K_1}{L_1 s}, \tag{6}$$

The closed loop transfer function of the current controller in the APF mode is obtained as

$$G_{icloop} = \frac{\left(k_{P2} + \frac{k_{I2}}{s}\right) \cdot K_1}{L_1 s}, \tag{7}$$

The parameters of the output voltage regulator are designed as follows: K_{p2}=6.5 and K_{i2}=1.22. The phase margin of the compensated current loop gain is 73°.

Fig. 4 shows the simulation results in the case of compensation for the load harmonics and power factor.

In the simulation, V_g, and I_g are the grid voltage and current, respectively; V_o and I_{ld} are the output voltage and current, respectively; I_{ld_Hflt} is the detected harmonic load current; and I_1 is the inverter current. In Fig. 4(a), the grid current is sinusoidal, and the power factor is controlled to be unity because the APF compensates for the load harmonics and the power factor [18, 19].

Fig. 4(b) shows the waveforms of the output voltage and the load current. The figure shows that 50% of the diode rectifier load and 50% of the RL load are applied. Fig. 4(c) shows the detected harmonic load current from Fig. 3(a). Fig. 4(d) shows the inverter current; its waveform is

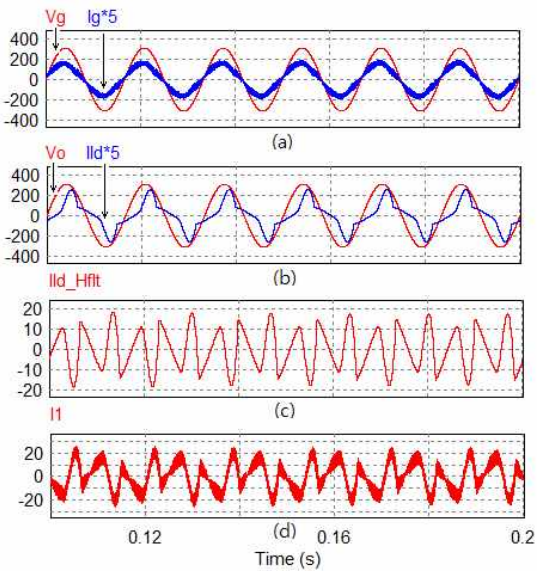


Fig. 4. Simulation results in the case of compensation for load harmonics and power factor: (a) Source voltage and current. (b) Output voltage and current. (c) Detected harmonic load current. (d) Inverter current.

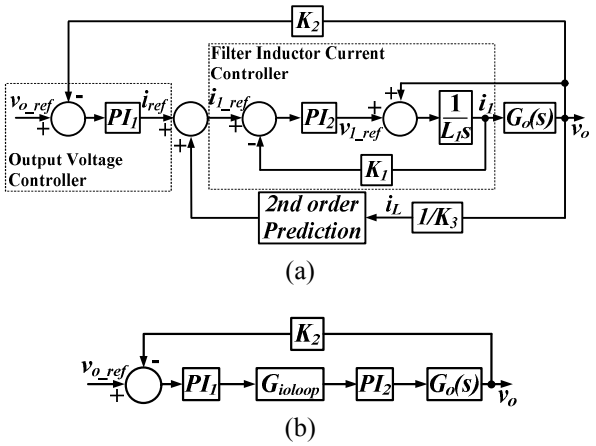


Fig. 5. Block diagram of UPS in off-grid mode: (a) Control block diagram of UPS. (b) Simplified control block diagram

opposite to that of the harmonic load current owing to the compensation of the latter.

2.2 Control of UPS and Inverter

The control block diagram of a UPS in the off-grid mode is shown in Fig. 5(a), where PI_2 refers to the integral and proportional coefficients of the current controller (PI_2). L_1 is the equivalent filter inductor, and K_1 to K_3 are the feedback coefficients of the filter inductor current (i_1), the output voltage (v_o), and the load current (i_L), respectively. The output voltage controller is used to regulate the output voltage, where the reference voltage (v_{ref}) is a sinusoidal waveform and is given by the digital signal processor (DSP).

Fig. 5(b) shows the simplified control block diagram, where K_2 is the feedback coefficient of the grid voltage [20][21]. The open-loop transfer function of the controller in the off-grid mode is described as follows:

$$G_{voloop} = K_2 \cdot G_{ioloop} \cdot G_o(s) \tag{8}$$

The closed-loop transfer function of the controller in off-grid mode is described as follows:

$$G_{vcloop} = A_1 \cdot K_2 \cdot G_{icloop} \cdot G_o(s) \tag{9}$$

where A_1 refers to the integral and proportional coefficients of the voltage controller (PI_1) [22, 23]. The parameters of the output voltage regulator are designed as follows: K_{p1} = 1.2 and K_{i1} =4.8.

2.3 Phase-locked loop and voltage detection

Fig. 6 shows the block diagram of the digital PLL and sag detection block diagram.

The virtual phase V_{gq}^s can be obtained from the measured source voltage $V_{gd}^s = -V_g$ by using the all-pass

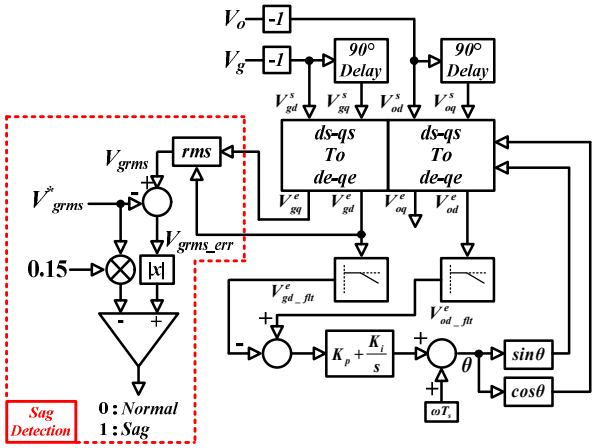


Fig. 6. Digital phase-locked-loop and sag detection block diagram

filter in the discrete-time domain as follows:

$$V_{gd}^{s} = -V_{g} \tag{10}$$

$$V_{gq}^{s}(t) = -kV_{gq}^{s}(t-1) + kV_{gd}^{s}(t) + V_{gd}^{s}(t-1) \tag{11}$$

By using a synchronous rotating reference frame, the rms value of the source voltage is obtained as follows:

$$V_{grms} = \sqrt{\frac{(V_{gd}^{e})^2 + (V_{gq}^{e})^2}{2}} \tag{12}$$

$$V_{grms\_err} = V_{grms} - V_{grms}^{*} \tag{13}$$

If V_{grms_err} is beyond 15% of the absolute source voltage (reference, $0.15 \times V_{g\_rms}^{*}$), the source voltage sag is detected.

2.4 Seamless transfer between APF and UPS

In order to realize seamless transfer from the APF mode to the UPS mode, an algorithm for instantaneous detection of the grid voltage is needed.

When a drop in the grid voltage is detected for one sampling period, the SBS is turned off immediately, and the system is transferred to the UPS mode. The beginning of the output voltage reference starts at the grid voltage of the grid voltage drop.

When the system is transferred from the UPS mode to the APF mode in order to realize seamless transfer, the load voltage must match the magnitude, frequency, and phase of the grid voltage well before connecting to the utility.

The detailed process of the seamless transfer between the two modes is illustrated in the following subsections [8].

2.4.1 APF mode to UPS mode

a) Detect the voltage drop on the utility.
b) Deactivate the APF mode, turn off the SBS, and separate the output voltage from the utility immediately.
c) Confirm that the SBS is completely off and then transition to the UPS mode. In the case of a voltage drop, synchronize v_{o_ref} with v_{g}. In the case of a black out, synchronize v_{o_ref} with the clock signal.
d) The beginning of the output voltage reference starts at the grid voltage at the grid voltage drop.

All changes in the reference current, reference voltage, and SBS occur at a voltage drop and black out. After confirmation that the SBS is completely shut down, a transition is made to the UPS mode. The detection of the grid voltage plays an important role in this transfer [15].

2.4.2 UPS mode to APF mode

a) Detect that the grid is operating under the nominal condition.
b) Adjust *vo_ref* to match the frequency and phase of the grid voltage. The time required to adjust the reference is less than several times the grid period.
c) Once the amplitude and phase of the load voltage and the grid voltage are equal (in one period), the UPS mode is turned off, and the SBS is turned on.
d) After the SBS is turned on, the APF/UPS system is transferred to the APF mode.

To boost the DC-link voltage and compensate for the harmonics and power factor, the reference grid current is increased slowly from zero to the desired value (in both magnitude and phase). When the grid is operating under a nominal condition, and the amplitude and phase of the load voltage and grid voltage are equal, the UPS mode is turned off, and the SBS is turned on. After confirming that the SBS is on, the system is transferred to the APF mode [24].

Fig. 7 shows block diagrams of the APF mode and the UPS mode. The transfer between the two modes is performed by a change in the reference signal. The seamless transfer

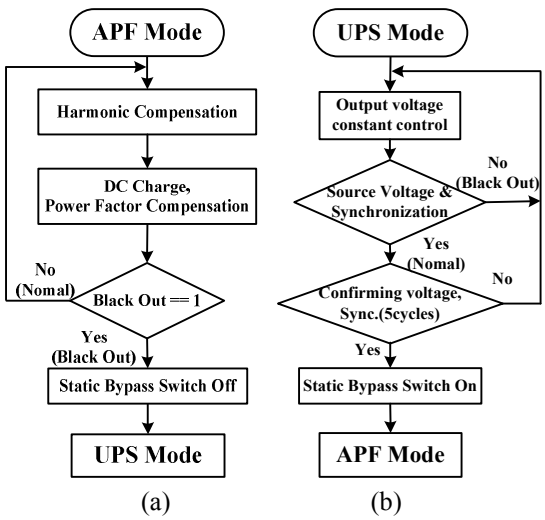


Fig. 7. Block diagrams of the APF and UPS modes: (a) APF mode; (b) UPS mode.

can be easily realized by a DSP.

Fig. 7(a) shows that the APF/UPS system operates as an APF that compensates for the harmonics of the load current, controls the power factor, and charges the DC-link capacitor. When the source voltage is out of range, the system turns off the SBS and transfers to the UPS mode. Fig. 7(b) shows that the system operates as a UPS that controls the output voltage constantly. When the source voltage returns to the normal range, the system waits for five cycles to confirm synchronization, after which the SBS is turned on and the operation mode is changed from UPS to APF. Therefore, a transition from the UPS mode to the APF mode as soon as the source voltage is returned to the nominal value is impossible.

2.5 Design of DC-Link capacitance

To design the DC-link capacitance, the compensation energy, power, and capacitance are expressed as follows:

$$E = \frac{1}{2} \cdot C_{DC-Link} \cdot (Vdc_{DC-Link}^2 - V_{Grid\_Peak}^2)[J], \quad (14)$$

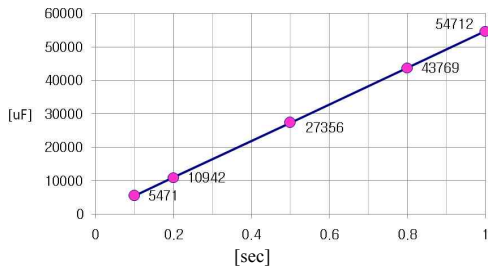
$$P = \frac{C_{DC-Link} \cdot (Vdc_{DC-Link}^2 - V_{Grid\_Peak}^2)}{2 \cdot Conpensation\_time}[W], \quad (15)$$

$$C_{DC\_LInk} = \frac{P \cdot Conpensation\_time}{0.5 \cdot (Vdc_{DC-Link}^2 - V_{Grid\_Peak}^2)}[F], \quad (16)$$

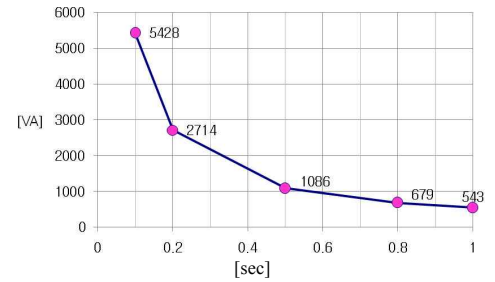
where $V_{dc\ DC\text{-}Link}$ = 442 V, and, V_{Grid_Peak} = 208×sqrt(2)

Fig. 8(a) shows the capacitance depending on the compensation time under the 3-kVA load condition. The system needs a capacitor of 5,471 or 10,942 μF to compensate for 0.1 s or 0.2 s, respectively. Fig. 8(b) shows the rating depending on the compensation time when the capacitance is 9,900 μF. In a real situation, a capacitance of 9,900 μF instead of 10,942 μF is used. Therefore, the compensation time is less than 0.2s. If the system compensates for 0.1s or 0.2s, it can supply a power of 5.4 kVA or 2.7kVA, respectively.

If a supercapacitor is used instead of a conventional electrolytic capacitor for boosting the DC-link voltage, then the compensation time is easily enhanced without additional hardware.



(a)



(b)

Fig. 8. DC-link capacitance depending on compensation time at a rating of 3 kVA: (a) Capacitance versus compensation time; (b) Rating versus the compensation time.

3. Experimental Results

To verify the proposed strategy, the algorithm was implemented with a DSP (TMS320C33). A single 32-bit floating-point DSP with a single-cycle execution time of 13.3 *n*s was used. The laboratory prototype with IGBT modules was a 3-kVA APF/UPS system, and the switching period of the PWM was 91 μs. Moreover, a single-phase diode rectifier and R-L load were included to show the characteristics of harmonic load current elimination and power factor correction. The system parameters are listed in Table 1.

The nominal input voltage was 208 V. Voltage sags were simulated with a tap-changing transformer and switching devices, enabling various voltage sag levels to be generated. In this paper, the source voltage drops from 208 V to 104 V

Table 1. System Parameters

Parameters	Value
Source Voltage (V_g), Rating	207 V, 60 Hz, 3 kVA
Switching Frequency (fs)	11 kHz
DC-link Capacitor (C_{1dc})	9,900 μF
DC-link Voltage (V_{1dc})	442 V
L_1, C_1	0.4 mH, 100 μF
L_2, C_2	0.2 mH, 800 μF
R_{1ld}, L_{1ld} (50%, 100%)	22Ω +44 mH, 11Ω +22 mH (PF = 0.8)
R_{2ld} (50%, 100%)	60 Ω, 30 Ω

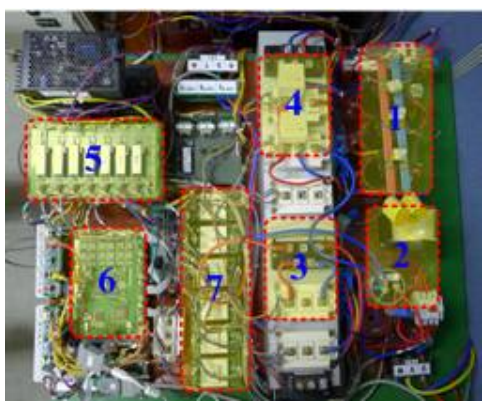


Fig. 9. Prototype of proposed APF/UPS system.

in a sag event. The DC-link voltage was boosted to 442 V.

Fig. 9 shows a prototype of the proposed APF/UPS system. The prototype is composed of a DC-link capacitor (1), an LC filter (2), a static IGBT switch (3), IGBT inverter modules (4), a sensing board (5), a DSP board (6), and gate drivers (7).

3.1 APF mode (DC boost and harmonic compensation)

Fig. 10 shows the start-up in the APF/UPS system when the DC-link voltage increases from 290 Vdc to 442 Vdc under the no-load condition. In this figure, Ch 3 and Ch 4 show that the DC-link voltage follows the reference voltage of 442 V. Although the inverter current (i_1) is 0 before start-up, when the DC-link voltage is increased from 290 Vdc to 442 Vdc, an inverter current of approximately 7-8 to 3-4 A is detected, respectively. After V_{dc} reaches 442 V, an inverter current of approximately 2 A is detected.

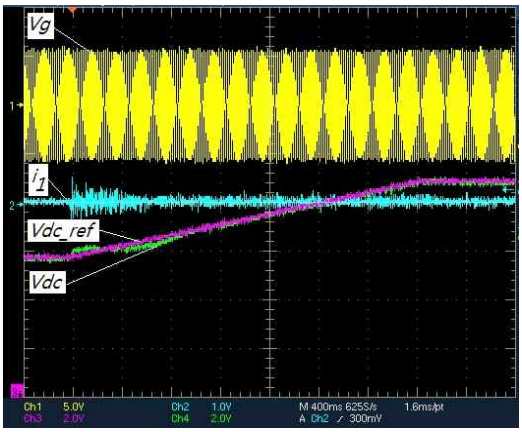


Fig. 10. Start-up in APF/UPS system when the DC-link voltage is increased from 290 to 442 Vdc under no-load condition: Ch 1. V_g: source voltage (250 V/div). Ch 2. i_1: output current (10 A/div). Ch 3. V_{dc_ref}: reference DC-link voltage (100 V/div). Ch 4. V_{dc}: DC-link voltage (100 V/div).

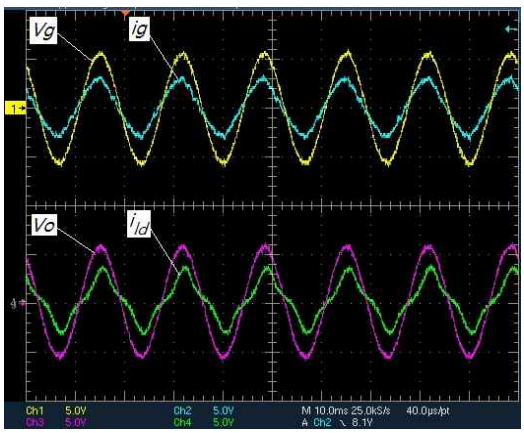


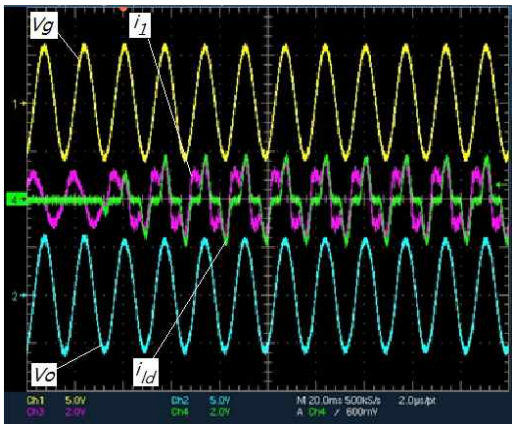
Fig. 11. Experimental results in APF mode: Ch 1. V_g: source voltage (250 V/div). Ch 2. i_g: source current (20 A/div). Ch 3. V_o: output voltage (250 V/div). Ch 4. i_{ld}: load current(20 A/div).

Fig. 11 shows the experimental results when 50% of the diode rectifier load and 50% of the RL load are applied. The source current is sinusoidal, and the power factor is controlled to be unity because the APF compensates for the harmonic load current and the power factor.

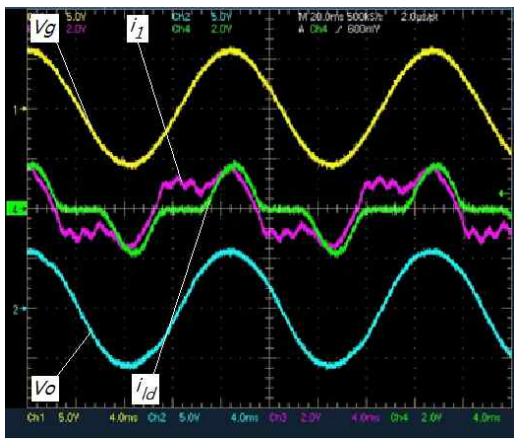
3.2 UPS mode

Fig. 12 shows the experimental results when the load changes from the no-load condition to 100% of the diode rectifier load. Although a diode rectifier load was applied to the system, the output voltage of the UPS was controlled to be sinusoidal and was synchronized with the grid voltage.

Fig. 12(b) shows zoomed-in waveforms under the steady state condition.



(a)

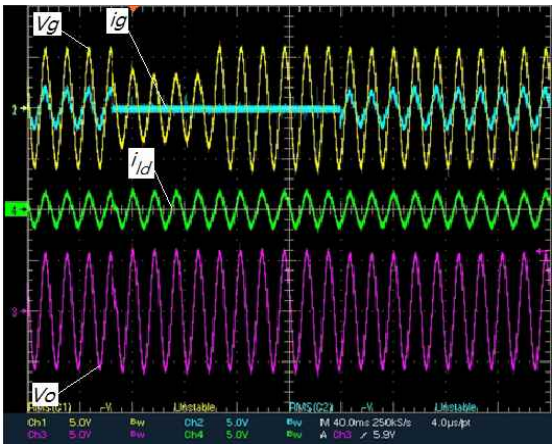


(b)

Fig. 12. Experimental results when the load changes from the no-load condition to 100% of the diode rectifier load: (a) Transient waveforms; (b) Zoomed-in waveforms in steady state. Ch 1. V_g: source voltage (250 V/div). Ch 2. V_o: output voltage (250 V/div). Ch 3. I_1: inverter current (20 A/div). Ch 4. I_{ld}: load current (20 A/div).

3.3 APF/UPS mode transfer (50% voltage sag)

Fig. 13 shows the experimental results when 100% of the R-L load is applied. Fig. 13(a) shows when the IGBT and diodes were used as a static bypass switch. When the source voltage drops by up to 50%, the APF/UPS system cannot adequately operate as an APF system. In this case, the voltage drop is of greater concern than the harmonic current. Thus, the operational mode must be switched from APF to UPS. The system increases the output voltage up to the nominal value as soon as a voltage drop occurs. When the source voltage is returned to the nominal value, several cycles are required to adjust the output voltage to match the grid voltage in both frequency and phase. When the output voltage and grid voltage are synchronized for five cycles, the SBS is turned on, and the operational mode is changed from UPS to APF. However, if the time to confirm synchronization of the output voltage and grid voltage is reduced, the transfer time can be reduced. Fig. 13(b) shows that when the SCR switch was used as the SBS, the output voltage was not fully increased to the nominal value within a half cycle.



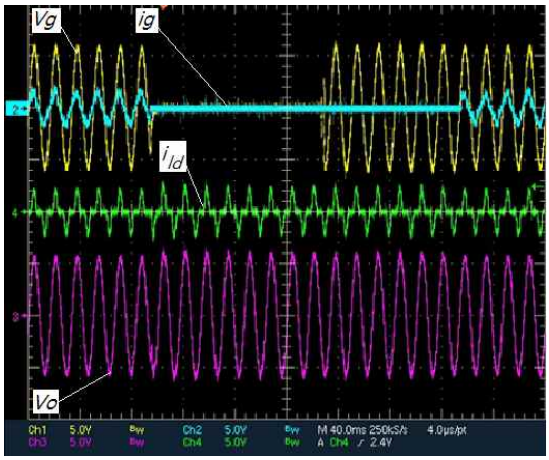
(a)

(b)

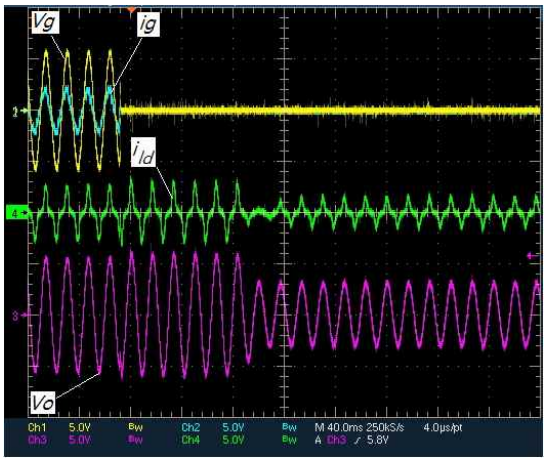
Fig. 13. Experimental results during voltage sag from 207 V to 104 V: (a) When the IGBT and diode were used as a static bypass switch; (b) When the SCR switch was used as a static bypass switch. Ch 1. V_g: source voltage (250 V/div). Ch 2. i_g: source current (50 A/div). Ch 3. V_o: output voltage (250 V/div). Ch 4. i_{ld}: load current (50 A/div).

3.4 APF/UPS mode transfer (in case of outages)

Fig. 14(a) shows the experimental results during blackouts when the rectifier load was applied. Similar to the case of Fig. 13(a), a seamless transfer from the APF to the UPS was implemented. When a voltage interruption occurred, the output voltage was somewhat distorted. The input voltage causes this effect because the blackouts were created by turning off the no fuse breaker (NFB). Fig. 14(b) shows the results of a long blackout. When the DC-



(a)



(b)

Fig. 14. Experimental results during blackouts: (a) Short blackout period; (b) Long blackout period. Ch 1. V_g: source voltage (250 V/div). Ch 2. i_g: source current (50 A/div). Ch 3. V_o: output voltage (250 V/div). Ch 4. i_{ld}: load current (50 A/div).

link voltage drops to less than 320 V, the system outputs 110 V_{ac} to prolong the backup time until the DC-link voltage reaches 160 V_{dc}. This is because most power electronic devices can operate at input conditions of 220 to 110 V_{ac}. If the system outputs 220 V_{ac}, the DC-link voltage should be greater than 320 V_{dc}. However, if the system outputs 110 V_{ac}, the DC-link voltage should be greater 160 V_{dc}. Therefore, the system can prolong the backup time until the DC-link voltage reaches 160 V_{dc}.

4. Conclusion

In this paper, a cost-effective way to compensate for voltage drops was proposed. When the source voltage is normal, the system operates as an APF, which compensates for the harmonics and power factor, while boosting the DC-link voltage to prepare for the disturbance. This renders the additional DC charging circuit and batteries unnecessary. A new algorithm to detect the load current harmonics was also proposed.

When the source voltage is out of range (owing to sag, swell, or outage), the system operates as a UPS that controls the output voltage constantly by discharging the DC-link capacitor. Furthermore, instead of the conventional SCR switch, an IGBT switch with diodes was used as the SBP, and a seamless transfer method for the single-phase inverter between the APF mode and the UPS mode was also proposed. The APF, charging circuit, and UPS systems were implemented in a single-phase inverter system. The control algorithm and mathematical models were described, and the simulated and experimental results were presented to verify the performance of the proposed control strategy.

The validity of the proposed scheme was investigated through simulations and experiments with a 3-kVA APF/UPS system.

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