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Dynamic Reference Scheme with Improved Read Voltage Margin for Compensating Cell-position and Background-pattern Dependencies in Pure Memristor Array

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***Abstract*—In this paper, a new dynamic reference scheme is proposed to improve the read voltage margin better than the previous static reference scheme. The proposed dynamic reference scheme can be helpful in compensating not only the background pattern dependence but also the cell position dependence. The proposed dynamic reference is verified by simulating the CMOS-memristor hybrid circuit using the practical CMOS SPICE and memristor Verilog-A models. In the simulation, the percentage read voltage margin is compared between the previous static reference scheme and the new dynamic reference scheme. Assuming that the critical percentage of read voltage margin is 5%, the memristor array size with the dynamic scheme can be larger by 60%, compared to the array size with the static one. In addition, for the array size of 64 x 64, the interconnect resistance in the array with the dynamic scheme can be increased by 30% than the static reference one. For the array size of 128 x 128, the interconnect resistance with the proposed scheme can be improved by 38% than the previous static one, allowing more margin on the variation of interconnect resistance.**

***Index Terms*—Dynamic reference scheme, read voltage margin, cell-position and background-pattern dependencies, pure memristor array**

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I. INTRODUCTION

Because it becomes more difficult to continue device scaling further in memory technologies, many researchers have been exploring new materials and devices for the next-generation memories. Among them, memristors with resistive switching behavior have gained substantial interest as one of alternative memory devices [1-7]. Memristors are known that they are non-volatile, low power, and very dense. One more advantage of memristors is a possibility that can be implemented by pure memristor array not using any selection devices such as diodes and transistors [8, 9]. This pure memristor array without any selection devices can be very suitable to 3-D integration, because transistors and diodes are much more difficult to be stacked layer by layer, compared to pure memristor array [10-14].

In the pure memristor array, however, we have sneak-path leakage which can flow through the unselected cells. Moreover, some amounts of voltage drop can be caused by interconnect resistance along the row and column lines [2]. The sneak-path leakage and interconnect resistance together degrade the read voltage margin of the selected cell severely.

The amount of degradation of read voltage margin is affected by the background data patterns which are stored in the array. A simple schematic of pure memristor array is shown in Fig. 1(a). In the array, the number of rows

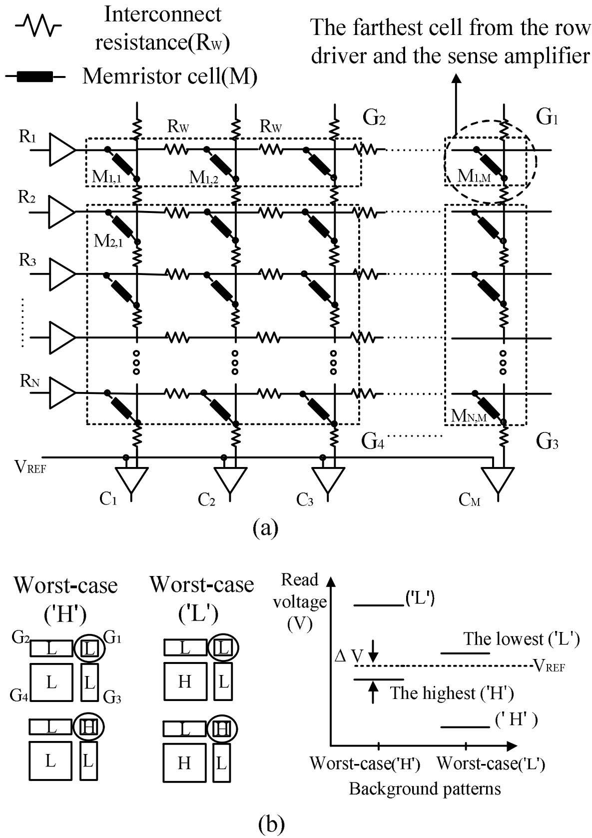


Fig. 1. The simple schematic of pure memristor array with n×m memristors. Here, the number of rows and that of columns are n and m, respectively. (b) The worst-case (‘H’) and the worst-case (‘L’) of the read voltage margin for reading ‘H’ and ‘L’ of the selected cell. The worst-case (‘H’) is the highest (‘H’) read voltage of the selected cell among 8 possible cases of different background patterns. The worst-case (‘L’) is the lowest (‘L’) read voltage of the selected cell with ‘L’ among 8 cases of different background patterns. The worst-case (‘H’) and worst-case (‘L’) represent the two worst-case read voltage margin for reading ‘H’ and 'L‘, respectively. V_{REF} is the reference voltage to be compared with the read voltage to decide ‘H’ or ‘L’ of the selected cell.

and that of columns are n and m, respectively. R_1 represents the first row driver in the array. C_1 represents the first column sense amplifier. $M_{1,1}$ is the cross-point memristor on the first row line and first column line. The array size is n×m. Each memristor in the array can be either Low resistance state (‘L’) or High resistance state (‘H’). R_W is interconnect resistance along the row and column lines.

In Fig. 1(a), we divided all the memristor cells into 4 groups in the nxm array. Here, G_1 represents the selected cell, $M_{1,M}$. Here, $M_{1,M}$ is decided to be selected because it is the farthest cell from both row drivers and column sense amplifiers. The farthest cell has the smallest read voltage margin among all the cells in nxm array. G_2 is the second group of memristors which are on the selected row in the nxm array. G_3 is the third group of memristors that are placed on the selected column that is sensed by the column sense amplifier C_M. G_4 is the fourth group, where the cells are on the columns and rows that are not selected, as shown in Fig. 1(a). Fig. 1(b) shows the worst-case (‘H’) and worst-case (‘L’) of read voltage margin. The worst-case (‘H’) is the worst-case of read voltage margin for reading ‘H’. When the selected cell is ‘H’, the read current flowing into the column sense amplifier becomes small thus the read voltage becomes low. The amount of (‘H’) read voltage, however, can be affected by the background data patterns of G_2, G_3, and G_4. The number of possible cases of background patterns of G_2, G_3, and G_4 is $2^3 = 8$, because G_2, G_3, and G_4 in Fig. 1(a) are either ‘L’ or ‘H’, respectively. Among 8 cases of background patterns, the worst-case (‘H’) happens when G_2 = ’L’, G_3 = ’L’, and G_4 = ’L’. In this worst-case, the (‘H’) read voltage can be the highest to get closer to the reference voltage, V_{REF}. As the highest (‘H’) read voltage gets closer to V_{REF}, it becomes difficult to distinguish between the (‘H’) read voltage and V_{REF}. In Fig. 1(b), ΔV is the read voltage margin that is defined by the voltage gap between the highest (‘H’) read voltage and V_{REF}.

Similarly, the worst-case (’L’) happens when reading ‘L’. When the selected cell has ‘L’, the read current flowing into the column sense amplifier becomes large thus the read voltage becomes high. Among 8 different background patterns, the worst-case (‘L’) happens when G_2 = ’L’, G_3 = ’L’, and G_4 = ’H’. In this worst-case, the (‘L’) read voltage can be the lowest to get closer to the reference voltage, V_{REF}. As the lowest (‘L’) read voltage gets closer to V_{REF}, it becomes more difficult to distinguish between the (‘L’) read voltage and V_{REF}. For the worst-case (‘L’), ΔV can be defined by the voltage gap between the lowest (‘L’) read voltage and V_{REF}.

In the static reference scheme as shown in Fig. 1(b), V_{REF} is fixed by a static and constant voltage regardless of different background patterns of G_2, G_3, and G_4. Thus, V_{REF} should be a middle point between the highest (‘H’) read voltage and the lowest (‘L’) read voltage, as shown in Fig. 1(b), to maximize the voltage margin, ΔV.

One more thing to degrade the read voltage margin is the position dependence in the array [15, 16]. Fig. 2 shows the read voltage of the selected cell with varying

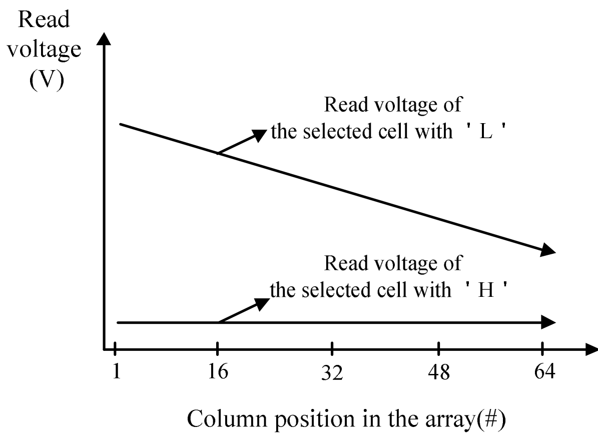


Fig. 2. The read voltage of the selected cell according to column position in the array. The upper line is for the read voltage of the selected cell with 'L' and the lower line is for the selected cell with 'H' as the column position is varied. Here, we assume 64x64 pure memristor array. The '1' in the x-axis is the first column from the row driver. The '64' means the farthest 64th column from the row driver.

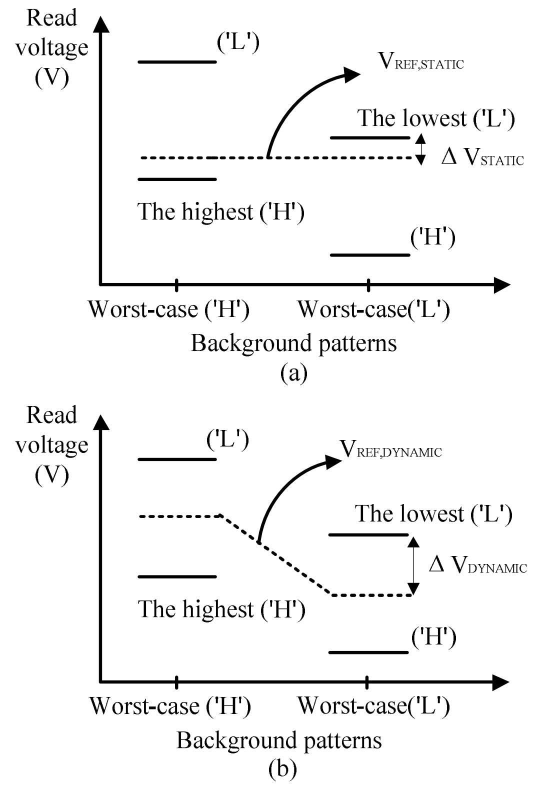


Fig. 3. The conceptual schematics of (a) The static reference scheme, (b) The dynamic one. The y-axis is the read voltage of the selected cell. The worst-case ('H') is the highest ('H') read voltage of the selected cell. The worst-case ('L') is the lowest ('L') read voltage of the selected cell. $V_{REF,STATIC}$ is the reference voltage of the static reference scheme. $V_{REF,DYNAMIC}$ is the reference voltage of the dynamic reference scheme. ΔV_{STATIC} is the read voltage margin of the static reference scheme and $\Delta V_{DYNAMIC}$ is the margin of the dynamic scheme.

the column position in the array, when G_2 = 'L', G_3 = 'L', and G_4 = 'H'. The upper line of the read voltage is for reading 'L' and the lower line is for sensing 'H'. From this figure, we can know that the read voltages of 'H' and 'L' have not only the data pattern dependence but also the position dependence.

In the following section II, a new dynamic reference scheme is proposed to improve the read voltage margin better than the static reference scheme in Fig. 1(b) [17]. The proposed dynamic reference scheme can be helpful in compensating not only the background pattern dependence but also the cell position dependence. In the section III, we show the simulation results, where the read voltage margin is compared between the previous static reference scheme and the new dynamic reference scheme. In the section IV, we summarize this paper.

II. WORST CASE SIMULATION SETUP AND THE NEW PROPOSED SCHEMATIC

To improve the read voltage margin better than the previous static reference scheme, we proposed a new dynamic reference scheme, where the reference voltage can be changed according to data patterns of the unselected cells and position of the selected cell in pure memristor array. Fig. 3(a) and (b) show the conceptual schematics of the previous static reference scheme and the new dynamic one, respectively. The y-axis represents the read voltage of the selected cell. The worst-case ('H') is the highest ('H') read voltage of the selected cell. The worst-case ('L') is the lowest ('L') read voltage of the selected cell. ΔV_{STATIC} is the read voltage margin of the static reference scheme and $\Delta V_{DYNAMIC}$ is the margin of the dynamic scheme. In the static reference scheme, the reference voltage is fixed by a constant voltage thereby the read voltage margin is very much narrowed, as shown in Fig. 3(a). On the contrary, in the dynamic reference scheme, the reference voltage can be adjusted according to the background data patterns and the cell position in the array. By doing so, the read voltage margin in the dynamic reference scheme can be improved better than the static reference scheme, as shown in Fig. 3(b).

In Fig. 4, we propose a new read circuit for implementing the dynamic reference voltage. In Fig. 4,

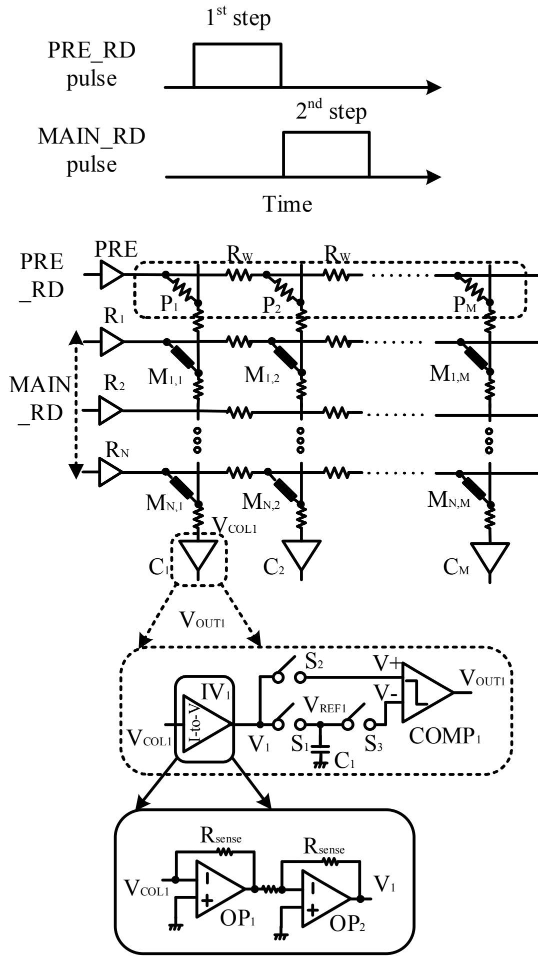


Fig. 4. The schematic of the read circuit with the proposed dynamic reference scheme. The read operation is composed of two steps, as shown here. The first step is driven by 'PRE_RD' pulse and the second step is activated by 'MAIN_RD' pulse.

the read operation is composed of two steps which are driven by the 'PRE_RD' and 'MAIN_RD' pulses, respectively. Here, the first step is driven by 'PRE_RD' pulse and the second step is activated by 'MAIN_RD' pulse. When 'PRE_RD' pulse is high, the reference voltage which can be different according to different background patterns and different position of the selected cell is adjusted to maximize the read voltage margin for the following 'MAIN_RD' step. When 'MAIN_RD' pulse is high, the selected cell is read and compared with the reference voltage that has been just adjusted in the 'PRE_RD' step in order to decide whether the stored cell is 0 or 1.

PRE in Fig. 4 is the 'PRE_RD' driver for sensing the dynamic reference voltage during the 'PRE_RD' step. The pure memristor array is composed of nxm memristors, which are represented by $M_{1,1}$, $M_{1,2}$, etc. Here, $M_{1,1}$ is on the crossing point between the first row and first column. $M_{1,2}$ is on the crossing point between the first row and second column. In Fig. 4, R_W means the interconnect resistance. R_1 is the row driver for reading the first row. C_1 is the column sense amplifier for the first column. P_1, P_2, etc. are representing the resistors for sensing the reference voltage that can be adjusted dynamically according to background data patterns of G_2, G_3, and G_4 and position of the selected cell in the memristor array. The column sense amplifier is shown in detail in the inset of Fig. 4. The first column line is connected to IV_1 that is the current-to-voltage converter. The output of IV_1 is connected to S_1 and S_2. During the 'PRE_RD' step, S_1 is on and S_2 is off, thus the sensed reference voltage is stored at C_1. For the next 'MAIN_RD' step, S_1 becomes off and S_2 and S_3 are on. At this time, the read voltage of selected cell is compared with the reference voltage that has been sensed during the 'PRE_RD' step. Because the reference voltage can be changed dynamically according to background patterns of G_2, G_3, and G_4 and position of the selected cell, the comparator can have more voltage margin in reading the selected cell. $COMP_1$ in Fig. 4 is the comparator. The detailed schematic of IV_1 is shown in the inset figure. R_{SENSE} is the sensing resistor and OP_1 and OP_2 are the operational amplifiers that constitute the current-to-voltage converter, IV_1. In Fig. 4, V_{COL1} is the first column-line voltage. V_1 is the output node voltage of IV_1. V_{REF1} is the adjusted reference voltage that is stored on C_1. V_{OUT1} is the output voltage of the comparator, $COMP_1$. V^+ is the (+) input voltage of $COMP_1$. V^- is the (-) input voltage of $COMP_1$.

Fig. 5 shows the voltage waveforms of the read circuit with the proposed dynamic reference scheme in Fig. 4. In the simulation, the array size is assumed 64 × 64. Here, V_{64} is the output node voltage of IV_{64}. V_{REF64} is the reference voltage of 64th column and V_{OUT64} is the output voltage of the 64th column. In Fig. 5, the 64th column means the farthest from the row drivers. In the read operation, 'PRE_RD' pulse should be activated for the 'PRE_RD' step. During this step, V_{64} is delivered to V_{REF64} and stored on C_{64}. When 'MAIN_RD' pulse is high, V_{64} and V_{REF64} are delivered to V^+ and V^- of the comparator, respectively. By comparing V^+ and V^-, the comparator decides its output voltage of V_{OUT64}. In this

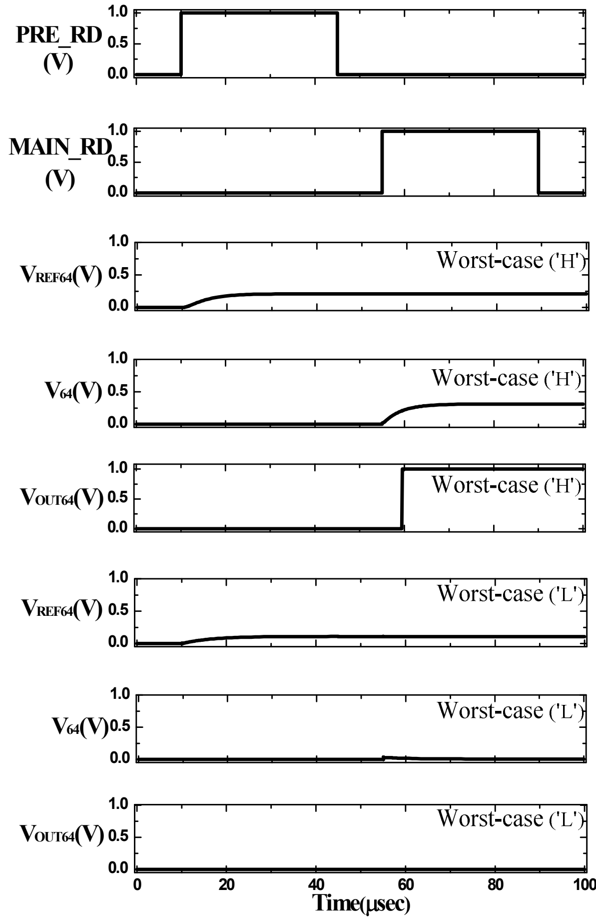


Fig. 5. The waveforms of the read circuit with the proposed dynamic reference scheme.

simulation, we showed two worst cases of V_{64}, V_{REF64}, and V_{OUT64}, as indicated by the worst-case ('H') and worst-case ('L'), in Fig. 5.

III. SIMULATION RESULT

In this paper, the simulation of CMOS-memristor hybrid circuits is performed by CADENCE SPECTRE [18]. Here, CMOS spice parameters were obtained from SAMSUNG 0.13-μm technology. In the simulation, we assumed that High resistance state (H) and Low resistance state (L) are as high as 1 MΩ and as low as 5 kΩ, respectively. The sensing resistance value used in this paper is 12.2 kΩ. And the interconnect resistance (R_W) is varied from 0 Ω to 4.25 Ω. This range of interconnect resistance is obtained from International Technology Roadmap for Semiconductors (ITRS) [19]. The sensing resistance (R_{SENSE}) is 5 kΩ. The supply voltage (V_{DD}) is 1 V.

For the memristor Verilog-A model, we reflected the recent experimental measure data of memristor devices. To do so, we considered the non-linear dopant kinetics which are dominant at the boundaries of resistive switching in the Verilog-A model [20, 21]. Before we developed the memristor Verilog-A model, we should consider memristive behavior first. The following equation can explain the memristor's current-voltage relationship [1]. Here, v(t) and i(t) represent memristor's voltage and current flow through memristor, respectively. $R_X(t)$ is the value of memristance calculated by Eq. (1). R_{SET} and R_{RESET} are low resistance value and high resistance value, respectively. w(t) is the effective width of memristor and D is the maximum drift distance of w(t). q(t) and Q_{CRIT} mean the accumulated charge flow through the memristor and critical charge for the transition from RESET-to-SET. Here, μ_v is the mobility of dopant in the equation [1].

$$
\begin{aligned}
v(t) &= Rx(t)\cdot i(t) \\
&= \left(R_{SET}\frac{w(t)}{D} + R_{RESET}\left(1-\frac{w(t)}{D}\right)\right) i(t) \\
&= \left(R_{SET}\frac{q(t)}{Q_{CRIT}} + R_{RESET}\left(1-\frac{q(t)}{Q_{CRIT}}\right)\right) i(t)
\end{aligned}
$$

where

$$
\frac{w(t)}{D} = \mu_v \frac{R_{SET}}{D^2} q(t) = \frac{q(t)}{Q_{CRIT}}, \text{and } Q_{CRIT} = \frac{D^2}{\mu_v R_{SET}} \tag{1}
$$

The threshold behaviors and window function are also included in the circuit simulation for verifying the proposed dynamic reference scheme [20, 21].

Fig. 6 shows the simulation results of the memristor Verilog-A model which is used in this paper. Fig. 6(a) shows the input sinusoidal voltage waveform, and Fig. 6(b) shows the current flow through the memristor model that reflects the threshold behavior. In the Fig. 6(c), the resistance is changed from high resistance state to low resistance state when the polarity of the input voltage is positive. When the input voltage is negative, the resistance value is reached from low resistance state to high resistance state.

In Fig. 7(a) and (b), we compared the read voltage

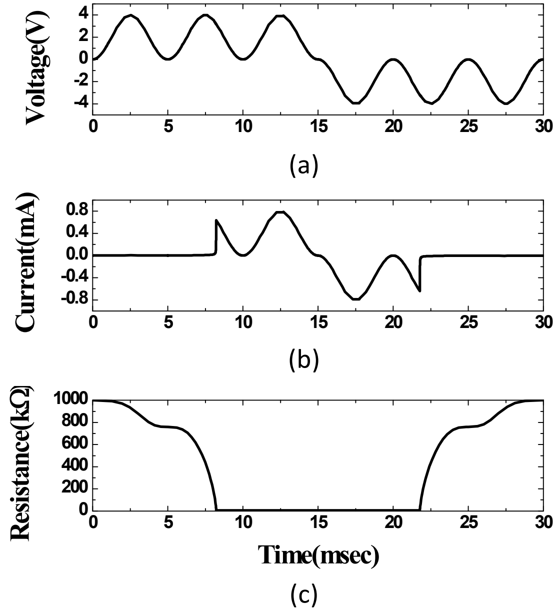


Fig. 6. Simulation result of the memristor Verilog-A model (a) Input sinusoidal voltage, (b) The current flow through memristor model, (c) the change of resistance value.

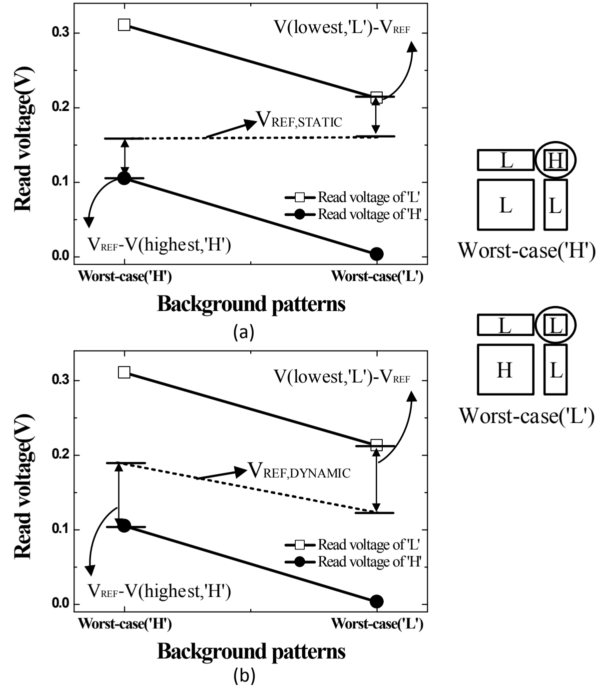


Fig. 7. (a) The read voltages with the different background patterns of worst-case (‘H’) and worst-case (‘L’) for the static reference scheme, (b) The read voltages with the different background patterns of worst-case (‘H’) and worst-case (‘L’) for the dynamic reference scheme.

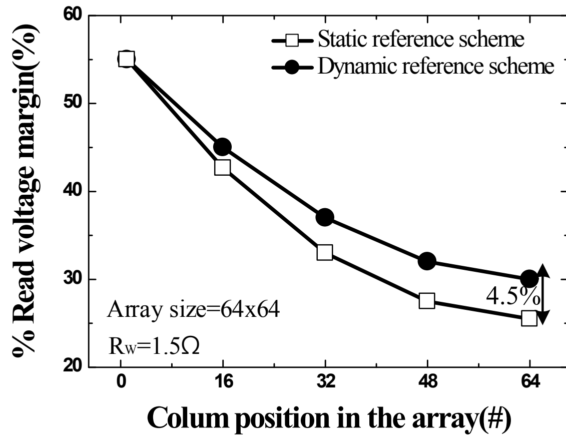
margin between the previous static reference scheme and the proposed dynamic reference scheme. Here, the read voltage margin, ΔV is defined by

$$\Delta V = \min\begin{pmatrix} V(lowest,'L') - V_{REF} \\ V_{REF} - V(highest,'H') \end{pmatrix} \quad (2)$$

In this paper, V(lowest, ‘L’) means the lowest read voltage of the selected cell with ‘L’ among 8 different cases of neighboring groups. V(highest, ‘H’) means the highest read voltage for reading ‘H’ among 8 different cases. V_{REF} is the reference voltage. The read voltage margin, ΔV can be decided by the minimum value between V(lowest, ‘L’) - V_{REF} and V_{REF}-V(highest, ‘H’). In Fig. 7(a) and (b), ΔV_{STATIC} and $\Delta V_{DYNAMIC}$ represent the read voltage margins of the static and dynamic reference schemes. Here, the worst-case (‘H’) is for the highest (‘H’) read voltage and the worst-case (‘L’) is for the lowest (‘L’) read voltage, among 8 different background patterns. Comparing ΔV_{STATIC} and $\Delta V_{DYNAMIC}$ shows that the dynamic reference scheme can improve the read voltage margin by as much as 58.28% than the static scheme, by compensating the dependence of read voltage on background patterns. More specifically, for calculating ΔV_{STATIC} in Fig. 7(a), V_{REF}-V(highest, ‘H’) and V(lowest, ‘L’) - V_{REF} are obtained, respectively. Between V_{REF}-V(highest, ‘H’) and V(lowest, ‘L’)-V_{REF}, according to Eq. (2), the lower value can be regarded ΔV_{STATIC} in Fig. 7(a), which is as low as 51.3 mV. Similarly, for calculating $\Delta V_{DYNAMIC}$, V_{REF}-V(highest, ‘H’) and V(lowest, ‘L’)-V_{REF} are obtained, respectively, in Fig. 7(b). V_{REF}-V(highest, ‘H’) and V(lowest, ‘L’)-V_{REF} in Fig. 7(b) are 81.2 mV and 82 mV, respectively. Between V_{REF}-V(highest, ‘H’) and V(lowest, ‘L’)-V_{REF}, according to Eq. (2), the lower value can be regarded $\Delta V_{DYNAMIC}$, which is 81.2 mV. This value is higher than ΔV_{STATIC} by 58.28%.

Fig. 8(a) and (b) show the percentage read voltage margin with varying the column position of the selected cell in the array. The percentage read voltage margin is defined by $\Delta V / VDD \times 100\%$.

In the Fig. 8(a) and (b), the percentage margin of the read voltage is large when the sense amplifier is close to the row drivers. As the column position becomes farther from the row drivers, the percentage read voltage margin becomes worse. Fig. 8(a) shows the comparison between the dynamic reference scheme and the static one in terms



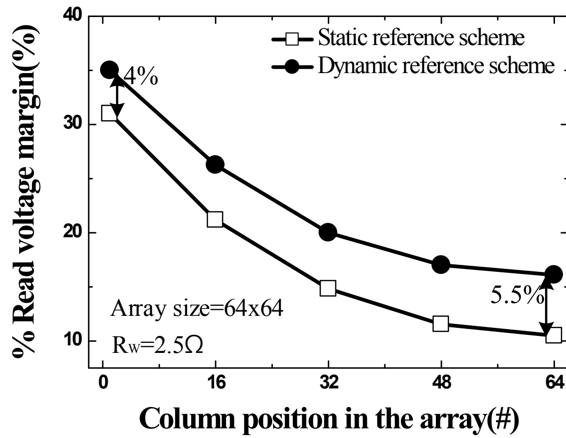
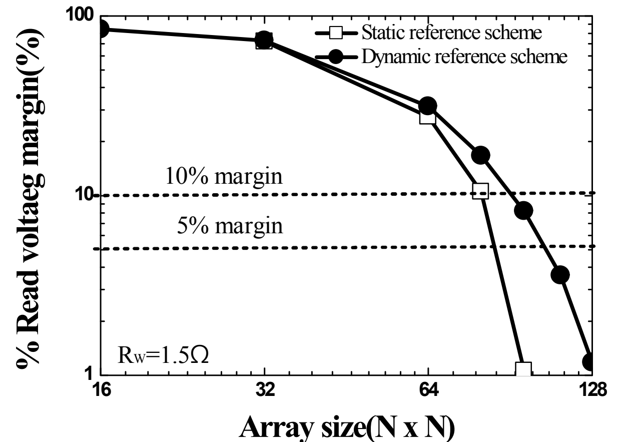


Fig. 8. The percentage read voltage margin with varying the column position of the selected cell in the array for the static and dynamic reference scheme for (a) R_W = 1.5 Ω, (b) R_W = 2.5 Ω.



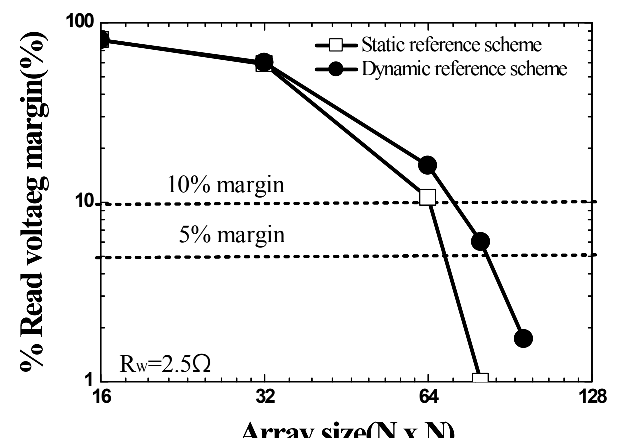


Fig. 9. The percentage read voltage margin with varying the size of array in the simulated array from 16x16 to 128x128 for (a) R_W = 1.5 Ω, (b) R_W = 2.5 Ω.

of the percentage read voltage margin when the value of interconnect resistance 'R_W' is 1.5 Ω. The dynamic reference scheme is improved by 3% than the static scheme on average. When the value of the interconnect resistance is 2.5 Ω, the percentage read voltage margin of dynamic reference scheme is improved by 5% on average, as shown in Fig. 8. This results mean that if the value of interconnect resistance is increased, the proposed dynamic reference scheme can improve the read margin more and more.

Fig. 9(a) compares the percentage read voltage margin between the previous static scheme and the new dynamic one with varying the array size with R_W = 1.5 Ω. Here, the critical percentage margin for reading the selected cell is assumed 10% [9] and 5%, respectively. The critical margin means that we cannot distinguish 'L' and 'H', if the percentage read margin is smaller than the critical margin. For R_W = 1.5 Ω, the proposed dynamic scheme can increase the array size by 38.5% than the static scheme, assuming the critical margin of 10%. If we lower the critical margin to 5%, the array size can be increased by as much as 60% in the proposed scheme. Fig. 9(b) compares the margin between the previous scheme and proposed one for R_W = 2.5 Ω. In this case, the proposed scheme can increase the array size by 37.5% and 55% for the critical margin of 10% and 5%, respectively, compared to the previous scheme.

Fig. 10(a) shows the percentage read margin with varying the interconnect resistance from 1.5 Ω to 4.25 Ω, for the array size of 64 x 64. Here, the interconnect resistance can be increased to as large as 3.25 Ω in the proposed dynamic scheme, for the successful read operation with 10% critical margin. On the contrary, the interconnect resistance should be smaller than 2.5 Ω in

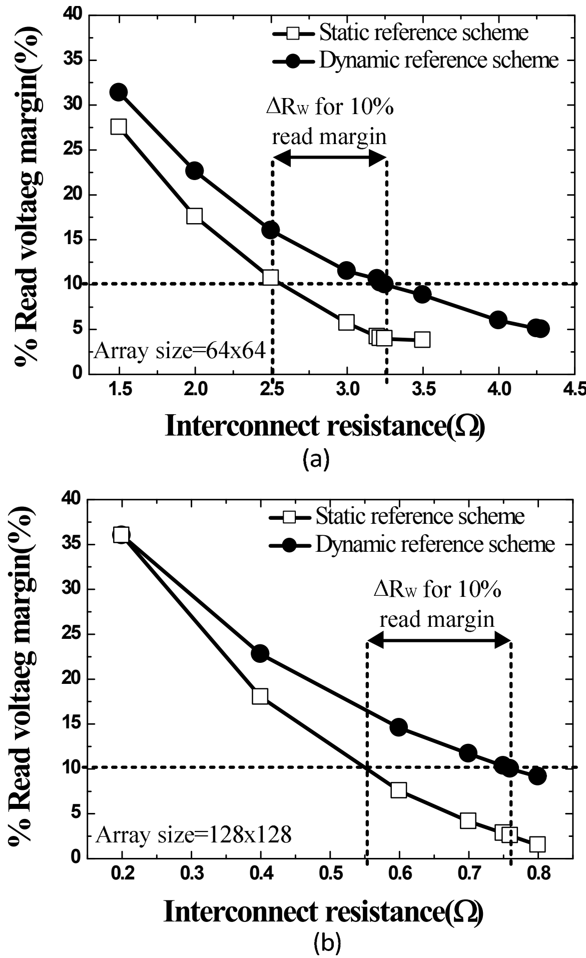


Fig. 10. (a) The percentage read voltage margin with varying the interconnect resistance from 1.5 Ω to 4.25 Ω with 64x64 array size, (b) The interconnect resistance from 0.2 Ω to 0.8 Ω with 128 x 128 array size.

the previous static scheme. Thus, we can know that the interconnect resistance of the dynamic scheme can be larger by 30% than the static reference scheme, allowing more margin on the variation of interconnect resistance. In Fig. 10(b), the 128 x 128 array is simulated with varying the interconnect resistance from 0.2 Ω to 0.8 Ω. For the successful read operation with 10% critical margin, the interconnect resistance can be increased to 0.76 Ω in the proposed scheme. In the previous static scheme, the interconnect resistance should be smaller than 0.55 Ω. Therefore, the interconnect resistance of the proposed dynamic scheme can be larger by 38% than the static reference scheme, allowing more margin on the variation of interconnect resistance. This comparison in Fig. 10(a) and (b) indicate that the proposed dynamic reference scheme can be more reliable in performing read operation with the variation of interconnect resistance. And also, the proposed scheme can be more suitable in the scaled dimensions of interconnect lines in future process technology.

IV. CONCLUSIONS

In this paper, the dynamic reference scheme was proposed to improve the read voltage margin better than the previous static reference scheme. The proposed dynamic reference scheme can be helpful in compensating not only the background pattern dependence but also the cell position dependence. The proposed dynamic reference circuit was verified by simulating the CMOS-memristor hybrid circuit with the practical CMOS SPICE and memristor Verilog-A models. In the simulation, the percentage read voltage margin was compared between the previous static reference scheme and the new dynamic reference scheme. As a result, the dynamic scheme could improve the read voltage margin by 58.28% than the previous static scheme. Assuming that the critical percentage of read voltage margin is 5% and R_W = 1.5 Ω, the memristor array size with the dynamic scheme can be increased by 60%, compared to the array with the static one. For the array size of 64 x 64, the margin of the interconnect resistance of the dynamic scheme can be larger by 30% than the static reference scheme. For the array size of 128 x 128, the margin of the interconnect resistance of the proposed scheme can be improved by 38% than the previous static reference scheme, allowing more margin on the variation of interconnect resistance.

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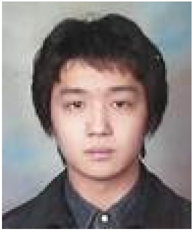

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