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The Oscillation Frequency of CML-based Multipath Ring Oscillators

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***Abstract*—A novel phase interpolator (PI) based linear model of multipath ring oscillator (MPRO) is described in this paper. By modeling each delay cell as an ideal summer followed by a single pole RC filter, the oscillation frequency is derived for a 4-stage differential MPRO. It is analytically proved that the oscillation frequency increases with the growth of the forwarding factor α, which is also confirmed quantitatively through simulation. Based on the proposed model, it is shown that the power to frequency ratio keeps constant as the speed increases. Running at the same speed, a 4-stage MPRO can outperform the corresponding single-stage ring oscillator (SPRO) with 27% power saving, making MPRO with a large forwarding factor α an attractive option for lower power applications.**

***Index Terms*—Oscillator, multipath ring oscillator, oscillation frequency, oscillation criterion, oscillation mode, mode gain, forwarding factor**

I. INTRODUCTION

Ring oscillator has been widely adopted in a broad range of electrical applications [1-3] for its design simplicity, wide tuning range, low power and ease of integration. At the cost of a DC current, the CML-based differential ring oscillator, which is shown in Fig. 1(a), is especially popular as it provides truly differential output phases rather than pseudo differential output phases from the inverter-based ring oscillator. The CML-based ring oscillator supports even number of output phases, which facilitates the design of follow-on phase interpolator, while the conventional single-ended inverter-based ring oscillator is limited to odd number of phases. Furthermore, the oscillating frequency of a CML-based ring oscillator is determined by the output resistance and capacitance, which can be programmed regardless of process speed. Therefore, it can run at higher speed than the corresponding inverter-based ring oscillator, whose maximum achievable frequency is highly correlated with the process technology. For example, as high definition (HD), ultra-high definition (UHD) and 8K (Quard-UHD) TVs are being adopted in the television market, the throughput of the intra-panel interface from the timing controller (TCON) to the source-driver IC (SIC) can exceed 10 Gbps, while the SIC circuit process technology is typically limited to 180 nm CMOS because of high voltages needed for pixel driving [4-7]. To enable the next generation display interface, CML-based ring oscillators running at higher frequency with conventional process technologies are highly desired.

However, calculating the oscillation frequency of the multipath ring oscillator, such as the 4-stage MPRO with a forwarding factor α shown in Fig. 1(b), is not trivial. The oscillation frequency issue for inverter-based MPRO has been studied in depth with detailed analytical expressions and numerous simulations [12, 13]. A simpler systematic modeling of CML-based MPRO is desired to study its oscillation frequency property and to provide general design guidance. Focusing on the CML-based MPRO, in this paper, we simplified each buffer

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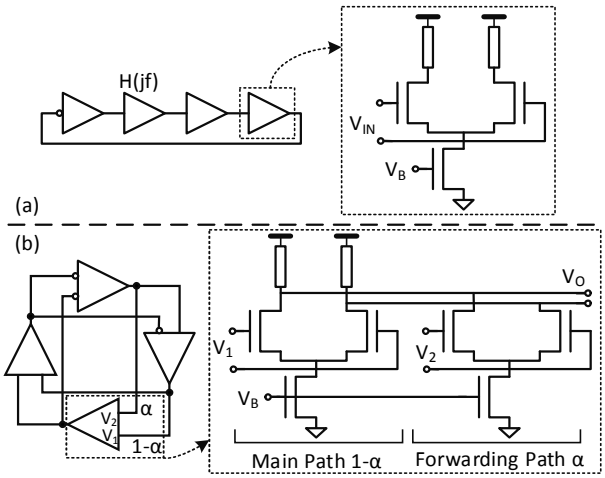

Fig. 1. (a) A 4-stage differential single path ring oscillator with H(jf) as each buffer's frequency transfer function, (b) A 4-stage differential multipath ring oscillator with H(jf) as the frequency transfer function of each buffer stage (assuming both inputs identical). The forwarding path is with weight α and the main path is with weight 1-α.

stage as an ideal weighted summer followed by a single pole low pass filter and derived the MPRO oscillation frequency analytically. The analytical results matched simulation results well and demonstrated that multipathing can effectively improve power efficiency, making it desirable for lower power applications, such as consumer electronic devices.

This paper is organized as following, section II addresses a simple phase interpolator-based linear model for the delay stage, which includes an ideal weighted summer and one pole low pass filter, and derives the oscillation criterion for the 4-stage MPRO. The detailed analysis on the modeling results is addressed in section III, The power to the oscillation frequency ratio is studied, which demonstrates the power saving merit besides speed advantage provided by multipathing. The conclusions are drawn in section IV.

II. The Oscillation Criterion and Frequency of a 4-Stage CML-Based MPRO

1. Oscillation Criterion of SPRO

For a fair comparison, the oscillation criterion for the single path ring oscillator (SPRO) is addressed first to set the benchmark. For a 4-stage differential SPRO shown in

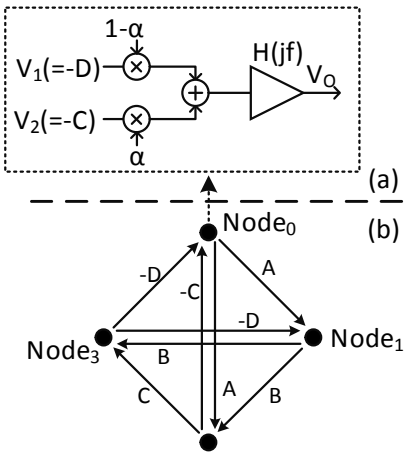

Fig. 2. (a) Linear model of the delay stage $Node_0$ for MPRO,. (b) Closed loop modeling of a 4-stage MPRO.

Fig. 1(a) with the frequency transfer function of each stage assumed to be H(jf), at the oscillating frequency f_s, the open loop gain must be one and the closed loop phase shift must be 2π:

$$-1\times H^4\left(jf_s\right)=1, \tag{1}$$

where the factor -1 is due to the phase inverting between the output of the last stage and input of the first stage.

Thus, once the frequency transfer function H(jf) is determined, the oscillation frequency can be derived accordingly. In other words, to meet the oscillating frequency target f_s, the frequency transfer function H(jf) must be designed with the right selection of output resistance, capacitance and tail current to satisfy Eq. (1). Assuming that each buffer is a single pole system, the pole f_0 should be equal to the oscillation frequency:

$$f_0 = f_s, \tag{2}$$

and the DC gain should be $\sqrt{2}$. Thus, at the oscillation frequency, each stage provides a phase shift of π/4 and the accumulated phase shift around the loop is 2π. Furthermore, the loop gain at oscillation frequency is 1. Therefore, the oscillation criterion Eq. (1) is met and it oscillates at the frequency matching the buffer's output pole.

2. Oscillation Criterion of MPRO

For the sake of simplicity, a 2-path MPRO is studied here and the related methodology can be applied to other multi-path ring oscillators. As shown in Fig. 2(a), for

each of the buffer stage, there are two inputs and one output. Equivalent to a phase interpolator, it can be modeled as an ideal analog summer with weights α and 1-α respectively, where α is the forwarding factor, and followed by a filter H(jf). The output filter is assumed to be a single pole low pass filter with 3 dB bandwidth f_0:

$$H(jf) = \frac{A_{DC}}{1 + jf / f_0} \tag{3}$$

3. Oscillation Criterion of 4-stage CML-based MPRO

With the linear model of delay stage, the closed loop system of a 4-stage MPRO is shown in Fig. 2(b). In frequency domain, the outputs of $Node_0$ to $Node_4$ are A, B, C and D respectively, where the input of $Node_0$ is -D and -C and input of $Node_1$ is A and -D because of phase inversion. In the steady state, the system must satisfy the following relation:

$$\begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix} = M \times \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix}, \tag{4}$$

where M represents matrix:

$$\begin{bmatrix} 0 & 0 & -\alpha H & -(1-\alpha)H \\ (1-\alpha)H & 0 & 0 & -\alpha H \\ \alpha H & (1-\alpha)H & 0 & 0 \\ 0 & \alpha H & (1-\alpha)H & 0 \end{bmatrix} \tag{5}$$

To make sure that there is a non-singular solution for Eq. (4), the following equation must be satisfied:

$$|M - I| = 0, \tag{6}$$

where I is a 4x4 unit matrix. Thus,

$$\left| \begin{bmatrix} -1 & 0 & -\alpha H & -(1-\alpha)H \\ (1-\alpha)H & -1 & 0 & -\alpha H \\ \alpha H & (1-\alpha)H & -1 & 0 \\ 0 & \alpha H & (1-\alpha)H & -1 \end{bmatrix} \right| = 0 \tag{7}$$

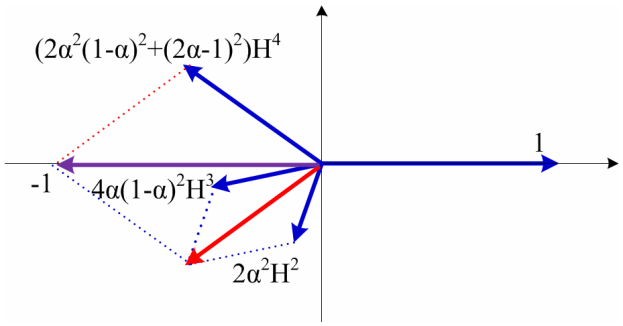

Fig. 3. An illustration of Eq. (8) in vector at oscillation frequency f_s. At oscillate frequency, the sum of vectors $2\alpha^2 H^2$, $4\alpha(1-\alpha)^2 H^3$ and $\left(2\alpha^2(\alpha-1)^2 + (2\alpha-1)^2\right)H^4$ must be -1.

Therefore,

$$\left(2\alpha^2(\alpha-1)^2 + (2\alpha-1)^2\right)H^4 + 4\alpha(1-\alpha)^2 H^3 + 2\alpha^2 H^2 + 1 = 0, \tag{8}$$

which provides the information on the oscillation of MPRO. For each α, the corresponding solution to Eq. (8) yields the required filter gain and phase shift per stage for oscillation. From a design point of view, for an arbitrary H(jf) defined by Eq. (3), the frequency f_s at which H(jf) meets the phase requirement is the potential oscillation frequency. Furthermore, to oscillate at f_s, the DC gain A_{DC} must be adjusted accordingly so that the filter gain requirement is satisfied as well. Thus, the oscillation frequency and the corresponding minimal DC gain for a MPRO with forwarding factor α can be derived accordingly.

III. Analysis and Simulation on MPRO

1. Oscillation Frequency of MPRO

As a simple data point of Eq. (8), when the forwarding factor α equals zero, meaning that there is no path between $Node_0$ and $Node_2$ (or between $Node_1$ and $Node_3$), Eq. (8) degrades to:

$$H^4(jf) + 1 = 0, \tag{9}$$

which is consistent with the oscillation criterion of a 4-stage single path ring oscillator presented by Eq. (1): it oscillates at frequency f_0, where f_0 is the 3 dB bandwidth

of the buffer H(jf) with a required DC gain of $\sqrt{2}$. On the other hand, when α = 1, meaning that there is no path from $Node_0$ to $Node_1$ (or $Node_1$ to $Node_2$, or $Node_2$ to $Node_3$ or $Node_3$ to $Node_0$), Eq. (8) degrades to:

$$H^2(jf)+1=0 \tag{10}$$

Since each single pole buffer H(jf) can only provide a phase shift up to π/2, there is no valid solution to Eq. (10). Therefore, the circuit will not oscillate with α = 1. For α between 0 and 1, all three factors in Eq. (8) are no less than 0:

$$\begin{aligned} 2\alpha^2(\alpha-1)^2+(2\alpha-1)^2 &\geq 0 \\ 4\alpha(1-\alpha)^2 &\geq 0 \\ 2\alpha^2 &\geq 0 \end{aligned}$$

According to the vector relation, which is shown in Fig. 3, at the oscillating frequency f_s:

$$\begin{aligned} \angle H^4(jf_s) &\leq -\pi \\ \angle H^2(jf_s) &\geq -\pi \end{aligned}$$

Thus, f_s is greater or equal to f_0, proving that MPRO oscillates at higher rate than the corresponding 4-stage SPRO.

To investigate the property of this 4-stage CML-based MPRO, the forwarding factor α is swept and the solution to Eq. (8) is solved numerically. The derived oscillation frequency is normalized to f_0, the 3 dB bandwidth of filter H(jf), and shown in Fig. 4(a) with the required minimum DC gain presented in Fig. 4(b). When α is 0, the normalized oscillation frequency is 1 with the minimal gain requirement of $\sqrt{2}$, reflecting the case of a 4-stage SPRO. As α increases, the oscillating frequency increases with the minimal gain requirement increases as well. As shown in Fig. 4, when α equals 0.341, the MPRO oscillates a normalized frequency of $\sqrt{3}$ with a DC gain requirement 2.145. On the other hand, the corresponding 3-stage SPRO oscillates at a normalized frequency of $\sqrt{3}$ when the DC gain is at 2. Therefore, a 4-stage MPRO can run as fast as a 3-stage SPRO with 7.25% more DC gain requirement. For comparison, a MPRO design same as Fig. 1 is simulated with respect to the forwarding factor α. The required minimum DC gain and the oscillation frequency are simulated with both 65 nm and 180 nm processes. As illustrated in Fig. 4(a) and (b), the simulation results are well aligned with the analytical prediction.

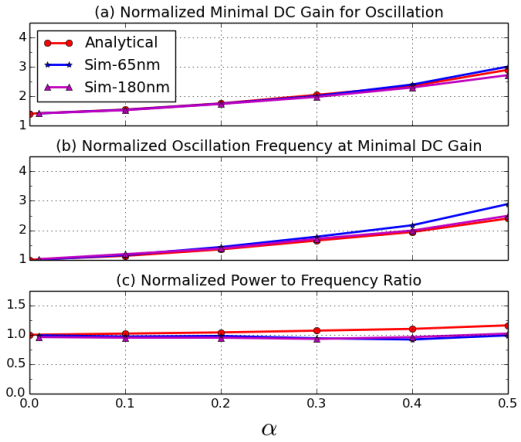

Fig. 4. (a) The required DC gain at different forwarding factor α according to analysis and simulation of MPROs implemented in 65 and 180 nm processes, (b) The corresponding normalized oscillation frequency at different α, (c) The ratio between the required power and normalized oscillation frequency at different α with γ to be 1.4.

2. Energy Efficiency of MPRO

With the filter's 3dB bandwidth f_0 normalized to be 1, the required gain bandwidth product for each of the MPRO stage is:

$$A_{DC}\times f_0 = g_m R_L \times \frac{1}{2\pi R_L C_L} = \frac{g_m}{2\pi C_L} \propto \sqrt[\gamma]{I}, \tag{11}$$

which is a monotonically increasing function of the current I, and hence also of the circuit power consumption. Here g_m is the transconductance of the CML pair device, R_L is the resistance of output node, C_L is the capacitance of output node and I is the DC current of CML tail device. As a function of the process technology, the coefficient γ maps the transconductace with the tail current and is close to 2 if the device current strictly follows the square law. As shown in Fig. 5, for the 65 nm process used in the simulation, γ is approximately 1.4 around the current range of interest. With the help of γ, the oscillation power can be derived through the required transconductance. Hence, the

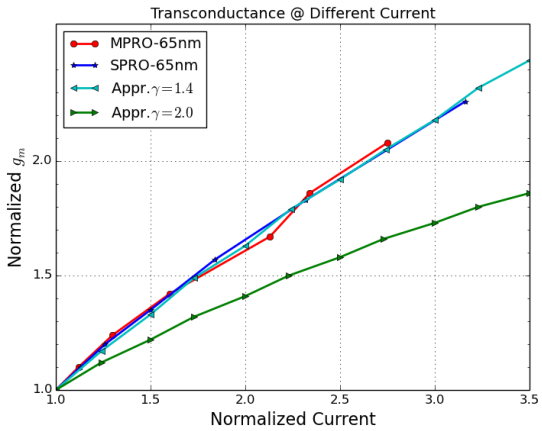

Fig. 5. The normalized transconductance g_m of the device at different normalized current I_{DS}. Based on the simulation results, γ is close to 1.4 for the adopted 65 nm process.

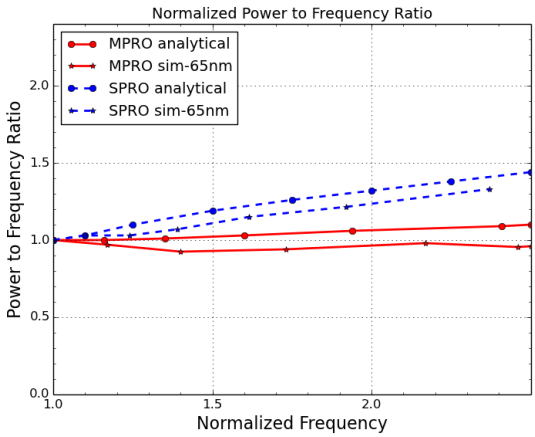

Fig. 6. The power to frequency ratio for MPRO and SPRO vs. frequency based on analysis and simulation.

comparison of power efficiency between MPRO and SPRO becomes possible.

As the oscillating frequency increases with larger forwarding factor α, the required DC gain increases as well. Given that the filter's 3dB bandwidth is fixed and normalized to be 1, the gain bandwidth product grows during this process and more power is required to oscillate. The ratio between the required power and the oscillation frequency at each α is explored and plot in Fig. 4(c). Multipathing increases the oscillation frequency effectively with the power to frequency ratio relatively flat across a wide range of α, consuming constant energy per toggling as the oscillation frequency increases. For example, as α increases from 0 to 0.4, the oscillation frequency grows by 94% according to the numerical solution to Eq. (8), meanwhile, power to frequency ratio grows by 5% based on analysis, -2% and -5% according to simulation at 65 nm process and 180 nm process respectively. The analysis matches the simulation result, showing that the MPRO increases the oscillation speed with a relatively constant energy per toggling efficiency.

Note that as α increases, both the required DC gain for oscillation and the corresponding oscillation frequency go up exponentially. For the circuit simulation, to achieve higher DC gain without changing the output pole, the output resistance and input device pair must be constant, while the tail current must increase. When α is sufficiently large, the tail device falls into linear region, exacerbates the common mode rejection ratio and introduces common mode oscillation [13], which is not the desired oscillation mode. Therefore, α is limited to be less than 0.5 in these experiments.

3. Comparison with SPRO on Power Efficiency

The discussion above shows that multipathing improves the oscillation frequency at a relatively constant energy per toggle efficiency. For conventional 4-stage CML-based SPRO designs, to improve the speed from f_0 to βf_0, the output pole has to be shifted from f_0 to βf_0 with the DC gain kept at $\sqrt{2}$. Thus, the gain bandwidth product grows from $\sqrt{2}\ f_0$ to $\beta\sqrt{2}\ f_0$ by a factor of β and the corresponding power goes up by a factor β^{γ} according to Eq. (13). As the oscillation frequency grows by β in this procedure, the power to oscillation frequency ratio increases by a factor $\beta^{\gamma-1}$. In summary, for SPRO designs, the normalized power to speed ratio increases exponentially with the frequency increase.

The analytical power to speed ratio for SPRO and MPRO are both shown in Fig. 6. As the frequency increases, the power to frequency ratio increases for SPRO while keeps flat for MPRO. For example, as the speed grows from 1x to 2x, the MPRO requires 5% increase on the energy per toggle. For comparison, a SPRO is also built with a 65 nm CMOS process. The output resistance is swept to change the output pole location. For each output resistance, the minimal tail current for oscillation is found and corresponding normalized energy per toggle is plot in Fig. 6 as well. As the frequency grows, the SPRO requires more and more power for each toggling. MPRO shows 27% power

saving than SPRO at maximum frequency.

III. CONCLUSIONS

A phase interpolator-based analytical approach is introduced to analyze the oscillation frequency of CML-based MPRO. Through modeling the delay stage as an ideal summer followed by a first order low pass filter, this method demonstrates that the oscillating frequency of MPRO is a monotonically increasing function of the multipathing factor α analytically and reveals that the power to speed ratio is constant for MPRO across a wide range of speed. Based on analysis and simulation, multipathing can save 27% power than the corresponding SPRO running at the same rate, making it attractive for lower power applications.

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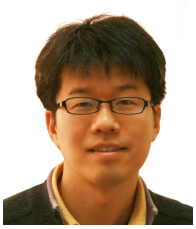

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