Integrate-and-Fire Neuron Circuit and Synaptic Device using Floating Body MOSFET with Spike Timing-Dependent Plasticity

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Abstract—**In the previous work, we have proposed an integrate-and-fire neuron circuit and synaptic device based on the floating body MOSFET [1-3]. Integrate-and-Fire(I&F) neuron circuit emulates the biological neuron characteristics such as integration, threshold triggering, output generation, refractory period using floating body MOSFET. The synaptic device has short-term and long-term memory in a single silicon device. In this paper, we connect the neuron circuit and the synaptic device using current mirror circuit for summation of post synaptic pulses. We emulate spike-timing-dependent-plasticity (STDP) characteristics of the synapse using feedback voltage without controller or clock. Using memory device in the logic circuit, we can emulate biological synapse and neuron with a small number of devices.**

Index Terms—**Integrate-and-fire neuron circuit, synaptic transistor, spike-timing-dependent-plasticity, long and short-term memory, floating body MOSFET**

I. INTRODUCTION

Until recently, the interest in biological system has increased and many researchers have attempted to emulate neural networks characterized by parallel processing and low power consumption. Various types of synaptic devices based on resistive switching memory, and neuron circuits using a capacitor have been proposed [4-7]. Integrate-and-fire (I&F) neuron circuit was introduced to emulate biological neuron characteristics, and "Axon-Hillock" model proposed by Mead [8] is the most representative model of the I&F neuron circuit. This model using two capacitors and six transistors is very simple and compact for integrating and firing. Most of I&F neuron circuits are constructed with a capacitor for the integration. Using a capacitor increases power consumption and delay time as well as size of the neuron circuits. These will be a critical problem if a number of neuron circuits are integrated on a chip.

In terms of synaptic device, most of researches about the synaptic device focus on memristor based resistive switching memory [9]. The memristor is a two-terminal device whose conductance can be modulated by charge through it. As we connect neuron and synapse, the two-terminal memristor device will require additional controller or clock for the implementation of spike-timing-dependent-plasticity (STDP) characteristics [10, 11]. If the system uses controller or clock, the system will be synchronized by the clock. But the biological system is asynchronous and the connection weight of biological synapse is adjusted automatically by the input signals and feedback signal of the neuron. In this work, we connected the neuron circuit and synaptic device using current mirror circuit and emulated the STDP characteristics. STDP is performed automatically by input signal and feedback signal of the neuron circuit. I&F neuron circuit is constructed with a floating body MOSFET whose operation is similar to the 1-transistor
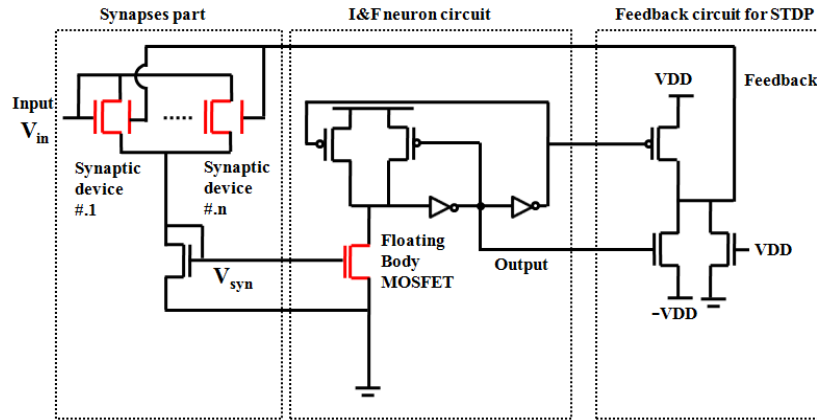
Fig. 1. Circuit description of synapse part and I&F neuron circuit and feedback circuit.

DRAM. The capacitor-less 1T-DRAM does not need a storage capacitor, since it uses floating body to store. The synaptic device consists of floating body and additional floating gate and back gate, and it has the transition from short-term to long-term memory in a single silicon device. The simulation was performed by SILVACO ATLAS mixed mode.

II. I&F NEURON CIRCUIT AND SYNPATIC DEVICE

Fig. 1 shows the synapse and neuron circuit diagram. This circuit is made up three part, synaptic devices, neuron, feedback and output generation. For the neuron circuit, 3 p-type MOSFETs, 4 n-type MOSFETs and 2 inverters are used. And one synaptic device is used per a synapse without additional transistor. So we can minimize the number of transistor to emulate the biological neuron and synapse.

1. Integrate-and-Fire Neuron Circuit with Floating Body MOSFET

The essential characteristics of the biological neuron are spatial and temporal integration, threshold triggering, output generation and refractory period. To emulate these properties, we used the floating body MOSFET whose operation is similar to the 1-transistor DRAM.

The first property is temporal integration. It is performed by the hole integration in the floating body MOSFET of the neuron circuit in Fig. 2. Fig. 3 shows the simulation result of the hole concentration in the floating
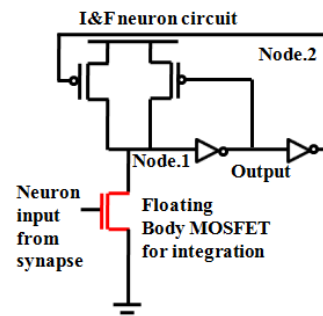

Fig. 2. Circuit diagram of integrated and fire neuron circuit.
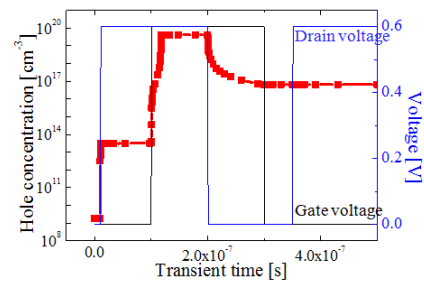

Fig. 3. Simulated hole concentration in the floating body. When the gate and drain voltages are high, holes are accumulated.

body and Fig. 4 shows drain current. As input pulses are applied to the gate of the floating body MOSFET, the holes made by impact ionization at the drain side are accumulated in the floating body and the drain current is increased rapidly by the holes. As the drain voltage is 0 V, the holes in the floating body are erased and return to the initial state. When the pulse trains from one synaptic device are applied to the gate of the floating body MOSFET, the holes are made by impact ionization at every pulse, and these holes are integrated in the floating
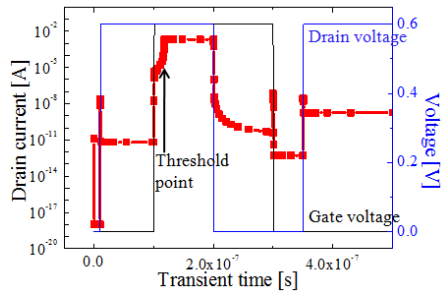
Fig. 4. Simulated drain current of the floating body MOSFET. Drain current increases very rapidly because of the accumulated holes.
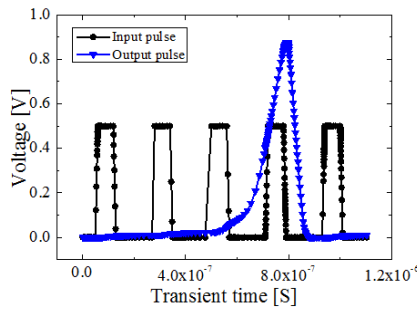

Fig. 5. Repeated low-voltage input pulse simulation result. The holes are accumulated during the first three input pulses, and then the neuron circuit is fired.

body. After several input signals are applied, enough holes are integrated to generate output voltage. It is temporal integration property as shown in Fig. 5. The holes are accumulated in the floating body during the first three input pulses, and then the neuron circuit generates the output voltage.

The second property is threshold triggering. The biological neuron has "all-or-none" characteristics. If the accumulated signal is over the threshold potential, the neuron will generate output signal to the other synapses. This property is performed by hole concentration in the floating body. As shown in Fig. 3, the holes are increasing exponentially at first. Because the holes make floating body potential lower, the current increases. And it makes more holes by impact ionization. Because of this positive feedback, the number of holes is increasing very fast at the threshold point and the hole concentration saturates later. The difference of the number of holes and drain current between saturation and non-saturation state is about three orders of magnitude as shown in Fig. 4. Therefore, the circuit determines fire-or-not according to the hole concentration.
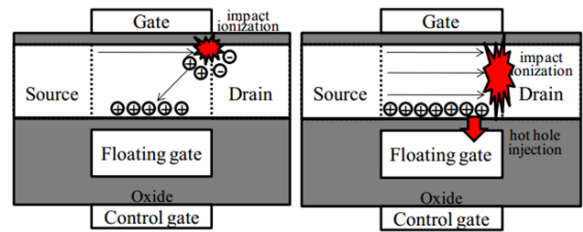

Fig. 6. Schematic view of (a) short term memory, (b) long term memory mechanism [8].

The final property is refractory period. If the neuron generates an output signal, the neuron will return to the initial state and not be affected by the input signal. Most of I&F neuron circuits use an additional transistor to discharge the capacitor. But this neuron circuit does not need an additional transistor as the holes accumulated in the floating body are erased after the generation of the output signal as shown in Fig. 3.

2. Silicon-Based Floating-Body Synaptic Transistor

The essential rolls of the biological synapse are transporting the signal between neurons and adjusting connection weight through experience for short or long term. Connection weight of the synapse is increased as the stimulus is transported through the synapse. And about thousand synapses are linked with a neuron. To perform the synaptic activity, we proposed silicon based synaptic transistor [3]. Fig. 6 shows the synaptic device structure. The structure is based on a floating body transistor for short term memory and utilizes a back floating gate and a back gate for long term memory and STDP. Because it is four-terminal device, it is easier to implement STDP in logic circuit than two-terminal device.

The important consideration is the number of synapse per a neuron. The biological neuron can have about thousand synapses. Therefore, the number of devices that comprises a synapse has to be minimized. To minimize it, we have used current mirror circuit shown in Fig. 1. As the number of input signals from different synapses increases, V_{syn} also increases proportional to the number of input as shown in Fig. 8. It is the spatial integration property of the neuron.

Short term potentiation: When the input pulse is applied to the gate and drain of the synaptic device, its
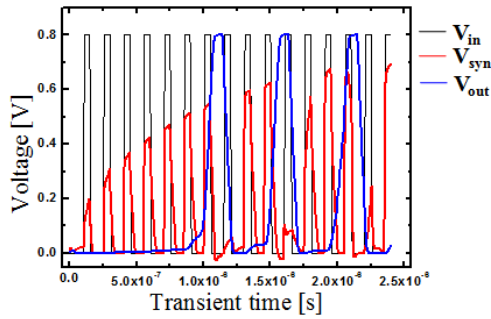
Fig. 7. V_{syn} is increased at every input pulse due to the decreased threshold voltage of the synaptic device.
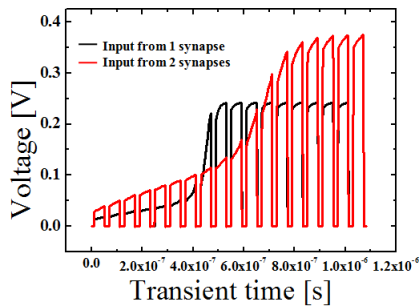

Fig. 8. Simulation result of post synapse voltage according to the number of input pulse. As the number of input signal from different synapses increase, V_{syn} is also increase proportional to the number of input.

conductance is increased and the threshold voltage is decreased temporarily due to the excess holes made by impact ionization in the floating body. When the holes in the floating body are saturated, newly generated holes are injected into floating gate by negative back gate bias from feedback and the hole injection results in long term memory as shown in Fig. 6. Fig. 7 shows the adjusted connection weight through experience. V_{in} is the pre-synaptic pulse from pre-neuron. V_{syn} is post-synaptic signal through synaptic transistor, to be transported to dendrite of the neuron circuit. V_{out} is the output pulse of the neuron circuit (Fig. 1). V_{syn} is increased by the input pulse because of the excess holes made by impact ionization in the floating body. It means that the synaptic device learns through experience. Before synaptic device learning, the neuron circuit requires many input pulses to generate output voltage. But, after the synaptic device learning, the neuron circuit needs just one or two input pulses for firing (Fig. 7).
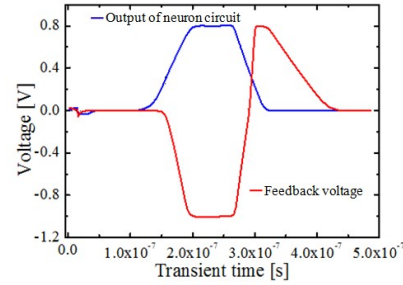

Fig. 9. Feedback voltage for STDP generates negative and positive bias continuously.
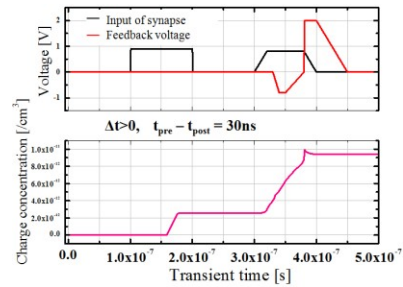

Fig. 10. Charge concentration in the floating gate, when relative timing difference (Δt) is positive.

3. Spike Timing Dependent Plasticity (STDP) for Long Term Potentiation and Depression

STDP is an advanced synaptic function to change synaptic weight. It is a form of plasticity driven by precise spike timing differences between pre-synaptic and post- synaptic spikes [12]. Most of two-terminal device such as memristor, additional transistor is needed for STDP expression [10]. We used four-terminal device for long- term memory and STDP (Fig. 6) and a feedback circuit was added to the neuron circuit (Fig. 1). The n-channel MOSFET linked with the output in the feedback circuit has high threshold voltage due to negative source voltage. As the I&F neuron circuit makes output voltage, the feedback circuit generates negative and positive bias continuously shown in Fig. 9. The feedback voltage is applied to all back gate of the synaptic transistors connected with the neuron circuit. In this circuit, the input of synapse is presynaptic pulse and the feedback voltage is postsynaptic pulse. The holes are injected into the back floating gate when the presynaptic pulse spikes before the postsynaptic pulse as shown in Fig. 10. As the gate and drain of the synaptic transistor is positive biased, the excess holes are made by impact ionization. At that time, the excess holes are injected to the back floating
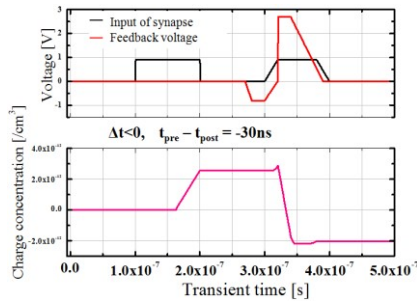
Fig. 11. Charge concentration in the floating gate, when relative timing difference (Δt) is negative.
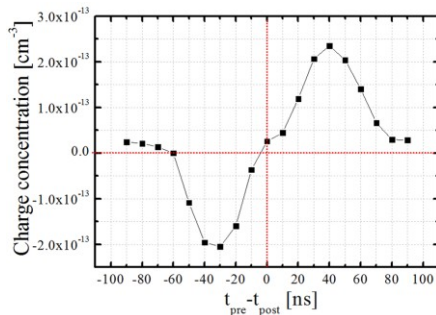

Fig. 12. Simulated charge concentration in the floating gate versus relative timing difference.

gate because the back gate is negative biased. If the holes are trapped into the back floating gate, the current drivability of the synaptic device will be increased which it means long term potentiation of the synaptic weight. Oppositely, the electrons are injected into the back floating gate when the presynaptic pulse spikes after the postsynaptic pulse as shown in Fig. 11. If the electrons are saved into the back floating gate, the current drivability of the synaptic device will be decreased which means long term depression. Fig. 12 shows the charge concentration in the floating gate versus the relative timing difference between pre and post- synaptic neuron, verifying that STDP characteristic is similar to that of biological synapse. When the relative timing difference is positive, there are positive charges (hole) in the floating gate, and the conductance is increased. And if the relative timing difference is negative, there are negative charges (electron) in the floating gate.

III. CONCLUSIONS

In this work, we connected synaptic device and I&F neuron circuit using current mirror circuit. We verified STDP characteristics using four-terminal synaptic device without clock or controller. The number of device per a synapse is minimized, just one device is used. The total chip size is reduced dramatically, since thousands of synapses are connected to a neuron circuit. We emulated the essential property of the biological neuron and synapse such as spatial and temporal integration, all-or-none property, synaptic learning, short term and long term memory.

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