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Accurate RF C-V Method to Extract Effective Channel Length and Parasitic Capacitance of Deep-Submicron LDD MOSFETs

Sangjun Lee and Seonghearn Lee

***Abstract*—A new paired gate-source voltage RF capacitance-voltage (C-V) method of extracting the effective channel length and parasitic capacitance using the intersection between two closely spaced linear regression lines of the gate capacitance versus gate length measured from S-parameters is proposed to remove errors from conventional C-V methods. Physically verified results are obtained at the gate-source voltage range where the slope of the gate capacitance versus gate-source voltage is maximized in the inversion region. The accuracy of this method is demonstrated by finding extracted value corresponding to the metallurgical channel length.**

***Index Terms*—MOSFET, CMOS, parameter extraction, effective channel length, parasitic capacitance, modeling, RF C-V, S-parameter**

I. INTRODUCTION

An effective channel length L_{eff} is an important parameter in MOSFETs for process monitoring, analysis of short-channel characteristics, and SPICE compact modeling. In order to extract bias-dependent L_{eff} and external resistance R_{EXT}, a conventional paired gate-source voltage V_{GS} DC method to obtain the intersection of the linear regression lines of the total channel resistance R_{TOT} as a function of the total gate length L_g with various V_{GS} has been widely used [1-3].

Since DC measurement of R_{TOT} is carried out at non-zero gate-drain voltage V_{DS}, the channel mobility is degraded by the lateral field effect in deep-submicron MOSFETs, thus resulting in an extraction error of L_{eff}. To eliminate this error, RF C-V methods [4-7] to extract the gate-channel capacitance C_{GC} from measured S-parameters at V_{DS} = 0 V have been used to determine L_{eff}.

For accurate extraction of C_{GC}, the extrinsic parasitic capacitance C_p outside the channel area should be eliminated from the measured gate capacitance C_G in the inversion region. In general, C_p is expressed as the sum of C_{of}, C_{ov}, and C_{if} where C_{of} is the outer fringing capacitance, C_{ov} is the bias-dependent gate to source/drain overlap capacitance, and C_{if} is the bias-dependent inner fringing capacitance caused by the depletion region between the LDD(lightly doped drain) and poly Si gate [7-9].

Conventionally, two methods based on the determination of C_p have been well known to extract C_{GC} [3-6]. First a zero-bias method using C_p measured at V_{GS} = 0 V leads to a L_{eff} extraction error, because C_{if} existing at V_{GS} = 0 V is added to C_P. Second an accumulation method using C_p measured in the accumulation region also produces a L_{eff} extraction error, because accumulated majority carriers make the LDD inverted.

In order to avoid these C_p extraction errors, a simple method [7] using the ratio of maximum C_G values between two short and long channel devices in the inversion region has been reported to remove the C_{if} error in determining L_{eff}. However, it also produces large

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Department of Electronic Engineering, Hankuk University of Foreign Studies, San 89, Wangsan-ri, Mohyun-myun, Yongin, Kyungki-do 449-791, Korea
E-mail : shlee@hufs.ac.kr

errors in deep-submicron MOSFETs, because C_{of} and C_{ov} still exist in strong inversion condition.

In order to eliminate these problems in these conventional methods, in this paper, we propose a new paired V_{GS} RF capacitance-voltage (C-V) method to extract L_{eff} using the intersection of linear regression lines in C_G versus gate length L_g in the inversion region. This method is very accurate, because L_{eff} and C_p are determined simultaneously without errors from the conventional ones.

II. MEASUREMENT AND ANALYSIS

S-parameters are measured on multi-finger N-MOSFETs fabricated using 0.13 μm RF CMOS process technology with the number of gate finger ($N_f = 16$), unit finger width (Wu = 2.5 μm), and gate length (L_g = 0.13, 0.18, 0.25 and 0.35 μm) at V_{DS} = 0 V with various V_{GS}. The accurate de-embedding procedure was carried out to remove pad and interconnection parasitics from the S-parameters [10]. Using a RF direct extraction method under the assumption of $C_{GD} = C_{GS}$ where C_{GD} is the gate-drain capacitance and C_{GS} is the gate-source capacitance, at V_{DS} = 0 V for MOSFETs with symmetric drain and source structure [6] C_G is determined in the low frequency (LF) region using :

$$C_G = 2C_{GD} \approx (-2/\omega)\,\mathrm{Imag}(Y_{12})_{LF} \qquad (1)$$

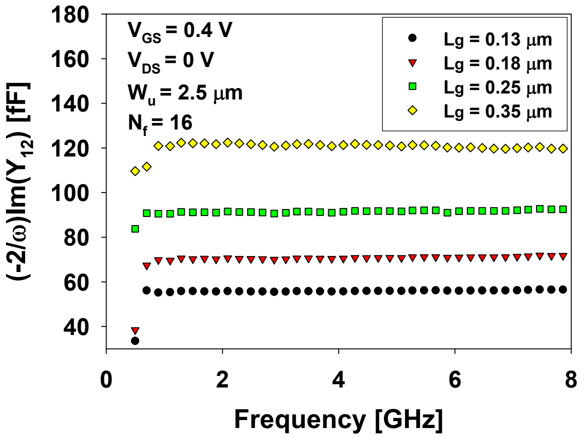

Fig. 1. Measured (−2/ω)Imag(Y_{12}) vs. frequency at various L_g.

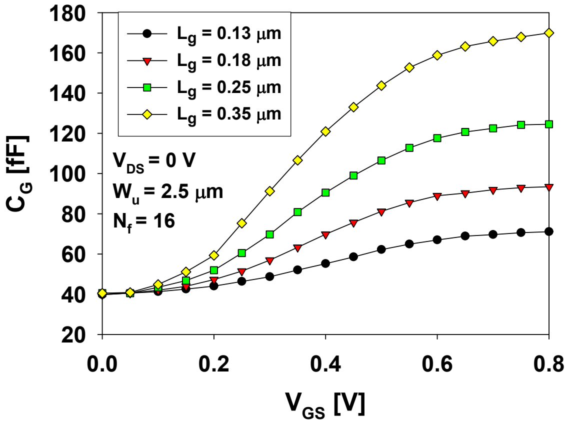

Fig. 2. V_{GS}-dependent curves of extracted C_G at various L_g.

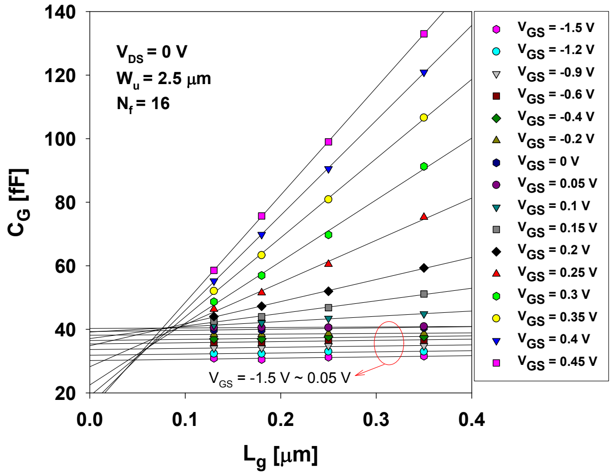

Fig. 3. Extracted data and regression lines of C_G versus L_g at various V_{GS}.

In Fig. 1, the low frequency data of about 1 GHz were chosen for C_G to neglect the influence of series resistances and inductances [4-6]. As shown in Fig. 2, the extracted C_G data linearly increase at 0.3 V < V_{GS} < 0.4 V and their increasing rate decreases at V_{GS} > 0.4 V.

In order to accurately analyze the V_{GS}-dependent characteristics of C_p from C_G, linear regression lines of C_G are plotted as a function of L_g in Fig. 3. The value of C_p corresponding to C_G data at V_{GS} < 0.05 V is shown to be irrelevant to L_g in Figs. 2 and 3. In Fig. 3, C_p increases at higher values at -1.5 V < V_{GS} < 0.05 V above the flatband voltage, because the depletion capacitance in the surface of n^- lightly doped drain (LDD) region under the gate oxide becomes larger with increasing V_{GS}. Thus, C_{ov} consisting of series connection of the surface depletion capacitance and oxide capacitance increases. In this case, C_{if} also increases because the depletion layer between n^-

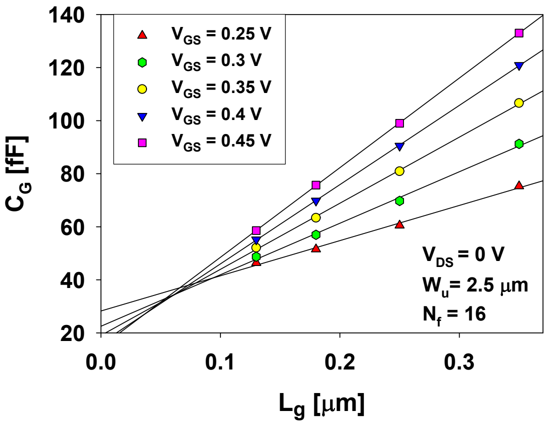

Fig. 4. Linear regression lines of extracted C_G data versus L_g at 0.25 V < V_{GS} < 0.45 V.

LDD and p-channel region is expanded into the channel region until the formation of inversion channel.

In Fig. 3, the linear regression line slopes begin to increase slightly from V_{GS} = 0.1 V, because the very weak inversion channel is formed. In the range of V_{GS} = 0.3 V ~ 0.4 V, the slopes in Fig. 3 appear to increase linearly due to the rise of strong inversion channel capacitance in Fig. 2. The increasing rate of the slope starts to decrease from V_{GS} = 0.4 V.

III. EXTRACTION

Based on the linear-dependence of C_{GC} on L_g, C_G is expressed as:

$$C_G = C_{ch}L_{eff} + C_p = C_{ch}(L_g - \Delta L) + C_p \tag{2}$$

where C_{ch} and ΔL are defined as the bias-dependent C_{GC} per unit length and the channel length reduction, respectively.

According to (2), the linear regression lines of C_G versus L_g at different V_{GS} should intersect at the same point (ΔL, C_p), because C_{ch} varies with V_{GS}. Fig. 4 shows that the intersections of ΔL and C_p are changed with varying V_{GS}, indicating that ΔL and C_p are V_{GS}-dependent.

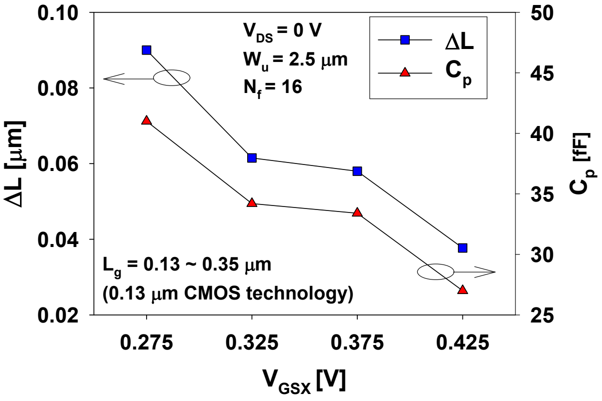

Fig. 5. ΔL and C_p versus V_{GSX} extracted at 0.25 V < V_{GSX} < 0.45 V using the new method. V_{GSX} is the average voltage of each V_{GS} pair in Fig. 4. These extraction results are obtained from N-MOSFETs (L_g = 0.13, 0.18, 0.25, 0.35 μm) fabricated using same 0.13 μm RF CMOS process technology.

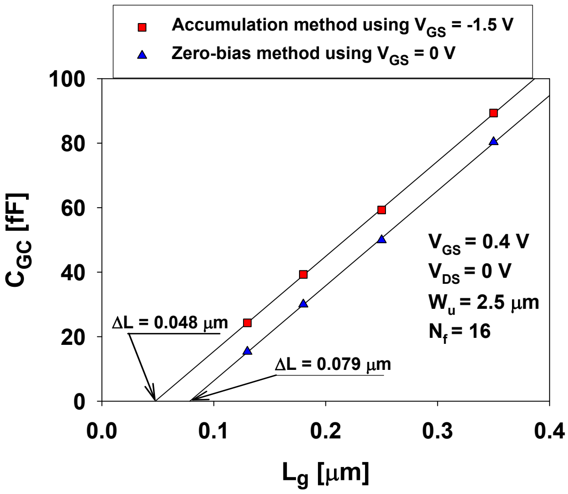

Fig. 6. C_{GC} versus L_g using two conventional methods.

Therefore, ΔL and C_p in the inversion region should be determined from the intersection between two adjacent linear regression lines with small V_{GS} differences to ignore the V_{GS}-dependence in Fig. 4. This new paired V_{GS} RF C-V method is similar to the conventional paired V_{GS} DC method [1-3]. However, this method is able to extract ΔL and C_p simultaneously without the L_g-dependent error of the short-channel mobility caused by the lateral field effect. Using this new method, ΔL and C_p extracted at the average voltage V_{GSX} of a V_{GS} pair used for the intersection in Fig. 4 are plotted in Fig. 5.

IV. DISCUSSION

As shown in Fig. 5, ΔL and C_p abruptly decrease with increasing V_{GSX}. In order to analyze the physical validity, ΔL is extracted using conventional zero and accumulation methods [3-6] shown in Fig. 6. The values of C_{GC} at various L_g are extracted by subtracting C_p at the same L_g in Fig. 3 from measured C_G at V_{GS} = 0.4 V. From the x-intercept of C_{GC} versus L_g in Fig. 6, it is obtained that $\Delta L = 0.079$ μm from the zero-bias method and $\Delta L = 0.048$ μm from the accumulation method.

However, since the data of C_p at $V_{GS} = 0$ V in Fig. 3 contain extra value of C_{if} disappeared in the inversion region, unphysically large capacitance values are removed from C_G for each L_g. Therefore, the extracted value of ΔL using the zero-bias method is overestimated. On the contrary, the extracted ΔL using the accumulation method is underestimated, because unphysically small values of C_p reduced in the accumulation region at $V_{GS} = -1.5$ V in Fig. 3 are removed from C_G for each L_g. Since the new paired V_{GS} RF C-V method uses the intersection of two linear regression lines for C_G versus L_g in the inversion region, it is possible to determine ΔL and C_p accurately without the C_p errors.

As L_g is scaled down, the influence of C_p on the determination of C_{GC} increases because C_G is reduced. Thus, the reliability of conventional methods based on the removal of C_p is more seriously deteriorated due to the inaccuracy of the C_p extraction at shorter L_g. However, the new method is theoretically more accurate than the conventional ones, because removal process of C_p is not needed.

However, in Fig. 5, ΔL at $V_{GSX} = 0.275$ V is larger than the overestimated value of the zero-bias method and ΔL at $V_{GSX} = 0.425$ V is smaller than the underestimated value of the accumulation method. This unphysical extraction at $V_{GSX} = 0.275$ V and 0.425 V is generated because the increasing rate in the nonlinear region of C_G versus V_{GS} is irregularly varied at different L_g in Fig. 2. If a regression error due to this irregular slope change in the range of L_g occurs, this intersection becomes inaccurate. Since a V_{GS}-dependent slope C_{ch} in (2) should be independent of L_g to prevent this inaccuracy of ΔL, the intersection should be extracted in the linear region of C-V curve in $0.3 \text{ V} < V_{GS} < 0.4$ V where the increasing rate of C_G versus V_{GS} is maximized.

In this valid range of V_{GS}, the values of $\Delta L = 0.0615$ μm at $V_{GSX} = 0.325$ V and 0.058 μm at 0.375 V are physically acceptable because these are between the overestimated value of the zero-bias method and the underestimated one of the accumulation method. Due to the same reason, the extracted values of $C_p = 34.2$ fF at $V_{GSX} = 0.325$ V and 33.4 fF at $V_{GSX} = 0.375$ V that are smaller than C_p of 39.5 fF at $V_{GS} = 0$ V but larger than C_p of 30 fF at $V_{GS} = -1.5$ V are also valid. These physical results are obtained because the intersections are determined in the linear C_G-V_{GS} region with a maximum slope. When the channel carrier density increased at larger V_{GS} is higher than the doping density in the n^- LDD region, the n^- LDD overlap length is reduced [1]. Thus, the extracted ΔL at $V_{GSX} = 0.375$ V is slightly shorter than that at 0.325 V in Fig. 5.

In order to verify the accuracy of the new method, another extraction method [11] to obtain the metallurgical channel length L_{met} is performed as follows: The intrinsic gate-bulk capacitance C_{GBI} is extracted by subtracting the extrinsic gate-bulk capacitance C_{GBE} at $V_{GS} = 0.4$ V from the gate-bulk capacitance C_{GB} at $V_{GS} = -1.5$ V by using Y-parameter equation: $C_{GB} = (1/\omega)\text{Imag}(Y_{11}+2Y_{12})$ converted from S-parameters. When a decreasing rate of the overlap and depletion length L_{OD} extracted from x-intercept data of C_{GBI} versus L_g has a maximum at $V_{GS} = -1.5$ V, the n^- LDD overlap length L_{ov} to obtain L_{met} is determined to be 0.058 μm. This value of L_{ov} agrees well with ΔL at $V_{GSX} = 0.325$ V and 0.375 V, verifying the accuracy of the new method.

The new method is much simpler than the one using C_{GBI} because the complex procedure to extract L_{OD} is not needed. Since ΔL is extracted in the inversion region, it is physically more accurate than the C_{GBI} method in the accumulation region.

V. CONCLUSIONS

We propose a new paired V_{GS} RF C-V method to extract ΔL and C_p simultaneously from the intersection between two closely spaced linear regression lines of C_G versus L_g in the linear region of C_G versus V_{GS} where the slope is maximized. Its validity is confirmed by observing more physical results than conventional C-V methods. The accuracy of this method is verified by finding the excellent correspondence to the metallurgical channel length obtained using L_g-dependent C_{GBI} data.

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REFERENCES

[1] G. J. Hu, C. Chang, and Y. T. Chia, “Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 34, no. 12, pp. 2469-2475, 1987.

[2] K. Takeuchi, N. Kasai, T. Kunio, and K. Terada, “An effective cannel length determination method for LDD MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 580-587, 1996.

[3] N. Arora, *MOSFET modeling for VLSI simulation theory and practice*, World Scientific, 2007.

[4] S. Lee, “A new RF capacitance method to extract the effective channel length of MOSFET’s using S-parameters,” *in Proc. IEEE Hong Kong Electron Devices Meet.*, 2000, pp. 56-59.

[5] S. Lee and S. Youn, “Improved extraction method for effective channel length of deep-submicron MOSFETs,” *Electron. Lett.*, vol. 40, no. 4, pp. 274-276, 2004.

[6] J.-Y. Kim, M.-K. Choi, and S. Lee, “Accuracy analysis of extraction method for effective channel length in deep-submicron MOSFETs,” *J. Semicond. Technol. Sci.*, vol. 11, no. 2, pp. 130-133, 2011.

[7] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, “Improved split C-V method for effective mobility extraction in sub 0.1 μm Si MOSFETs,” *IEEE Electron Device Lett.*, vol. 25 no. 8, pp. 583-585, 2004.

[8] F. Prégaldiny, C. Lallement, and D. Mathiot, “A simple efficient model of parasitic capacitances of deep-submicron LDD MOSFETs,” *Solid-State Electron.*, vol. 46, no. 12, pp. 2191-2198, 2002.

[9] S. Severi, L. Pantisano, E. Augendre, E. San Andres, P. Eyben, and K. De Meyer, “A reliable metric for mobility extraction of short channel MOSFETs,” *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2690-2698, 2007.

[10] J.-Y. Kim, M.–K. Choi, and S. Lee, “A “thru-short-open” deembedding method for accurate on-wafer RF measurements of nanoscale MOSFETs,” *J. Semicond. Technol. Sci.*, vol. 12, no. 1, pp. 53-58, 2012.

[11] J.–Y. Kim, B.–H. Ko, M.-K. Choi, and S. Lee, “RF extraction method for source/drain overlap and depletion length of deep-submicron RF MOSFETs using intrinsic gate-bulk capacitance,” *Electron. Lett.*, vol. 46, no. 23, pp. 1566-1568, 2010.

Sangjun Lee was born in Seoul, Korea, in 1984. He received the B.S. degree in electronics and information engineering in 2012 from Korea University, Sejong, Korea, and the M.S. degree in electronic engineering from the Hankuk University of Foreign Studies, Yongin, Korea in 2015. His current research work is focused on RF CMOS modeling and parameter extraction for RF circuit design.

Seonghearn Lee was born in Junjoo, Korea, in 1962. He received the B.E. degree in electronic engineering in 1985 from Korea University, Seoul, Korea, and the M.S. and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis, in 1989 and 1992, respectively. His doctoral dissertation work involved the design, fabrication, and parameter extraction of AlGaAs/GaAs heterojunction bipolar transistors. From 1992 to 1995, he was a Senior Member of the Research Staff with the Semiconductor Technology Division, Electronics and Telecommunications Research Institute, Taejon, Korea, where he worked on the development of polysilicon emitter bipolar transistors and Si/SiGe/Si heterojunction bipolar transistors. Since 1995, he has been with the Department of Electronic Engineering, Hankuk University of Foreign Studies, Yongin, Korea, where he is currently a Professor. Since 1996, he has carried out research on RF CMOS and bipolar compact modeling for the RF circuit design in wireless communications applications. In 2013, he successfully developed SPICE model library for SOI RF CMOS Process at the National NanoFab Center, Taejon, Korea. His research interests are in the field of design, modeling, and characterization of silicon and compound semiconductor devices for use in high-frequency integrated circuits. Prof. Lee is a senior member of the IEEE Electron Devices Society and a member of the Institute of Electronics and Information Engineers. He received the HUFS Excellence in Research Award from the Hankuk University of Foreign Studies, in 2001, 2003, and 2004. He has been listed in *Who’s Who in the World* and *Who’s Who in Asia*.