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Current-Steered Active Balun with Phase Correction

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***Abstract*—An active balun using current steering for phase correction is presented. The proposed active balun is constructed with two different unit balun structures based on current steering to reduce phase and amplitude errors. This type of topology can be compared with the conventional phase and amplitude correction techniques which do not incorporate the current steering. Designed and fabricated active balun in 0.18 μm CMOS process operates over 0.95 - 1.45 GHz band, showing input reflection coefficient under -15 dB, phase error of 11° and gain error of 0.5 dB. Gain is measured to be 0.3 dB maximum and power consumption of 7.2 mW is measured.**

***Index Terms*—Active balun, current steering, phase correction technique, phase imbalance, gain imbalance**

I. INTRODUCTION

In wireless communication systems a number of circuits are designed using differential structure because of less even-order distortion and common-mode noise. However since antenna usually takes single port, balun is indispensable for conversion of single-ended signal to differential signal and vice versa. Baluns take two types in passive or active circuits. Passive baluns can be fabricated in on-chip for millimeter-wave systems, leading to signal attenuation [1]. To tackle this inherent weakness, active baluns have been paid considerable attentions [2-4].

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Phase correction technique has been sometimes used for active baluns, where inevitable phase imbalance can be alleviated by adjusting the phase of balanced output signals adequately [5]. The conventional active baluns capitalize opposite frequency-vs-phase responses of two different amplifiers which can be mainly made up of common source and common gate configurations. Due to inherent different phase response between these two configurations, it is quite difficult to obtain exactly same amplitude and opposite phase characteristics using these amplifier configurations for constituting excellent active baluns in terms of low amplitude and phase errors.

In this work, we devise an active balun using current steering to provide pliable gain and phase adjustment based on two different unit balun structures, leading to low phase and gain errors. Design philosophy and fabricated results are presented along with simulation and layout in 0.18 μm CMOS technology.

II. THE PROPOSED ACTIVE BALUN

The fundamental principle of active baluns uses the characteristic of MOSFET amplifiers which can provide opposite phase responses for common-source and common-gate configurations [6-9]. The proposed active balun comprised of two different unit circuits is drawn in Fig. 1, where M_1 and M_2 are initially devised for wide input matching circuit using common-gate configuration. M_3 - M_5 construct a unit circuit described as balun 1 in Figs. 1 and 2. M_6 - M_7 and M_8 - M_9 pairs build the other unit circuits depicted in Figs. 1 and 2 as balun 2. The proposed active balun can be analyzed properly by cascoding these two unit circuits. Amplitude and phase imbalances at the balanced output always occur due to gain and phase mismatches of two unit circuits as

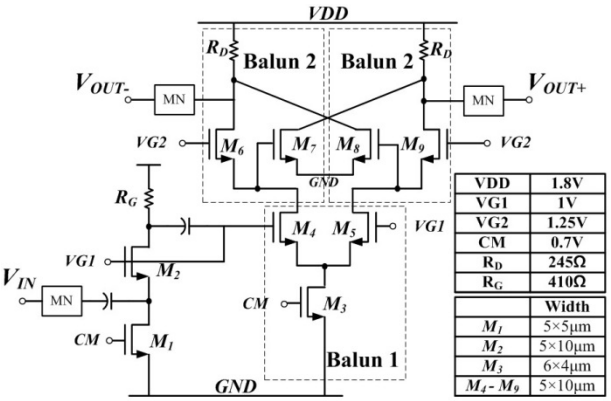


Fig. 1. Circuit of the proposed active balun.

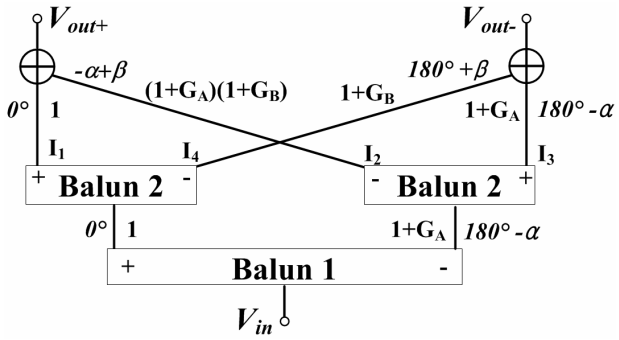


Fig. 2. Phase and amplitude imbalances of the proposed active balun.

represented in Fig. 2.

The principle of phase correction to reduce phase imbalance is symbolized in Fig. 2 which is constituted with two unit circuits [5]. Two unit circuits provide unequal phase-vs-frequency response. The outputs of balun 1 result in phase difference of 180˚-α, which means phase error of -α. Also the outputs of balun 2 yield phase difference of 180˚+β which means phase error of β where α and β take positive numbers. The reason why negative phase error is used for balun 1 is because balun 1 should be designed for ensuring phase difference less than 180˚. Phase difference greater than 180˚ corresponds to balun 2 as well. Phases of V_{out}+ and V_{out}- without gain error can be expressed as in (1):

$$\begin{aligned} \angle V_{out}+ &= \frac{-\alpha+\beta}{2} \\ \angle V_{out}- &= 180^\circ + \frac{-\alpha+\beta}{2} \end{aligned} \tag{1}$$

Therefore the phase imbalance (*i.e.* phase error) between V_{out}+ and V_{out}- becomes zero when gain imbalance (*i.e.* gain error) is not considered.

To calculate the total phase imbalance between V_{out}+ and V_{out}- considering gain imbalances as shown in Fig. 2, output signals of I_1 - I_4 are characterized with gain errors (G_A and G_B) and phase errors (α and β) of unit circuits as described in (2) [5] :

$$\begin{aligned} I_1 &= \sin\omega t \\ I_2 &= (1+G_A)(1+G_B)\sin(\omega t-\alpha+\beta) \\ I_3 &= -(1+G_A)\sin(\omega t-\alpha) \\ I_4 &= -(1+G_B)\sin(\omega t+\beta) \end{aligned} \tag{2}$$

Consequently the total phase error (PE) manifests itself in difference between phases of V_{out}+ and V_{out}- which is calculated as vector summation of I_1, I_2 and I_3, I_4, respectively, leading to (3) [5]:

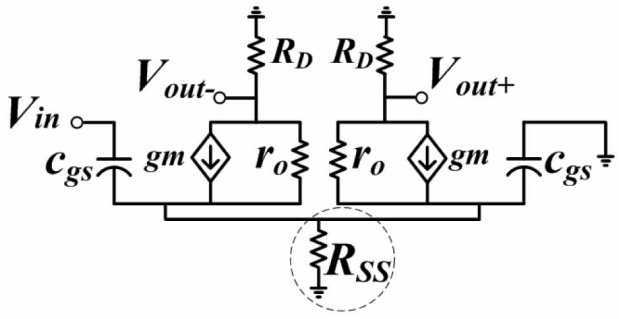
$$\begin{aligned} PE &= \left|\angle V_{out+} - \angle V_{out-}\right| - 180^\circ \\ &= \tan^{-1}\left[\frac{G_A-G_B}{2+G_A+G_B}\cdot\tan\left(\frac{-\alpha-\beta}{2}\right)\right] \\ &\quad -\tan^{-1}\left[\frac{G_A+G_B+G_AG_B}{2+G_A+G_B+G_AG_B}\cdot\tan\left(\frac{-\alpha+\beta}{2}\right)\right] \end{aligned} \tag{3}$$

where if G_A and G_B approach 0, phase error goes to 0.

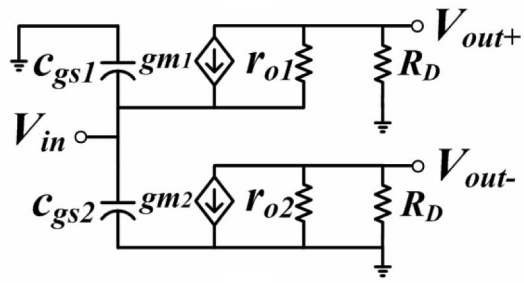
To correct phase imbalance in [5], FETs in balun 1 (M5 and M6 in [5]) must be designed in the same DC conditions and the voltage gains of M5 and M6 in [5] should be maintained to be exactly 0 dB, which is not easy. In order to overcome this limit, we propose the current-steering architecture for balun 1 which can be easily designed and provides the optimum point for gain and phase errors as shown in Fig. 4.

Equivalent circuit for balun 1 in Fig. 1 can be represented as shown in Fig. 3(a), where G_A is derived as in (4). G_A goes to 0 when tail current acts as an ideal current source (*i.e.* $R_{SS} = \infty$). However, R_{SS} is finite due to short channel effect, thus gain error of balun 1 cannot be avoided. Maintaining voltage gain, R_{SS} should be obtained as large as possible for balun 1.

$$G_A = \left|\frac{R_D+r_O}{1+g_mr_O}\left[\frac{1+\left(\frac{1}{R_{SS}}+j\omega C_{gs}+\frac{1+g_mr_O}{R_D+r_O}\right)\frac{g_mr_O}{j\omega C_{gs}}}{r_O+R_D+\frac{g_mr_O}{j\omega C_{gs}}}\right]\right| - 1 \tag{4}$$



(a)



(b)

Fig. 3. Equivalent circuit for the proposed circuit (a) balun 1, (b) balun 2.

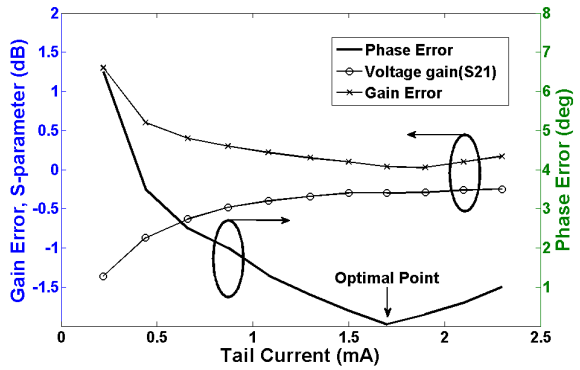


Fig. 4. Simulated results with tail current analysis.

where for G_A = 0, R_{SS} should be infinity. Similarly, equivalent circuit for balun 2 is drawn as shown in Fig. 3(b) where both transistors do not constitute DC symmetry unlike balun 1. G_B is expressed as in (5) where transconductance difference contributes to gain error.

$$G_B = \left| \frac{g_{m1}(R_D \parallel r_{O1})}{g_{m2}(R_D \parallel r_{O2}) + \dfrac{R_D}{r_{O2} + R_D}} \right| - 1 \cong \frac{g_{m1}}{g_{m2}} - 1 \quad (5)$$

Since two unit circuits need different design approaches, it is necessary to find out an optimal design

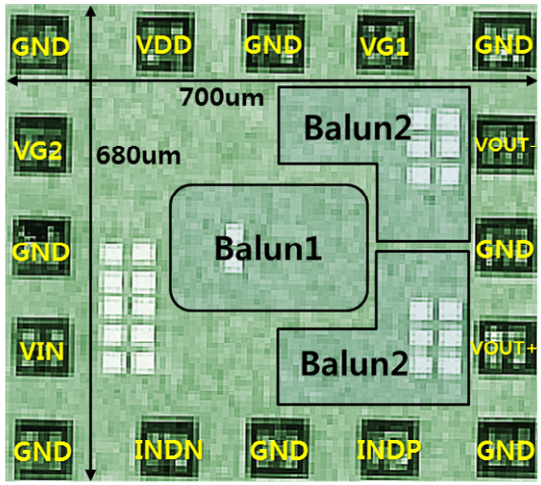


Fig. 5. Micro-photograph of the fabricated active balun.

where tail current plays a critical role in reducing G_A and G_B, and then P_E as deduced in (3)-(5). (3)-(5) are computed based on the parasitics of FET, these are valid as long as the operating frequency is lower than the unit gain frequency (f_T) of FET. Steering the tail current, the proposed balun is simulated, providing phase error, gain error and voltage gain as illustrated in Fig. 4. It reveals that phase and gain errors can be optimized around tail current of 1.7 mA or 1.8 mA.

Since G_A in balun 1 is unavoidable, minimizing G_B of balun 2 with maintaining the voltage gain of balun 1 ensures reduction of phase error of the whole circuit. From overall analysis, the proposed circuit performs design optimization by adjusting the tail current. Furthermore, phase correction is performed using symmetry of balun 2 and configuration of balun 1 allows a design freedom. For a design procedure, the input matching stage (M_1 and M_2) is firstly designed, next balun 1 and balun 2 are individually devised, and finally tail current is adjusted together with optimizing balun 1 and balun 2. The whole biasing and transistor dimensions are shown right below in Fig. 1.

III. Measurement Results

The designed active balun is fabricated in 1P6M 0.18 μm standard CMOS technology as shown in Fig. 5. The chip area including pads takes 700 μm x 680 μm excluding the input and output matching networks.

Parasitic capacitances and resistances are extracted and used for post-layout simulation. Die chip was bond-

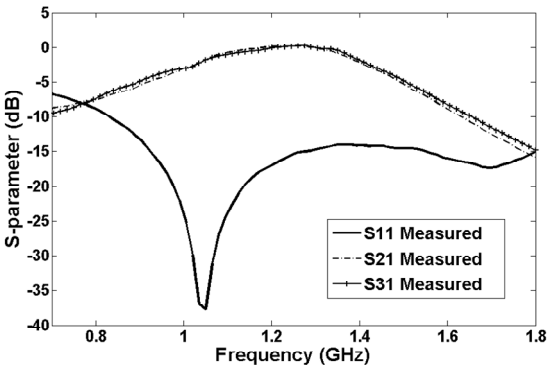


Fig. 6. Measured S-parameters.

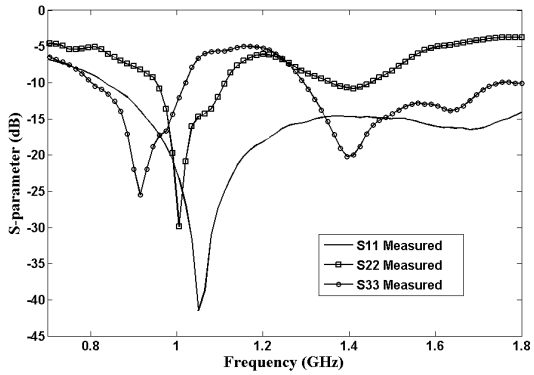


Fig. 7. Measured matching performances.

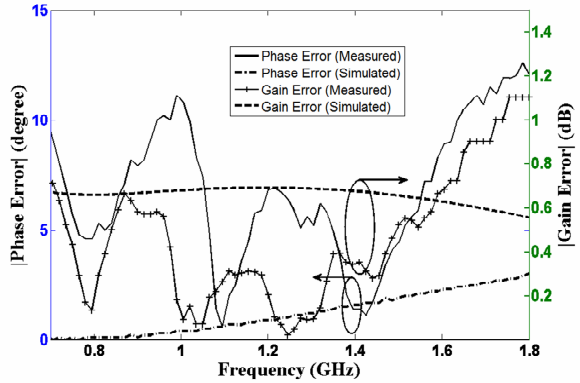


Fig. 8. Measured output phase and gain errors.

wired in a PC board to perform experiments. S-parameter measurements are shown in Figs. 6 and 7, where S_{21} and S_{31} show 0.3 dB maximum at 1.2 GHz. Bandwidth in terms of S_{21} and S_{31} is measured to be 0.5 GHz (0.95 - 1.45 GHz) where measured S_{11} is maintained under -15 dB. Also, output reflection coefficients, S_{22} and S_{33}, are less than -6 dB as shown in Fig. 7. Fig. 8 shows phase and gain errors at the balanced output port of the designed balun, where simulation shows 2˚ and 0.7 dB maximum, and measurement shows 11˚ and 0.5 dB maximum. Primary cause for deviation of phase error between simulation and measurement stems from parasitic series inductances of bonded wire used for connecting the die chip to a PC board which was not accurately included during simulation. Measured performances are compared with other previous works as summarized in Table 1 where the proposed active balun shows comparable results in terms of gain error, gain and power consumption in spite of a bit large phase error. Relatively low power consumption originates from low gain and optimized current steering for reducing gain and phase errors.

Table 1. Comparison of Active baluns

	BW (GHz)	GE (dB)	PE (º)	Gain (dB)	P_{DC} (mW)	Area (mm^2)
[2]	2-40	0.5	-	-1~1	40	0.56
[3]	DC-21	1.2	5	1.4~4.3	177	0.562
[5]	60.4-66.6	1.7	6.8	17.6*	19	0.275
[6]	0.2-5.2	0.7	2	13~15.6	21	-
[10]	1-2	1	2	9.3	9	N/A
[11]	0-8	2.7	4	N/A	1.44	N/A
This work	0.95-1.45	0.5	11	-3~0.3	7.2	0.476

* includes LNA

IV. CONCLUSION

An active balun using phase correction technique based on current steering is presented. The proposed architecture is devised efficiently to correct phase and gain errors compared with the conventional active baluns. Designed active balun shows bandwidth of 0.5 GHz where maximum phase error of 11˚ and maximum gain error of 0.5 dB in measurement as well as relatively low power consumption of 7.2 mW.

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