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Triple Material Surrounding Gate (TMSG) Nanoscale Tunnel FET-Analytical Modeling and Simulation

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Abstract—**In the nanoscale regime, many multigate devices are explored to reduce their size further and to enhance their performance. In this paper, design of a novel device called, Triple Material Surrounding Gate Tunnel Field effect transistor (TMSGTFET) has been developed and proposed. The advantages of surrounding gate and tunnel FET are combined to form a new structure. The gate material surrounding the device is replaced by three gate materials of different work functions in order to curb the short channel effects. A 2-D analytical modeling of the surface potential, lateral electric field, vertical electric field and drain current of the device is done, and the results are discussed. A step up potential profile is obtained which screens the drain potential, thus reducing the drain control over the channel. This results in appreciable diminishing of short channel effects and hot carrier effects. The proposed model also shows improved ON current. The excellent device characteristics predicted by the model are validated using TCAD simulation, thus ensuring the accuracy of our model.**

Index Terms—**Band to band tunneling, work function, TMSGTFET, short channel effects, gated p-i-n diode**

I. INTRODUCTION

Today semiconductor electronics enjoy an accelerating growth in performance and complexity. This fantastic progress is due to steady downscaling of MOSFET technology, needed to meet the requirements for speed, complexity, circuit density and power consumption. The device downscaling leads to the emergence of many new novel nanostructures, assuring high functionality, high device drive, and low power consumption which are the critical factors for the progress of electronics. But, however this shrinking of channel length leads to undesirable effects called short channel effects(SCEs) which degrades the device performance. Hence, the study of SCEs has become very crucial as they seriously challenge the efforts of downscaling the MOS technology.

As continuous reduction of feature sizes of MOSFETs reaches fundamental performance limitations, new devices, that uses tunneling for their ON-current [1-4] are needed to be explored. As theoretically analyzed by Zhang et al. [5], one such promising device is Tunnel FET that substitutes conventional MOSFETs for low power applications. A TFET can fulfill the same role in a circuit as a MOSFET and has the attractive advantages over a MOSFET in terms of subthreshold swing below 60mV/dec and low leakage current in the range of femtoamperes [2, 6, 7].

In order to suppress the SCEs, gate engineering and channel engineering novel techniques, which includes double gate, dual material gate, dual material double gate, surrounding gate, Ω-gate, ∏-gate, high-K dielectric, are adopted to have best control of the channel by the gate. Out of these multigate structures, surrounding gate have attracted significant research interest due to its astonishing feature of device geometry that offers high packing density. It shows improved gate control and excellent immunity against the undesirable SCEs. Further,

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a significant improvement in performance can be obtained by the innovative concept of gate material work function engineering. This technique uses gate with either two or three metals with different work functions. The step shape of the surface potential profile thus obtained, reduces the drain control over the channel and enhances immunity against SCEs and hot carrier effects [8, 9].

A number of simulation models of TFETs using different structures have been proposed to improve its electrical characteristics [1-9, 11, 12]. An improved ON-current and decreased subthreshold swing can be obtained by careful choice of a gate di-electric [12] in a double gate structure. But only a few analytical models of TFET are available in the recent years. Lee et al. proposed an analytical model for single gate TFET using superposition method [10]. Bardon et al. proposed a pseudo 2-D surface potential model for DGTFET and presented the analytical expressions for 2-D potential and electric field [11]. Our present endeavor merges the benefits of TFET and surrounding gate with three different gate material work functions. This novel nanoscale structure is explored and solved analytically using parabolic approximation technique.

II. Device Structure and Operation

TFETs attract attention because of their quantum tunneling barrier. When the device is turned on, the carriers must tunnel through the barrier in order for the current to flow from source to drain. During OFF condition, the presence of the barrier keeps the OFF-current extremely low in the range of femtoamperes, which is very much lower than the OFF current of conventional MOSFET [5, 10, 12].

TFETs are gated p-i-n diodes. For the n-type TFET, the n+ region is the drain, and p+ region is the source. When a positive voltage is applied to the drain, it reverse biases the p-i-n-diode and increasing the positive voltage in the gate is used to enable TFET conduction by electron band-to-band tunneling which occur from the valence band of the p+ source to the conduction band of the i-region and then move towards the n+ drain by drift diffusion. Tunneling occurs in the region of high electric field where the local band bending reduces the width of the forbidden band gap. This bending is done by using the gate voltage which pushes the energy bands downward in the intrinsic region [3, 12-14].

Rakhi Narang et al [15] reported a drain current model of a surrounding gate p-n-p-n Tunnel FET. Indeed the performance enhancement is achieved by implementing a surrounding gate with two or three materials with varying workfunctions, resulting in novel structures namely Dual Material Surrounding Gate Tunnel FET (DMSGTFET) and Triple Material Surrounding Gate Tunnel FET (TMSGTFET) respectively. Our proposed structure consists of surrounding gate made up of three different materials with different work functions. The source and drain are made up of highly doped p-type and n-type regions respectively. The intrinsic channel region is made up of a moderately doped n-type material. A S_iO_2 layer is used as a gate dielectric. The gate material work functions are chosen between 4 - 4.8 eV with Φ_{M1} = 4 eV (Sc), Φ_{M2} = 4.6 eV (Mo), Φ_{M3} = 4.8 eV (Au) [8]. The gate work function in the source side is less than the work function in the drain side. This results in low leakage current in the OFF state. In the ON state, the tunneling width decreases as the band overlap increases. Hence, there is a considerable rise in the tunneling probability in the source side, which results in improved ON current.

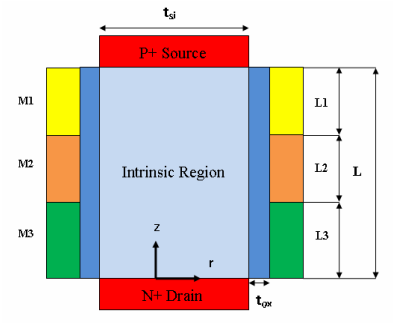
III. Model Formulation

A schematic view of Triple Material Surrounding Gate Tunnel FET is shown in Fig. 1 with three metal gate lengths L_1, L_2, and L_3. Due to the cylindrical symmetry of the proposed structure, a cylindrical co-ordinate system consisting of a radial direction r and a horizontal direction z is used.

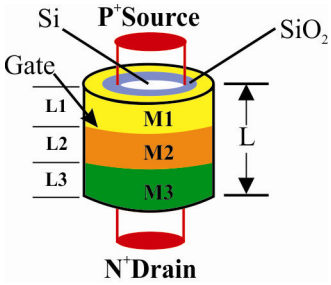
The potential and electric field have no variations with respect to the angle θ along the radial direction, due to the symmetry of the device structure. Hence, a two-dimensional analysis is sufficient for the modeling of the proposed structure. The surface potential, lateral electric field, vertical electric field and drain current of a triple material surrounding gate TFET are derived analytically for the first time using parabolic approximation technique.

1. Surface Potential

The potential profile is assumed to be parabolic along



(a)



(b)

Fig. 1. (a) Cross-sectional view, (b) Structure of Triple Material Surrounding Gate (TMSG) Tunnel FET.

the radial direction, and the 2-D Poisson's equation for the potential distribution in cylindrical co-ordinates [15] is given by,

$$\frac{1}{r}\frac{\partial}{\partial r}\left(\frac{r\partial\varphi_i(r,z)}{\partial r}\right)+\frac{\partial^2\varphi_i(r,z)}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}} \quad (1)$$

i = 1,2,3

The potential profile in the vertical direction can be approximated by a simple parabolic function given by

$$\varphi(r,z)=C_0(z)+C_1(z)r+C_2(z)r^2 \quad (2)$$

where the coefficients C_0, C_1 and C_2 are functions of z only, and the Poisson's equation is solved separately for the three regions by considering the boundary conditions stated below:

The surface potential at the interfaces of the three dissimilar metals are continuous:

$$\varphi_1(r,L_1)=\varphi_2(r,L_1) \quad (3)$$

$$\varphi_2(r,L_1+L_2)=\varphi_3(r,L_1+L_2) \quad (4)$$

(ii) The electric field at the center of the channel is zero:

$$\left.\frac{\partial\varphi(r,z)}{\partial r}\right|_{r=0}=0 \quad (5)$$

(iii) The electric field at the S_i/S_iO_2 interface is continuous for both metal gates:

$$\left.\frac{\partial\varphi_i(r,z)}{\partial z}\right|_{r=R}=\frac{\varepsilon_{ox}}{\varepsilon_{si}R}\left[\frac{\psi_{G_i}-\varphi_i(r,z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right] \quad (6)$$

i = 1,2,3

where $\psi_{G_i}=V_{GS}-\varphi_{m_i}+\chi+\frac{E_g}{2}$ (7)

E_g is band gap energy (eV), q is electronic charge(coulombs), ε_{si} is permittivity of silicon, ε_{ox} is permittivity of gate oxide(S_iO_2), φ_{m_i} is the gate material work function.

(iv) The potential at the source end is:

$$\varphi(r=R,z=0)=V_{bis} \quad (8)$$

(v) The potential at the drain end is:

$$\varphi(r=R,z=L_1+L_2+L_3)=V_{bid}+V_{DS} \quad (9)$$

The built-in potential of drain and source regions are given as,

$$V_{bid}=\frac{KT}{q}\ln\frac{N_D}{n_i} \quad (10)$$

$$V_{bis}=-\frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (11)$$

where K is the Boltzmann constant, T is the temperature, and q is the electronic charge.

The differential equations for potential distribution are obtained by substituting the boundary conditions (3)-(9) in Eq. (2)

$$\frac{d^2\varphi_{s1}(z)}{dz^2}-\lambda\varphi_{s1}(z)=P_1,\quad 0\le z\le L_1 \quad (12)$$

$$\frac{d^2\varphi_{s3}(z)}{dz^2}-\lambda\varphi_{s2}(z)=P_2,\ L_1\le z\le L_1+L_2 \quad (13)$$

$$\frac{d^2\varphi_{s3}(z)}{dz^2}-\lambda\varphi_{s3}(z)=P_3,\ L_1+L_2\le z\le L_1+L_2+L_3 \quad (14)$$

where

$$\lambda^2=\frac{1}{R}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_{G_i}-\varphi_i(r,z)}{t'_{ox}} \quad (15)$$

$$P_i=\frac{qN_A}{\varepsilon_{si}}-\lambda^2\psi_{G_i},\ \text{i=1,2,3} \quad (16)$$

$$\text{R=t}_{si}/2;\ t'_{ox}=r\times\ln\left(1+\frac{t_{ox}}{R}\right) \quad (17)$$

The equations for surface potential for three regions are obtained as

$$\varphi_{S1}(z)=C_1e^{\lambda z}+D_1e^{-\lambda z}+\frac{P_1}{\lambda^2},\ 0\le z\le L_1 \quad (18)$$

$$\varphi_{S2}(z)=C_2e^{\lambda z}+D_2e^{-\lambda z}+\frac{P_2}{\lambda^2},\ L_1\le z\le L_1+L_2 \quad (19)$$

$$\varphi_{s3}(z)=C_3e^{\lambda z}+D_3e^{-\lambda z}+\frac{P_3}{\lambda^2}\ L_1+L_2\le z\le L_1+L_2+L_3 \quad (20)$$

Substituting the boundary conditions in (18), (19) and (20), the expressions are for the constants are obtained as

$$D_3=\left(\frac{\alpha P_3\left(2e^{\lambda\beta_5}-e^{\lambda(\beta_2+2L_3)}-e^{\lambda(3L_1+\beta_4)}-e^{\lambda L_2}\right)}{e^{\lambda L_2}\left(2-2e^{2\lambda\beta_5}+e^{\lambda\beta_4}\right)}\right)+\left(\frac{\alpha P_2(e^{\lambda(\beta_2+2L_3)}+e^{\lambda(3L_1+\beta_4)}+e^{\lambda L_2}-e^{\lambda(L_1+\beta_4)})}{e^{\lambda L_2}\left(2-2e^{2\lambda\beta_5}+e^{\lambda\beta_4}\right)}\right)+\left(\frac{\alpha P_1\left(e^{\lambda(L_1+\beta_4)}-2e^{\lambda\beta_5}\right)+2e^{\lambda\beta_5}V_{DS}}{e^{\lambda L_2}\left(2-2e^{2\lambda\beta_5}+e^{\lambda\beta_4}\right)}\right) \quad (21)$$

$$D_2=D_3e^{\lambda\beta_5}+e^{\lambda(-\beta_0-L_3)}P_2\mu-e^{\lambda(-\beta_0-L_3)}P_3\mu \quad (22)$$

$$D_1=\left(\frac{P_3\alpha\left(\frac{e^{\lambda\beta_3}}{2}-e^{\lambda L_1}+\frac{e^{\lambda\beta_2}}{2}\right)+P_2\alpha\left(e^{\lambda L}-\frac{e^{\lambda\beta L}}{2}-\frac{e^{\lambda\beta_3}}{2}\right)}{e^{\lambda L}\sinh\lambda L}\right)+\left(\frac{P_1\alpha\left(e^{\lambda\beta_1}+e^{\lambda L}\right)+D_3\left(e^{-\lambda L_3}-e^{\lambda\beta_4}\right)+V_{bid}e^{\lambda\beta_1}}{e^{\lambda L}\sinh\lambda L}\right) \quad (23)$$

$$C_1=V_{bis}+P_1\alpha-D_1 \quad (24)$$

$$C_2=e^{\lambda\beta_0}\left(\alpha\left(V_{bid}+V_{DS}+P_3\right)-D_3e^{-\lambda\beta_3}\right)+e^{\lambda(\beta_3-L)}P_2\mu-e^{\lambda(\beta_3-L)}P_3\mu \quad (25)$$

$$C_3=e^{-\lambda\beta_3}\alpha\left(V_{bid}+V_{DS}+P_3\right)-D_3e^{-2\lambda\beta_3} \quad (26)$$

where $\alpha=\frac{1}{\lambda^2};\quad \mu=\frac{\alpha}{2};\quad \beta_0=L_1-L;\quad \beta_1=L_1+L;$

$\beta_2=L_1+L_2;\quad \beta_3=L_1+L_3;\quad \beta_4=2(L_2+L_3)$

$\beta_5=L_1+L_2+L_3$

2. Electric Field

The electric field in TFET is vital to both the operation and reliability of the device. In this device, there are two electric field components namely lateral electric field(E_z) and vertical electric field(E_r). The gate voltage induced vertical field, and the drain voltage induced lateral field contributes the overall electric field. Due to work function engineering, the vertical electric field is altered and subsequently the overall electric field. Hence, the device performance is considerably improved.

By differentiating the surface potential obtained (18), (19) and (20), we get the electric field distribution along the channel length. The lateral electric field (E_z) is obtained as

$$E_{Z1}=\frac{\partial\varphi_{S1}(r,z)}{dz}=\lambda\left(C_1e^{\lambda Z}-D_1e^{-\lambda Z}\right)+\psi_{G_1},\ 0\le z\le L_1 \quad (27)$$

$$E_{Z2}=\frac{\partial\varphi_{S2}(r,z)}{dz}=\lambda\left(C_2e^{\lambda(Z-L_1)}-D_2e^{-\lambda(Z-L_1)}\right)+\psi_{G_2},\quad L_1\le z\le L_1+L_2 \quad (28)$$

$$E_{Z3}=\frac{\partial\varphi_{S3}(r,z)}{dz}=\lambda\left(C_3e^{\lambda(Z-L_2)}-D_3e^{-\lambda(Z-L_2)}\right)+\psi_{G_3},\quad L_1+L_2\le z\le L_1+L_2+L_3 \quad (29)$$

The vertical electric field is found to be

$$E_r=\frac{\partial\varphi(r,z)}{\partial r}=2C_2(z)r \quad (30)$$

$$C_2(z)=\frac{\varepsilon_{ox}}{2R\varepsilon_{si}}\frac{\psi_{G_i}-\varphi_i(r,z)}{\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (31)$$

3. Drain Current

The two electric field components contribute to the current generation [11]. The drain current I_D is based on the band to band tunneling of electrons and is obtained by the integration of the band to band generation rate G_{btbt} over the volume of the device [13].

$$I_D = q\int G_{btbt} dV \tag{32}$$

The tunneling generation rate G_{btbt} can be calculated using Kane's model [16].

$$G_{btbt} = A_{kane}\frac{|E|^2}{\sqrt{E_g}}\exp\left[\frac{-B_{kane}E_g^{\frac{3}{2}}}{|E|}\right] \tag{33}$$

where,

$$A_{kane} = \frac{q^2\sqrt{2m_{tunnel}}}{h^2\sqrt{E_g}} \tag{34}$$

$$B_{kane} = \frac{\pi^2 E_g^{\frac{3}{2}}\sqrt{\frac{m_{tunnel}}{2}}}{qh} \tag{35}$$

$$\frac{1}{m_{tunnel}} = \frac{1}{m_h m_o} + \frac{1}{m_e m_o} \tag{36}$$

$$|E| = \sqrt{E_r{}^2 + E_z{}^2} \tag{37}$$

Here $|E|$ is the magnitude of the electric field, E_r is the vertical electric field, E_z is the lateral electric field, E_g is the energy band gap, $m_o = 9.11\times10^{-31}$ kg, $m_h = 0.16\times m_o$ and $m_e = 0.98\times m_o$ [16].

IV. Results and Discussions

The accuracy of the analytical model is compared with the two-dimensional device simulation using the commercial technology computer aided design (TCAD Sentaurus) simulator [17]. Simulation conditions are summarized in Table 1. Calculated surface potential, lateral electric field, and vertical electric field and drain current are excellently matching with the simulated results. The investigated TMSGTFET exhibits improved electrical characteristics.

Table 1. Model Parameters

Parameters	Symbol	Value
Source Doping	N_A	10^{20} cm^{-3}
Drain Doping	N_D	5×10^{18} cm^{-3}
Channel Doping	n_i	10^{10} cm^{-3}
Silicon Body thickness	t_{si}	10 nm
Gate Oxide thickness	t_{ox}	3 nm
Channel Length	L	90 nm
Metal Work Function	$\Phi_{M1}, \Phi_{M2}, \Phi_{M3}$	4 – 4.8 eV

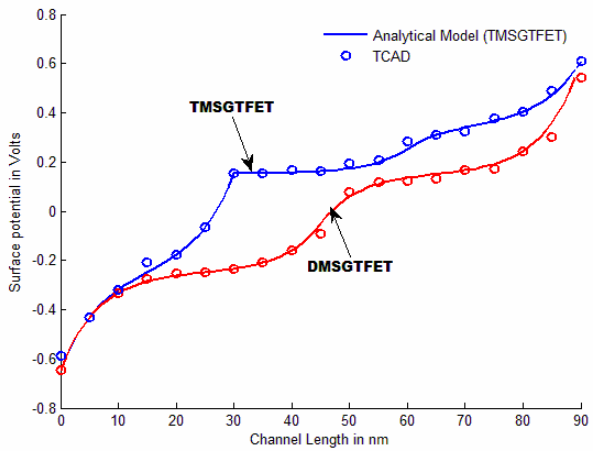


Fig. 2. Surface potential profiles of TMSGTFET(proposed device) and DMSGTFET with V_{GS} = 0.3 V and V_{DS} = 0.1 V. Simulation results are also shown.

Fig. 2 shows both calculated surface potential profile and simulated surface potential profile of the proposed structure in comparison with the dual material surrounding gate TFET with V_{DS} = 0.1 V and V_{GS} = 0.3 V. The potential varies near or across the junctions, but it is constant in the middle of the silicon body. There are two step changes in the potential profile of TMSGTFET along the channel at the interface of metal M_1 and M_2 & M_2 and M_3, which reveals the reduced drain control over the channel. The short channel effects are thus suppressed more noticeably than the DMSGTFET as evident from the figure.

Fig. 3 shows the variation of surface potential profile for various ratios of $L_1 : L_2 : L_3$ along the channel with V_{DS} = 0.1 V and V_{GS} = 0.3 V. There is a shift in the step profile proportionally to the changes in the length ratio, at the interface of metal M_1 and M_2 & M_2 and M_3. The potential changes near or across the junctions and constant in the middle of the silicon body. A good agreement is seen between the calculated results and

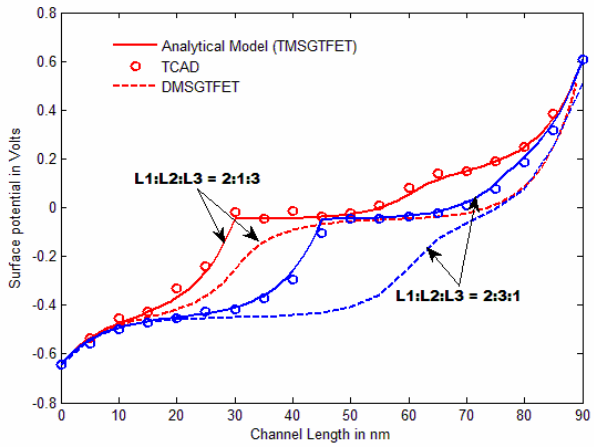


Fig. 3. Surface potential distribution of TMSGTFET for different ratios of length with V_{DS} = 0.1 V and V_{GS} = 0.3 V. It is compared with DMSGTFET. TCAD Simulation results are also shown.

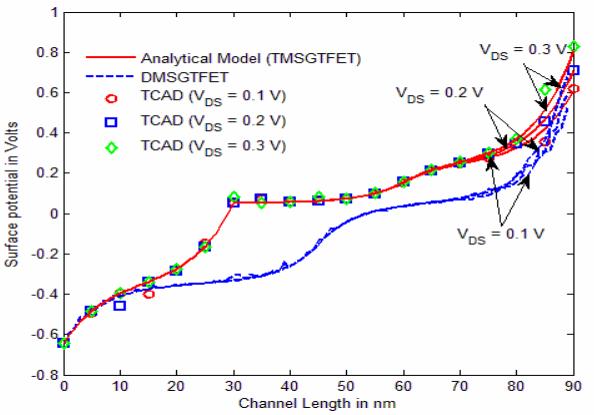


Fig. 4. Variations in Surface potential profile with V_{GS} = 0.1 V for different values of drain bias. The model of TMSGTFET is compared with DMSGTFET. TCAD Simulation results are also shown.

simulated results. The proposed Triple Material SGTFET is compared with Dual Material SGTFET for which the length ratios are taken as 2:1 and 1:2.It is evident that our proposed structure shows improved performance.

Fig. 4 shows the simulated and calculated surface potential for various values of V_{DS}. The impact of drain bias contributes to the lowering of barrier width of the tunnel junction. It is clearly seen that as the drain voltage increases, the potential near the drain end increases appreciably, and there is no notable change near the source end. Thus, it is concluded that the drain voltage has very little impact on the tunneling generation rate at the source end and reduces the drain induced barrier lowering effects of the device that is evident from the

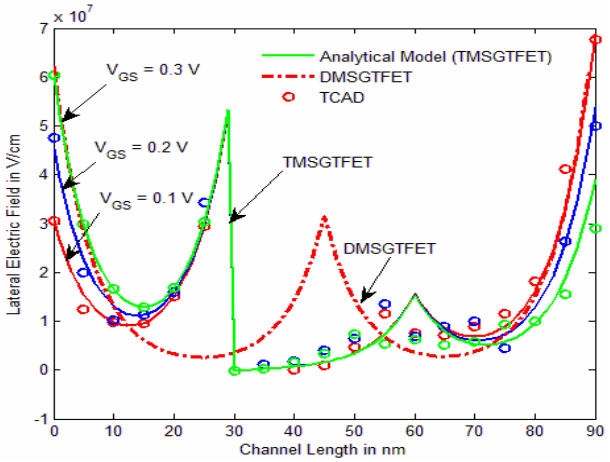


Fig. 5. Lateral Electric Field for V_{DS} = 0.1 V with different gate biases. It is compared with DMSGTFET. Simulation results are also shown.

two step up in the potential profile seen in figure. A good degree of analogy is achieved between simulated and calculated results. The comparison results ensure the enhanced performance of our proposed structure.

Fig. 5 shows the calculated and simulated lateral electric field distribution for various values of gate voltages. It is also compared with the DMSGTFET. The electric field is vital to both the operation and reliability of the device. When the device is ON, the variations in the potential are concentrated near the tunneling junction and hence the peak electric field appears at this point. The drain to source bias contributes to the lateral electric field distribution. Increase in V_{DS} causes a prominent rise in the lateral electric field and thus decreases the gate control over the channel. The agreement between the analytical results and the simulated results is good.

Fig. 6 shows the variations in vertical field distribution for variations in drain to source bias. It is evident from the figure that high drain voltage does not cause the change in the source field under metal M_1. Also, the peak electric field is low at the drain end, which can be understood as minimized hot carrier effect at the drain end. The validity of the proposed model is assured by the simulation results.

Fig. 7 depicts the vertical electric field distribution along the channel length for different gate biases. The gate bias affects the potential in the silicon body, thus increasing the field across the tunneling junction. The vertical field component(E_r) is responsible for the tunneling probability and hence drive current. The gate to

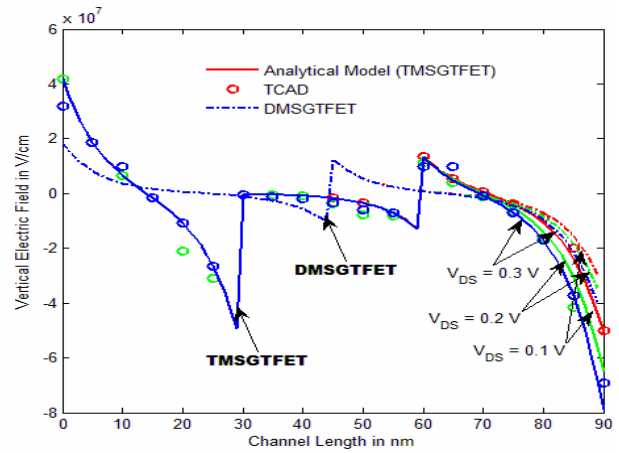


Fig. 6. Vertical Electric Field with V_{GS} = 0.2 V for different drain biases. Comparison with DMSGTFET and simulation results are shown.

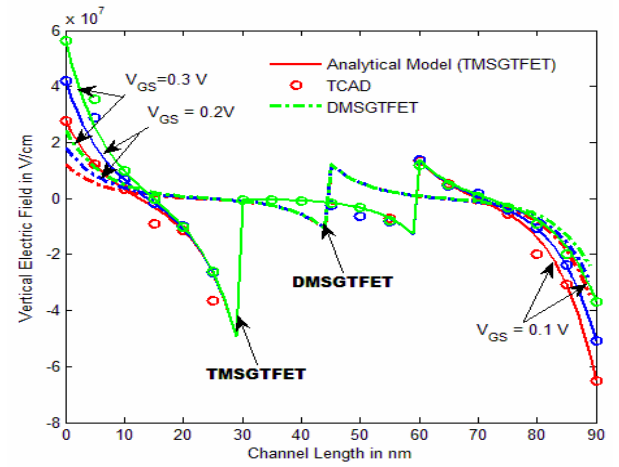


Fig. 7. Vertical Electric Field with V_{DS} = 0.1 V for various gate biases. Simulation results are shown. The model is compared with DMSGTFET.

source voltage contributes the vertical electric field of the device. A high vertical electric field is induced at the source to channel junction as the voltage applied in the gate increases. The figure shows stronger peak at the tunneling junction. Hence, maximum vertical electric field is present at the tunneling junction always, which results in minimum tunneling barrier width between the source and the intrinsic channel. This in turn yields higher ON current. However, both the components of the electric field(E_z and E_r) contributes to the current generation, as they have similar values at the junction edge. The comparison results between TMSGTFET and DMSGTFET are also shown.

The vertical field distribution of the proposed structure

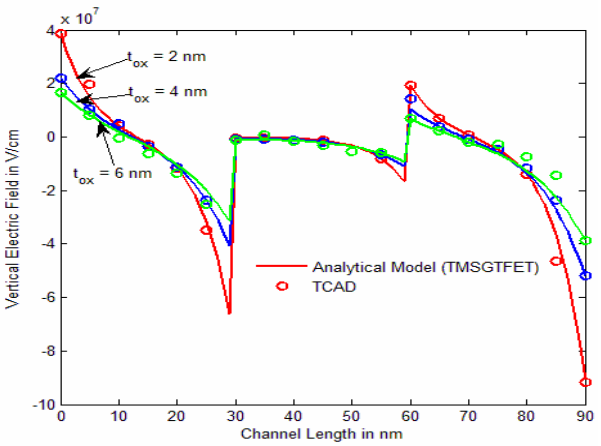


Fig. 8. Vertical Electric Field distribution (E_r) for different gate oxide thickness t_{ox} with V_{DS} = 0.1 V.

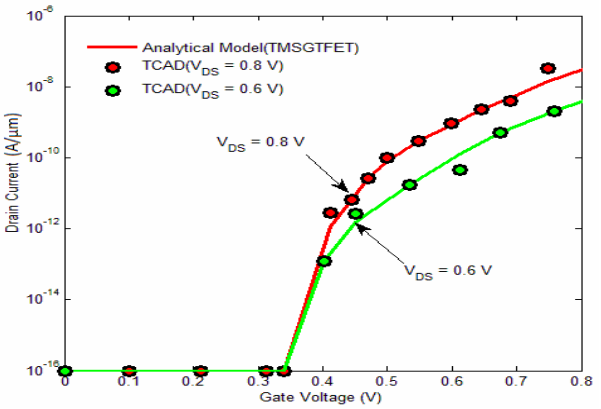


Fig. 9. Transfer characteristics of TMSGTFET for different values of V_{DS} = 0.6 V, 0.8 V.

has been plotted in Fig. 8 for various values of gate oxide thickness(t_{ox}). It can be observed from the figure that the vertical electric field can be increased by decreasing the thickness of the gate oxide. But, however scaling of t_{ox} has its physical limit for desirable characteristics. Fig. 9 shows the calculated and simulated values of drain current for various gate biases with V_{DS} = 0.6 V and 0.8 V. With the positive gate voltage, the energy bands in the intrinsic region are pushed down and the tunneling occurs between the valence band of the p+ region and the conduction band of the intrinsic region. A very high electric field is created, resulting in high I_{ON}. The device behaves as a p-type TFET for negative values of gate voltage. The energy bands in the intrinsic region beneath the gate are lifted and band to band tunneling takes place between the valence band of the intrinsic region and conduction band of the n+ region. The figure depicts that leakage current is significantly lowered and it is evidence

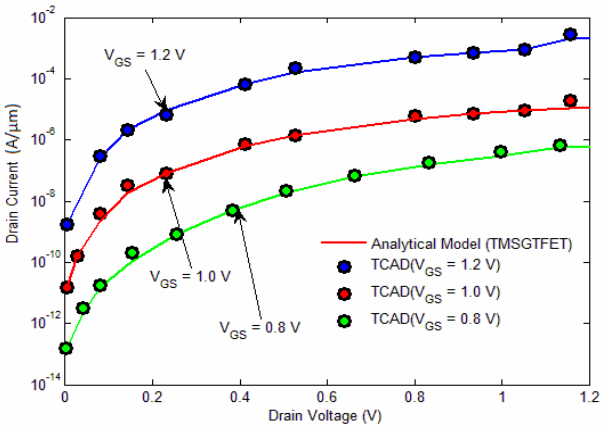


Fig. 10. I_D vs V_{DS} characteristics of TMSGTFET for different values of V_{GS} = 0.8 V, 1.0 V, 1.2 V.

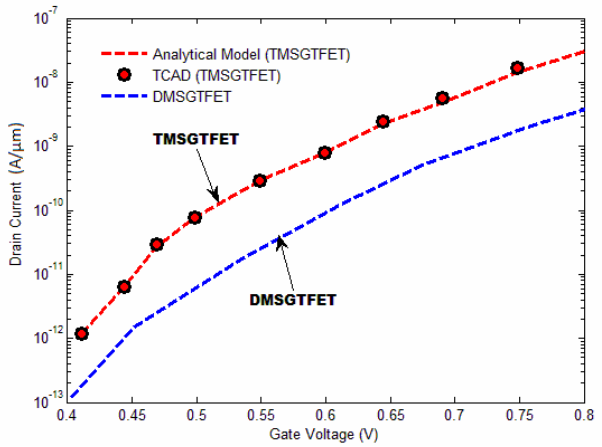


Fig. 11. Log I_D vs V_{GS} characteristics of TMSGTFET for V_{DS} = 0.8 V. Comparison results with DMSGTFET and simulation results are shown.

for suppression of SCE.

Fig. 10 shows the I_D vs V_{DS} characteristics of TMSGTFET for V_{GS} = 0.8 V, 1.0 V and 1.2 V. When V_{DS} is increased, a larger drain voltage exists at the tunneling junction and causes barrier lowering. The channel resistance becomes high and drain potential has no impact on tunneling barrier width at the source side. This results in saturation of drain current. Fig. 11 compares the drain current of the proposed device with the drain current of DMSGTFET. Due to different gate material work functions, the vertical electric field is improved. Also, the use of relatively low work function material in the source side results in narrowing the tunneling width which improves the ON current. The results predicted by the model are in excellent agreement with the simulation results.

V. Conclusion

In this paper, 2-D analytical model has been developed for TMSGTFET using parabolic approximation technique. Analytical expressions have been derived for surface potential, lateral electric field vertical electric field and drain current.The drain current is numerically extracted using both lateral and vertical electric field. The calculated results have been compared with the simulation results which show an appreciable level of agreement. This new structure undoubtedly predicts the improved control of the gate and exhibits remarkable characteristics depicting the reduced SCEs. Also, it shows an improved drain current than its TFET counterparts due to work function engineering.

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