Voltage Optimization of Power Delivery Networks through Power Bump and TSV Placement in 3D ICs

Cheoljon Jang and Jong-wha Chong

To reduce interconnect delay and power consumption while improving chip performance, a three-dimensional integrated circuit (3D IC) has been developed with die-stacking and through-silicon via (TSV) techniques. The power supply problem is one of the essential challenges in 3D IC design because IR-drop caused by insufficient supply voltage in a 3D chip reduces the chip performance. In particular, power bumps and TSVs are placed to minimize IR-drop in a 3D power delivery network. In this paper, we propose a design methodology for 3D power delivery networks to minimize the number of power bumps and TSVs with optimum mesh structure and distribute voltage variation more uniformly by shifting the locations of power bumps and TSVs while satisfying IR-drop constraint. Simulation results show that our method can reduce the voltage variation by 29.7% on average while reducing the number of power bumps and TSVs by 76.2% and 15.4%, respectively.

Keywords: Three-dimensional integrated circuit, power delivery network, through-silicon via, VLSI.

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Cheoljon Jang (jangcj@hanyang.ac.kr) is with the Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul, Rep. of Korea.

Jong-wha Chong (corresponding author, jchong@hanyang.ac.kr) is with the Department of Electronics Computer Engineering, Hanyang University, Seoul, Rep. of Korea.

I. Introduction

To overcome the physical limitations of semiconductor fabrication and to improve integration consistently according to Moore's law [1], three-dimensional integrated circuits (3D ICs), which expand the concept of multi-chip modules into the vertical direction, have recently gained popularity [2]. In 3D ICs, dies are piled up vertically in the same stack, and the components on different dies are connected with through-silicon via (TSV) [3]. 3D ICs provide a smaller footprint, shorter interconnect delay, lower power consumption, and improved total chip performance [4]. However, 3D implementation increases power density, which causes various challenges, including thermal problems [5], routing congestion [6], and power supply problems [7]. Among these challenges, power delivery network synthesis for adequate power supply is perceived as one of the most important issues. If power is inadequate in the power delivery network, then an IR-drop occurs, hence, degrading the chip's performance [8]. The power delivery network in a 3D IC places power bumps and TSVs near the high-activity area of the chip to minimize IR-drop [9]. It is very difficult to supply power to all parts of the integrated circuits stacked in 3D using power bumps and TSVs without IR-drop occurring. Moreover, to prevent both the overlap of standard cells and wire congestion, the number of power TSVs in a 3D power delivery network must be limited [10]. In addition, the alignment of power bumps has an impact on the quality of a 3D power delivery network [11].

Many techniques have been developed to solve the IR-drop problem in a 3D power delivery network. In [10], the number

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and location of power TSVs placed on the fixed mesh structure are optimized. In [12], the power TSVs are spread evenly throughout the die. Power TSV placement methodologies such as [10] and [12] assume that power bumps are located in regular array to solve the IR-drop constraint in 3D ICs. Because the number of power bumps placed in regular array in the early stage of the algorithm is too high, the number of clock bumps and signal bumps is limited. In addition, because these methodologies solve the IR-drop problem at the placement stage, when the IR-drop constraint is not satisfied and inserted power TSVs overlap with gates, for redesign, the methodologies should return to the early stages, which makes the design cost too high. In our previous work, [13] proposed a methodology to minimize the number and optimize the location of both power bumps and TSVs simultaneously to solve the IR-drop problem that may occur in the power delivery network at the floorplan stage of a 3D IC. The aforementioned methods are suitable to analyze a power delivery network only when it has a fixed mesh structure. Otherwise, the circuit topology changes, case by case, based on the circuits when optimizing the number and location of power bumps and TSVs, which causes considerable overhead. To solve this problem, another of our previous works [14] proposed a methodology to minimize the number and optimize the location of both power bumps and TSVs simultaneously to solve the IR-drop constraint with the optimum power mesh structure in a 3D power delivery network. However, because both previous methods do not consider voltage variation between the nodes in power delivery networks, severe voltage differences on the chip occur, which can degrade the entire system performance. Also, these two previous works have the limitation that they target two-die stacked power delivery networks with uniform mesh grids in which the grids on all dies are the same. To solve these problems, a design methodology for 3D power delivery networks is needed to minimize the number of power bumps and TSVs with non-uniform mesh grids and distribute IR-drop more evenly across the entire system while satisfying IR-drop constraints in a 3D chip.

In this paper, we propose a 3D power delivery network design methodology to synthesize a 3D power delivery network with more than two stacked dies at the floorplan stage that minimizes the number of power bumps and TSVs (using an optimum non-uniform mesh structure to satisfy IR-drop constraints) and shifts the locations of power bumps and TSVs to distribute the IR-drop more evenly while satisfying IR-drop at every node. Because of its optimized mesh structure usage, our proposed algorithm can further reduce the number of power bumps and TSVs to satisfy the IR-drop constraint. In addition, while satisfying IR-drop at every node, our algorithm moves the location of inserted power bumps or TSVs, lowers the worst IR-drop, and makes the voltage variation more even throughout the entire power delivery network; thus, it can prevent the degradation of the entire system performance.

II. Background

As shown in Fig. 1, the power bump is inserted on Die 1, the lowest die, and supplies power to the power delivery network in a 3D IC. The power TSV connects between the dies vertically and delivers power to the upper dies. The TSV is a vertical via passed completely through silicon dies. The main purpose of the TSV is to establish electrical connections between devices on two different dies in the 3D IC stack.

For the ground network, a ground TSV and a power TSV are inserted as a pair [15], and the analysis process for the ground TSV is the same as for the power TSV. Therefore, in this paper, we describe only the 3D power delivery network.

As shown in Fig. 2, each die of the 3D power delivery network consists of a mesh structure, which is a set of stripes with pitch and width defined on two or more layers [9]. From

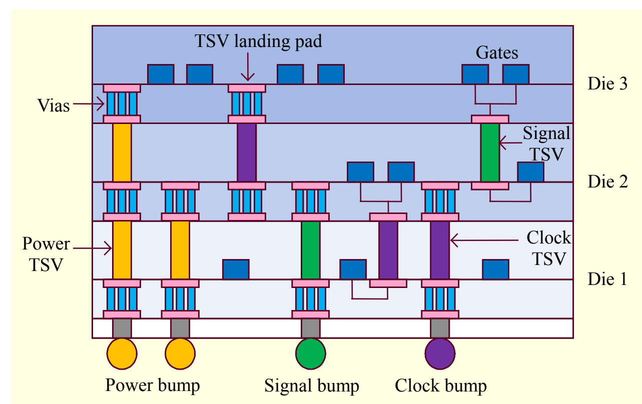

Fig. 1. 3D IC structure with bumps and TSVs.

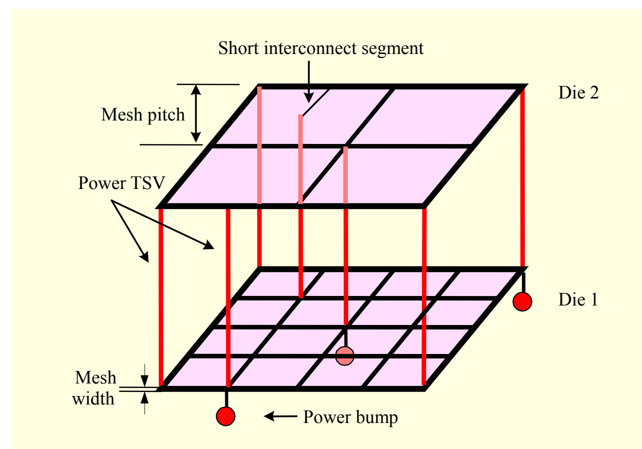

Fig. 2. 3D power delivery network.

now on, for simplicity, we describe the figures for the 3D power delivery network in this paper as 2 die-stacked 3D IC. In the mesh structure of a 3D power delivery network, the mesh pitch indicates the gap between the power wires, and the mesh width indicates the thickness of each power wire. The range of mesh pitch and mesh width in a mesh structure is determined by layout design rules. There are normally two types of mesh topology in a 3D power delivery network: a uniform mesh grid, in which the mesh pitches of the grids on all dies are the same; and a non-uniform mesh grid, in which each die has different mesh pitches. The previous works on 3D power networks, [13] and [14], restrict the uniform mesh grid by restricting the insertion of power TSVs to only the locations of the nodes on the mesh grid between power delivery networks on two adjacent dies. However, 3D integration can be implemented of dissimilar meshes because of heterogeneity. Therefore, in this paper, each die has a non-uniform mesh structure for the 3D power delivery network. When the location of an inserted power TSV is not at a cross point of one of the power delivery networks on two adjacent dies, a short interconnect segment is needed to connect it to the mesh wire, as can be seen in Fig. 2.

At each node in a power delivery network, blocks consume current and IR-drop occurs. The more the blocks consume current, the more severe the IR-drop that occurs. When IR-drop occurs dramatically in the power delivery network, blocks on the chip cannot operate properly. In general, the IR-drop constraint is determined as a voltage less than 5% of the initial supply voltage in a power delivery network [16]. If the voltage supplied to each node in the power delivery network is less than 5% of the initial supply voltage, blocks near the node cannot work properly and chip performance is degraded. Some papers refer to IR-drop as 10% of initial supply voltage. This means that the supply can drop by 5% of the initial supply voltage and the ground can bounce by 5% as well [9].

Metal coverage is defined by considering the mesh structure in a power delivery network, as shown in Fig. 3. The percentage of metal coverage is defined as follows:

$$\%Cov = \frac{A_{\text{Power}}}{A_{\text{Chip}}}, \quad (1)$$

where A_{Power} represents the area of power wire metal, A_{Chip} represents chip area, and $\%Cov$ represents the percentage of metal coverage [17]. In Fig. 3, the metal coverage can be found by subtracting the clear area without mesh wire from the area of the mesh element shown by the hash lines. Metal coverage, including signal wire and clock wire, is one important factor for determining routing congestion. Power wires commonly use 20% to 40% of all metal resources on a chip [9]. A power delivery network should have a metal coverage within a given range while satisfying IR-drop constraint. A higher percentage

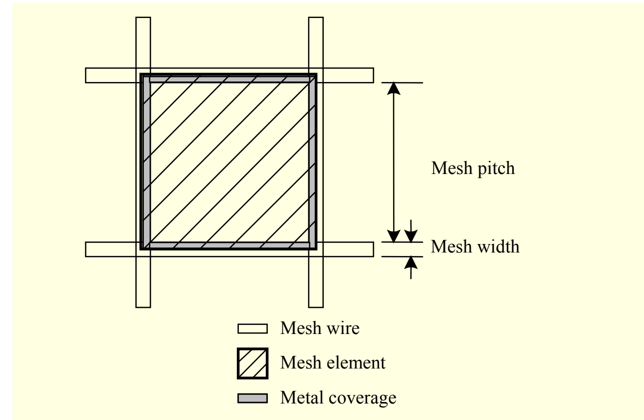

Fig. 3. Metal coverage in a mesh structure.

of metal coverage enables the power network to supply more power to the chip; however, routing congestion increases and chip performance may be degraded because of insufficient signal wire and clock wire. Hence, the IR-drop problem should be solved under power-optimized routing resources.

III. Proposed Algorithm

1. Overview: Overall Flow

The proposed 3D power delivery network design methodology is shown in Fig. 4.

The following explains the flow of the proposed algorithm and each of its steps.

2. Flows of the Proposed Algorithm

A. Step 0. Determine Optimum Mesh Structure

In the previous work [13], power bumps and TSVs are inserted to a 3D power delivery network with a fixed mesh structure to satisfy IR-drop constraint. Generally, when the

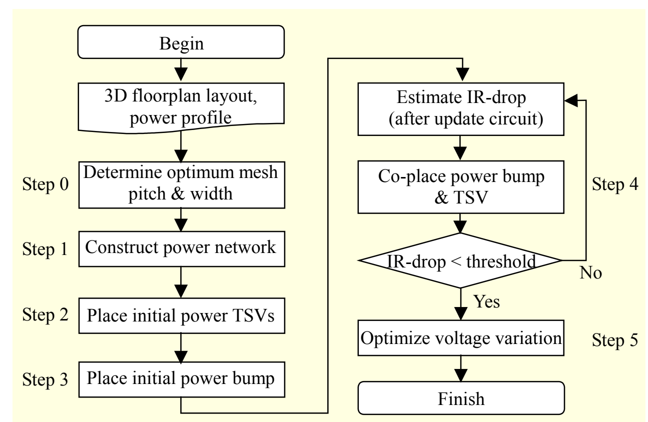

Fig. 4. Flow chart for proposed 3D power delivery network design methodology.

mesh width increases in a power delivery network, both its resistance and its IR-drop decrease [18]. Similarly, when the mesh pitch decreases in a power delivery network, the number of power bumps and TSVs needed to satisfy the IR-drop constraint decreases on account of adequate power supply on each node of the power delivery network. However, because the routing area and routing resources are limited, the ranges of the mesh pitch and mesh width are restricted under the condition of unchanged metal coverage. A saturation point happens where the number of power bumps and TSVs can no longer be reduced despite changes in the mesh pitch and mesh width. As a result of this, the other previous work [14] determines the optimum mesh pitch and mesh width to minimize the number of power bumps and TSVs needed to satisfy the IR-drop constraint.

The detailed steps for determining optimum mesh pitch and mesh width in a 3D power delivery network are as follows:

1. Step 0.1. Under the range of limited metal coverage, mesh pitch and mesh width increase independently from minimum value to maximum value as determined by the layout design rules for each die, as shown in Fig. 5.
2. Step 0.2. Assign virtual power bumps at the four corner-nodes of the lowest die, Die 1, to supply the same minimum voltage to the power delivery network even if the number of nodes increases with the various mesh pitches and widths.
3. Step 0.3. Assign virtual power TSVs at the four corner-nodes of the power delivery network for the purpose of basic connection between the dies without the effect of routing resources inside the core region.
4. Step 0.4. After assigning the virtual power bumps and TSVs as illustrated in Fig. 6, estimate the IR-drop.
5. Step 0.5. Assign additional virtual power bumps or TSVs to the location of the worst IR-drop until every node satisfies the IR-drop constraints.
6. Step 0.6. Repeat steps 0.1–0.5, and determine the value of the mesh pitch and mesh width that results in the minimum number of virtual power bumps and TSVs to satisfy the IR-drop constraint.

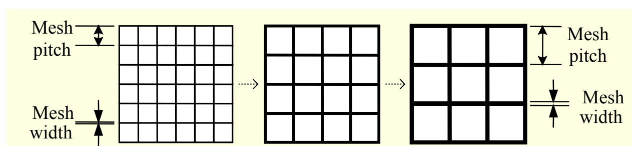

Fig. 5. Sizes of mesh pitch and mesh width in a power delivery network.

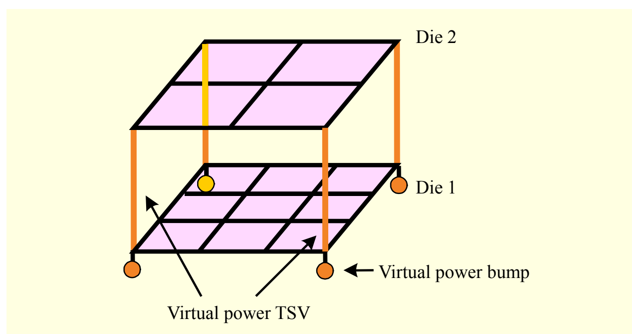

Fig. 6. Assignment of virtual power bumps and TSVs.

B. Step 1. Construct Power Delivery Network

The 3D power delivery network is constructed with the mesh pitch and mesh width determined by the optimum mesh structure.

C. Step 2. Place Initial Power TSVs

To construct the initial 3D power delivery network, the initial power TSVs and bump are placed so as to provide the absolute minimum required power. As shown in Fig. 7(a), initial power TSVs are placed at the four corner nodes of the 3D power delivery network to supply power to the upper dies for a bare-minimum connection. These TSVs, which are placed at the four corner nodes, do not affect the routing resources inside the core region.

D. Step 3. Place Initial Power Bump

As shown in Fig. 7(b), virtual power bumps are placed at each candidate node on Die 1. Then the IR-drop is estimated at each candidate node on each die. The candidate nodes for the placement of power bumps are all intersection points where vertical and horizontal power wires meet. Initially, virtual power bumps are placed at each intersection point of Die 1. The node with the lowest voltage is then identified and an initial power bump is then inserted at the node, as shown in Fig. 7(c). All virtual power bumps are then removed. The location of the node with the lowest voltage among the nodes on Die 1, means the location where the power supply is most needed.

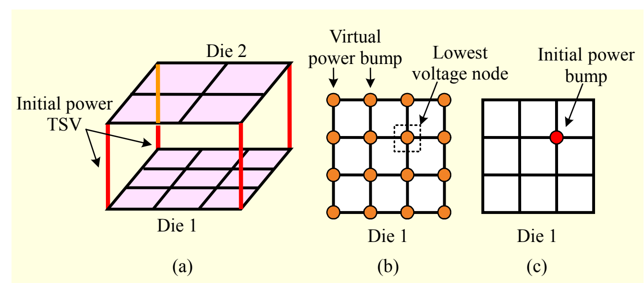

Fig. 7. Initial power delivery network: (a) Initial power TSVs assignment, (b) virtual power bumps, and (c) initial power bump assignment.

Fig. 8. 3D power grid circuit model.

E. Estimate IR-Drop

After placing the initial power bump and TSVs, the IR-drop is estimated for each node on all dies. In this paper, we assume a steady-state power grid that can be solved by DC analysis. The IR-drop estimation can be calculated by a circuit model corresponding to the 3D power grid, which is modified from [19]. A 3D power grid circuit model is illustrated in Fig. 8.

Then the DC analysis problem can be formulated as a linear system

$$\mathbf{A}\boldsymbol{x} = \boldsymbol{b}, \tag{2}$$

where $\mathbf{A}$ is a conductance matrix for interconnected resistances, $\boldsymbol{x}$ is a vector of node voltages, and $\boldsymbol{b}$ is a vector of independent sources. If the power grid has N rows, N columns, and k dies, then the total number of nodes is kN^2.

Two notation methods can be used to describe a node. In the first method, we use the coordinates of the node: A node at the ith row, jth column, and kth die is defined as (i, j, k). The other method is to number all nodes from 1 through to kN^2. Then node (i, j, k) can be written as $i\cdot N+j+(k-1)\cdot N^2$.

The matrix $\mathbf{A}$ in (2) can be expressed as:

$$\mathbf{A} = \begin{bmatrix} \mathbf{A}_{111} & \mathbf{D}_{11} & & & \mathbf{T}_{11} & & & \\ \mathbf{D}_{11} & \mathbf{A}_{221} & & & & \mathbf{T}_{21} & & \\ & \ddots & \ddots & \mathbf{D}_{(N-1)1} & & & \ddots & \\ & \ddots & \mathbf{D}_{(N-1)1} & \mathbf{A}_{NN1} & & & & \mathbf{T}_{N1} \\ \mathbf{T}_{11} & & & & \mathbf{A}_{112} & \mathbf{D}_{12} & & \\ & \mathbf{T}_{21} & & & \mathbf{D}_{12} & \mathbf{A}_{222} & \ddots & \\ & & \ddots & & & \ddots & \ddots & \mathbf{D}_{(N-1)2} \\ & & & \mathbf{T}_{N1} & & & \mathbf{D}_{(N-1)2} & \mathbf{A}_{NN2} \end{bmatrix}, \tag{3}$$

where

$$\mathbf{A}_{iik} = \begin{bmatrix} G_{(i,1,k)} & -g_{(i,1,k)(i,2,k)} & & \\ -g_{(i,2,k)(i,1,k)} & G_{(i,2,k)} & -g_{(i,2,k)(i,3,k)} & \\ & \ddots & \ddots & \ddots \\ & & -g_{(i,N,k)(i,N-1,k)} & G_{(i,N,k)} \end{bmatrix}, \tag{4}$$

$$\mathbf{D}_{ik} = \begin{bmatrix} -g_{(i,1,k)(i+1,1,k)} & & & \\ & -g_{(i,2,k)(i+1,2,k)} & & \\ & & \ddots & \\ & & & -g_{(i,N,k)(i+1,N,k)} \end{bmatrix}, \tag{5}$$

$$\mathbf{T}_{ik} = \begin{bmatrix} -g_{(i,1,k)(i,1,k+1)} & & & \\ & -g_{(i,2,k)(i,2,k+1)} & & \\ & & \ddots & \\ & & & -g_{(i,N,k)(i,N,k+1)} \end{bmatrix}, \tag{6}$$

where the interconnection between the nodes on the same ith row is represented by $\mathbf{A}_{iik}$, the connection between the nodes on the ith row and $(i+1)$th row at the same kth die is represented by $\mathbf{D}_{ik}$, and the TSV connection between node (i, j, k) and node $(i, j, k+1)$ is represented by $\mathbf{T}_{ik}$. The conductance between two neighboring nodes (i, j, k) and (l, m, n) is defined as $g_{(i,j,k)(l,m,n)}$.

$G_{(i,j,k)}$ can also be expressed as

$$G_{(i,j,k)} = \sum_{(l,m,n)\in N_{(i,j,k)}} |\, g_{(i,j,k)(l,m,n)} \,|, \tag{7}$$

where $N_{(i,j,k)} = \{(l,m,n) \mid g_{(i,j,k)(l,m,n)} \neq 0\}$ with the node (l, m, n) representing the neighbor of node (i, j, k). Because it is made up of horizontal and vertical straight lines, the power grid forms a rectangular network. The empty space shown in the matrices of (3)–(6) indicates zeroes. In particular, in the case of (6), the empty space also indicates a node without a TSV connection.

Source vector $\boldsymbol{b}$ can be expressed as

$$\boldsymbol{b} = \begin{bmatrix} \boldsymbol{b}_{11} \\ \boldsymbol{b}_{21} \\ \vdots \\ \boldsymbol{b}_{N1} \\ \boldsymbol{b}_{12} \\ \boldsymbol{b}_{22} \\ \vdots \\ \boldsymbol{b}_{N2} \end{bmatrix}, \quad \boldsymbol{b}_{ik} = \begin{bmatrix} -I_{(i,1,k)} \\ -I_{(i,2,k)} \\ \vdots \\ -I_{(i,N,k)} \end{bmatrix}, \tag{8}$$

where $I_{(i,j,k)}$ represents the current drain at node (i, j, k).

F. Step 4. Co-place Additional Power Bumps and TSVs and Satisfy IR-Drop Constraint

After estimating the IR-drop, we find the worst IR-drop node from among all nodes in all dies. As in Fig. 9(a), if the worst IR-drop node is found on Die 1, the lowest die, then a power bump is placed at the location of the worst IR-drop node on Die 1 and supplies additional power. Otherwise, if the worst IR-drop node is not found on Die 1, as in Fig. 9(b), then a power bump and TSV are placed at the location of the worst

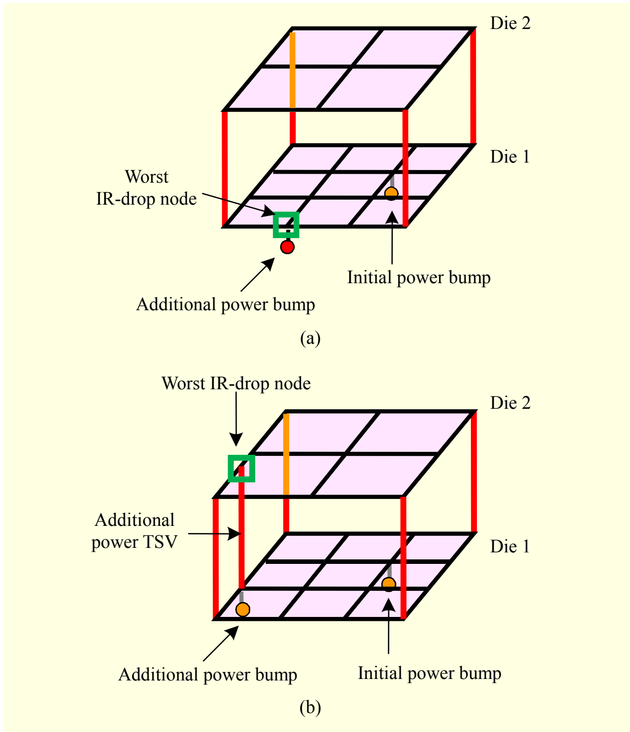

Fig. 9. Additional power bump and TSV placement.

IR-drop node, thus supplying additional power to the upper die. After placing an additional power bump or TSV, the IR-drop is re-estimated. If any node fails to satisfy the IR-drop constraint, another power bump or TSV is placed additionally at the worst IR-drop node in the same way. This step is repeated until every node on all dies satisfies the IR-drop constraints.

G. Step 5. Minimize Voltage Variation

At this step, the minimum voltage on the power delivery network is improved and the IR-drop variation of the whole power grid is distributed more evenly by the moving of power bumps and TSVs to their optimum location, without changing their number, to satisfy the IR-drop constraints in the 3D power delivery network.

An example of the power bump and power TSV candidate node locations in a power delivery network is shown in Fig. 10. The nodes with red circles represent the initially placed power bump and TSVs, while the nodes with white circles represent the candidate nodes for further additional power bumps and TSVs.

After a power bump or TSV near the minimum voltage node moves to the minimum voltage node among other candidate nodes, the values of voltages in the power grid are recalculated. A fast and efficient technique for recalculating voltage after the relocation of a power bump, is proposed in [20]. We modified the technique in [20] to recalculate voltage after the movement of both a power bump and a power TSV. The cost function for

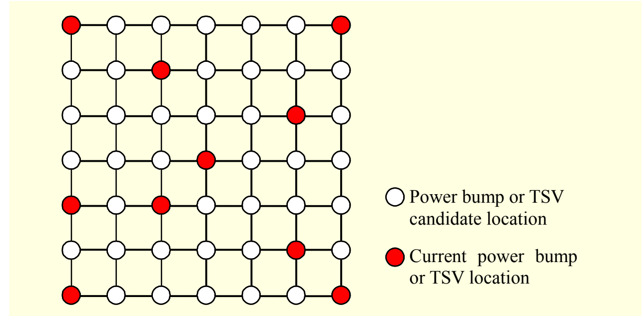

Fig. 10. Example: the locations of power bump and TSV candidate nodes.

increasing the minimum voltage in the power grid and also distributing IR-drop more evenly in the whole power grid can be expressed as

$$Cost(V) = \alpha(V_{\text{supply}} - V_{\text{worst}})^2 + \beta\sqrt{\frac{\sum_i^N (V_i - V_m)^2}{N}}, \quad (9)$$

where V_{supply} represents the supply voltage, V_{worst} represents the minimum voltage among all nodes, V_i represents the voltage of node i, V_m represents the average voltage of the nodes, and N represents the number of nodes. The constants α and β are bound on the cost function that control the tradeoff between the minimum voltage and the standard deviation of the voltages. Using $(V_{\text{supply}}-V_{\text{worst}})^2$ instead of $(V_{\text{supply}}-V_{\text{worst}})$ has both the advantage of making the cost function more sensitive to the voltage and of having a greater effect on decreasing the IR-drop. The voltage on each die is changed after the movement of power bumps and TSVs.

To minimize the voltage variation in the power grid, we find the minimum voltage node. Afterward, we calculate the force to move a power bump or TSV from a neighbor node to the minimum voltage node, and then shift the power bump or TSV to the minimum voltage node with the smallest cost function value. A smaller cost function value means that the minimum voltage and the voltage variation are improved; hence, the voltages on the network have a more balanced distribution. Thus, we permit this shift in the case of a decreased cost-function value and recalculate the voltage value at each node over the whole power grid. We repeat the movement process of power bumps or TSVs until the cost function value increases more than before.

In general, a power bump or TSV at a node x has an influence on the voltage of neighbor node a $\in N_x$, where N_x is a set of nodes near the node x including the nodes on different dies. Then, the power bumps or TSVs at the nodes of N_x have an effect on the voltage of neighbor node b $\in N_a$ sequentially. In other words, the voltage at node x spreads out like a wave until it affects every node in the power grid, as shown in Fig. 11.

We use a force-directed algorithm to both decrease IR-drop

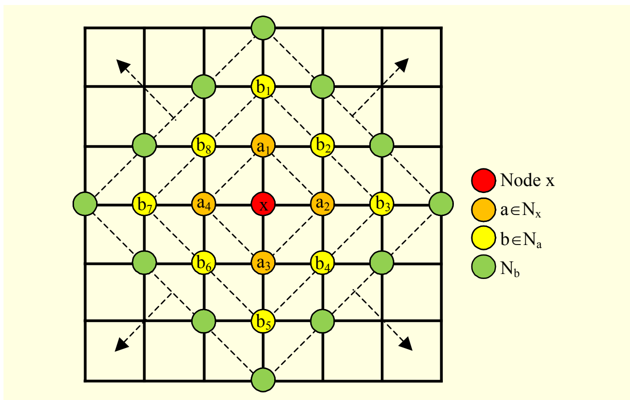

Fig. 11. Propagation illustration for calculating force at node x.

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Algorithm. Force-Directed Based Power Bump and TSV Optimization Algorithm
minimized_power_bump_and_TSV_placement()
i = 0 // iteration number
REPEAT // begin iteration
  i = i + 1
  // store all power bump and TSV location
  current_solution = store_current_solution()
  FOR each die from bottom-most die
    FOR each power bump and TSV node N
      node_force = (0, 0) // sum of total force on this node
      FOR each neighbor candidate nodes
        node_force = node_force + calculate_force(this_node, other_node)
      END FOR
      compute_approximate_new_location()
    END FOR
    // shift all power bump or TSV nodes by each force
    shift_nodes()
    update_voltage_map()
   END FOR
   previous_cost = current_cost
   current_cost = calculate_cost()
  UNTIL (i > max_iteration) || (current_cost > previous_cost)
END REPEAT
 RETURN current_solution
```

Fig. 12. Pseudocode of force-directed based algorithm.

at the nodes and minimize voltage variation in the power grid. The proposed force-directed-based algorithm is shown as Fig. 12.

IV. Simulation Results

Our proposed 3D power delivery network design methodology has been implemented in the C++/STL programming language. The simulations are performed on a 64 bit Ubuntu Linux PC with 3 GHz CPU and 4 GB memory. Four MCNC benchmarks are used for simulation [21], and the four circuits listed in Table 1 are assumed to be a 4-die stacked 3D IC. We modified 3DFP [22] and Parquet [23] to result in a 4-die stacked 3D floorplan. 3DFP is a thermal-aware floorplanner for the design of 3D ICs with multiple layers, and

Table 1. MCNC benchmark circuits.

Circuit	Area (μm × μm)	Die 1 power (W)	Die 2 power (W)	Die 3 power (W)	Die 4 power (W)	Total power (W)
Ami33	543.63 × 543.63	0.2025	0.2850	0.4025	0.4450	1.335
Hp	1664.57 × 1664.57	0.8200	1.2050	0.8050	1.0200	3.850
Ami49	2350.31 × 2350.31	2.0550	2.0700	2.3200	2.5050	8.950
Xerox	1951.18 × 1951.18	2.3300	2.4450	2.1250	2.4750	9.375

Table 2. Simulation settings.

Item	Value
TSV resistance (*m* Ω)	30
Bump resistance (*m* Ω)	5
Metal sheet resistance (*m* Ω/square)	22.1
Supply voltage (V)	1.1
Target IR-drop (%)	5

Table 3. Comparison results for number of power bumps and TSVs.

Circuits	Regular power bumps and non-regular TSVS [10]				Proposed	
	# of mesh	Mesh width (μm)	# of power bumps	# of power TSVs	# of power bumps	# of power TSVs
Ami33	10×10	6	100	21	5	24
Hp	10×10	22	100	42	11	40
Ami49	10×10	34	100	216	52	153
Xerox	10×10	26	100	84	27	90
Avg. ratio	-	-	1.000	1.000	0.238	0.846

Parquet is a free open-source software for floorplanning based on simulated annealing. The TSV simulation settings used are shown in Table 2 [7]. The metal coverage constraint for the power delivery network is set to 40% because the circuits used for simulations are of relatively small size [9].

1. Result of the Comparison for the Number of Power Bumps and TSVs

To demonstrate the superior results produced by our proposed algorithm, we compared our proposed algorithm to the conventional algorithm in [10], which places initial power bumps regularly and power TSVs non-regularly to satisfy the

IR-drop constraint. The simulation environment for the comparison between the two algorithms is the same as the previous simulation environment for obtaining an optimum mesh structure.

Table 3 compares results between the conventional algorithm [10] and our proposed algorithm for the number of power bumps and TSVs. In Table 3, each optimum mesh structure for ami33, hp, ami49, and xerox circuits is determined to minimize the number of power bumps and TSVs in [10]. The average results of the number of power bumps and TSVs of the conventional algorithm for several benchmarks are converted to 1.000 as a standard to compare with our proposed algorithm as shown in Table 3.

As in Table 3, the number of power bumps and TSVs used in our proposed algorithm is less than those used in the conventional algorithm to satisfy the IR-drop constraint with an optimum mesh structure. Our proposed algorithm reduced the number of power bumps by 76.2% and the number of power TSVs by 15.4% compared with the conventional algorithm, on average, for four circuits with 4-die stacked 3D ICs. In the cases of ami33 and xerox, the number of power TSVs is increased by approximately 10%. However, in these cases, our proposed algorithm reduced the number of power bumps by 95% and 73%, respectively. According to [14], a larger number of power bumps induces a smaller inserted number of power TSVs, to satisfy IR-drop constraint. Because there is a greater number of power bumps in [10] than in our proposed algorithm, for some benchmark circuits, the number of power TSVs is increased slightly. However, the benefit of the reduced number of power bumps far outweighs the small increase in the number of power TSVs.

2. Comparison of Voltage Variation with Conventional Algorithms

To verify that our proposed algorithm can not only minimize the number of power bumps and TSVs but also supply voltage more efficiently to the power delivery network by shifting the location of power bumps and TSVs and distributing the IR-drop more evenly, we compared our proposed algorithm to the conventional algorithm [10] and the previous work [14]. In [10], power TSVs are placed non-regularly, but power bumps are regularly placed on every node on Die 1. Because the amount of power that is supplied to the entire die from regularly placed power bumps is greater than the power of the results of our proposed algorithm, it is not appropriate to directly compare the voltage variation results of the two algorithms. In this section, we compare the results with a down-scaled number of regular power bumps of [10] similar to the number of power bumps of our proposed algorithm. In [14], power bumps and TSVs are paced non-regularly; however, the voltage variation is not optimized. Table 4 shows the result of comparing the minimum voltage and voltage variation in each die and the entire dies among the results from [10], [14], and

Table 4. Comparison results of voltage variation.

Circuits	Methods	Die 1		Die 2		Die 3		Die 4		Entire dies
		Min volt.	Volt. variation	Min volt.	Volt. variation	Min volt.	Volt. variation	Min volt.	Volt. variation	Volt. variation
Ami33	[10]	1.0637	0.0088	1.0536	0.0110	1.0503	0.0100	1.0454	0.0111	0.0149
	[14]	1.0668	0.0055	1.0585	0.0068	1.0578	0.0058	1.0480	0.0076	0.0105
	Prop.	1.0702	0.0051	1.0605	0.0055	1.0589	0.0050	1.0499	0.0061	0.0097
Hp	[10]	1.0487	0.0160	1.0471	0.0092	1.0453	0.0080	1.0450	0.0075	0.0155
	[14]	1.0619	0.0088	1.0611	0.0060	1.0470	0.0081	1.0512	0.0058	0.0110
	Prop.	1.0770	0.0053	1.0716	0.0041	1.0536	0.0056	1.0579	0.0045	0.0098
Ami49	[10]	1.0755	0.0072	1.0754	0.0052	1.0515	0.0080	1.0696	0.0056	0.0081
	[14]	1.0802	0.0065	1.0781	0.0053	1.0577	0.0091	1.0723	0.0062	0.0084
	Prop.	1.0873	0.0035	1.0846	0.0024	1.0606	0.0078	1.0742	0.0034	0.0077
Xerox	[10]	1.0495	0.0130	1.0550	0.0076	1.0459	0.0082	1.0454	0.0070	0.0117
	[14]	1.0643	0.0084	1.0622	0.0057	1.0472	0.0069	1.0478	0.0061	0.0127
	Prop.	1.0736	0.0066	1.0679	0.0046	1.0468	0.0072	1.0543	0.0054	0.0115
Average ratio	[10]	0.983	2.195	0.987	1.988	0.993	1.336	0.992	1.608	1.297
	[14]	0.991	1.424	0.994	1.433	0.997	1.168	0.995	1.324	1.101
	Prop.	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000

our proposed algorithm. In Table 4, "Min volt." denotes the minimum voltage value among the nodes in each die, and "Volt. variation" denotes the standard deviation of the voltage values of each node. The average results of the minimum voltage and voltage variation of our proposed algorithm for several benchmarks are converted to 1.000 as a standard. As shown in Table 4, we can identify that on average the minimum voltage of the nodes on each die is improved by 1.1% by using our proposed algorithm compared with the conventional algorithm for four circuits, while the number of power bumps and TSVs is reduced or similar. In the

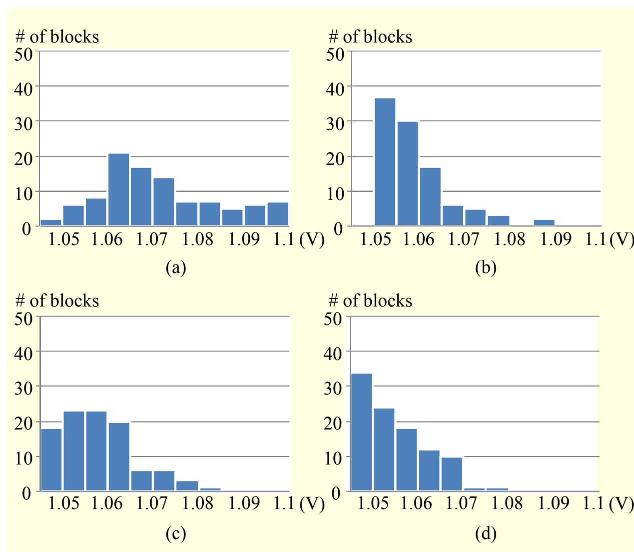

Fig. 13. Voltage histogram in power delivery network for 4-die stacked xerox circuit using the conventional algorithm: (a) Die 1, (b) Die 2, (c) Die 3, and (d) Die 4.

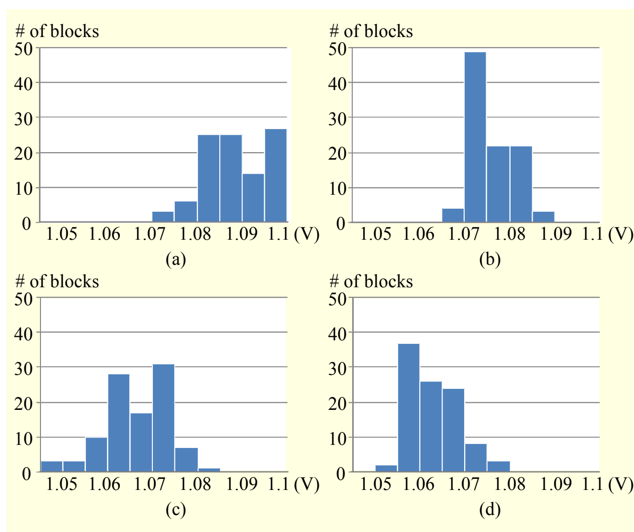

Fig. 14. Voltage histogram in power delivery network for 4-die stacked xerox circuit using the proposed algorithm: (a) Die 1, (b) Die 2, (c) Die 3, and (d) Die 4.

simulation, because the supply voltage is 1.1 V and the target IR-drop is 5%, the voltage values of the nodes of the results of all algorithms range between 1.045 V and 1.1 V; therefore, the improvement of the minimum voltage value of our proposed algorithm is not largely shown. However, in terms of voltage variation as the key of our proposed algorithm, we can confirm that the deviations of voltages of our proposed algorithm are improved by 119.5%, 98.8%, 33.6%, and 60.8% on average for Die 1, Die 2, Die 3, and Die 4, respectively, comparing with [10]. Also, the deviations of voltages of our proposed algorithm are improved by 42.4%, 43.3%, 16.8%, and 32.4% on average for Die 1, Die 2, Die 3, and Die 4, respectively, comparing with [14]. The voltage variations for all dies are improved by 29.7% and 10.1% for the four benchmarks comparing with [10] and [14], respectively.

Figure 13 shows the histograms of voltage variation at the nodes in a power delivery network for a 4-die stacked xerox circuit using the conventional algorithm. In the same manner, Fig. 14 shows the histograms of voltage variation at the nodes in a power delivery network for a 4-die stacked xerox circuit using our proposed algorithm. We can ascertain that the whole of the node voltages in the power grid increase somewhat and that the voltage variation is also reduced by using our proposed algorithm compared with the conventional algorithm.

V. Conclusion

This paper proposed a 3D power delivery network design methodology to determine optimum mesh pitch and mesh width in a power delivery network for each circuit, place power bumps and TSVs sensitively using this mesh structure, minimize the number of power bumps and TSVs to satisfy the IR-drop constraint, and reduce the voltage variation by shifting the locations of power bumps and TSVs. Our proposed algorithm reduced the number of power bumps by 76.2% and the number of power TSVs by 15.2% on average for four MCNC benchmarks with four stacked dies. Also, by shifting the placed power bumps and TSVs without changing their number, our algorithm can improve the minimum voltage and distribute the voltage variation more evenly. Our proposed algorithm improved voltage variation by 29.7%.

In this paper, we considered static IR-drop. During the switching activity of the digital circuits, dynamic IR-drop is greater than static IR-drop since the current flowing in the metal interconnects is greater than when the circuit is in a steady state. For the real design, dynamic IR-drop analysis is needed. However, it is more time-consuming and more complex to solve dynamic IR-drop analysis. Therefore, we have studied electromigration-aware dynamic IR-drop analysis in our forthcoming research.

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Cheoljon Jang received his BS and MS degrees in electronics and computer engineering from Hanyang University, Seoul, Rep. of Korea, in 2011 and 2013, respectively. He is currently pursuing his PhD degree in nanoscale semiconductor engineering at Hanyang University. His current research interests include SoC design methodology, including physical design automation of 3D ICs.

Jong-wha Chong received his BS and MS degrees in electronics engineering from Hanyang University, Seoul, Rep. of Korea, in 1975 and 1979, respectively and a PhD degree in electronics and communication engineering from Waseda University, Tokyo, Japan, in 1981. Since 1981, he has been a professor of the Department of Electronics Engineering at Hanyang University. From 1979 to 1980, he was a researcher at the C&C Research Center of Nippon Electronic Company, Tokyo, Japan. From 1983 to 1984, he was a visiting researcher at the Korean Institute of Electronics & Technology, Seongnam, Rep. of Korea. In 1986 and 2008, he was a visiting professor at the University of California, Berkeley, USA. He was the chairman of the CAD & VLSI society of the Institute of the Electronic Engineers of Korea in 1993 and the president of the IEEK and of the KIEEE in 2007 and from 2009 to 2010, respectively. He is currently the Chairman of the Fusion SoC Forum. His current research interests are SoC design methodology (including memory centric design and physical design automation of 3D ICs); indoor wireless communication SoC design for ranging and location; video systems; and power IT systems.