Robust Two-Phase Clock Oxide TFT Shift Register over Threshold Voltage Variation and Clock Coupling Noises

Hyoungsik Nam and Eunji Song

This letter describes a two-phase clock oxide thin-film transistor shift register that executes a robust operation over a wide threshold voltage range and clock coupling noises. The proposed circuit employs an additional Q *generation block to avoid the clock coupling noise effects. A SMART-SPICE simulation shows that the stable shift register operation is established for the clock coupling noises and the threshold voltage variation from –4 V to 5 V at a line time of 5 μs. The magnitude of coupling noises on the* Q*(15) node and* Q*b(15) node of the 15th stage is respectively –12.6 dB and –26.1 dB at 100 kHz in the proposed circuit, compared to 6.8 dB and 10.9 dB in a conventional one. In addition, the estimated power consumption is 1.74 mW for the proposed 16-stage shift registers at* V_{TH} *= –1.56 V, compared to 11.5 mW for the conventional circuits.*

Keywords: Shift register, oxide TFT, clock coupling noise, threshold voltage variation.

I. Introduction

Oxide thin-film transistors (TFTs) have been widely examined and developed as a next-generation backplane technology for amorphous silicon and low temperature polycrystalline silicon processes due to low-cost fabrication, high mobility, and desired uniformity for large-sized high-resolution active matrix liquid crystal displays and active matrix organic light-emitting diode displays [1], [2]. In particular, the high mobility of an oxide TFT backplane facilitates the integration of some driving circuitries, such as level shifters and gate driver circuits on glass, for low-cost implementation [3]-[5].

However, because most oxide TFTs are inherently depletion-mode devices and the TFT's threshold voltage is shifted over bias stresses, integrated oxide TFT circuits should be able to operate at a wide threshold voltage range from depletion mode to enhancement mode [6]. To cope with the depletion mode issue in integrated gate drivers, two low-level supply voltages were adopted [7], the double gate scheme was applied to the oxide TFT to control the threshold voltage [8], and the floating gate scheme was employed with capacitors [9]. However, [7] operated only with overlap multi-phase clocks, [8] required more complicated fabrication and circuitry, and [9] needed highly intricate operation and circuit structure.

On the other hand, integrated TFT shift registers should be designed to be robust over clock coupling noises. In general, the gate of a pull-up TFT should be bootstrapped in the floating on-state by a clock signal to pull up the output pulse to the target high level. This node also experiences the clock coupling in the floating off-state, which leads to the fluctuation at the low level of output signals. Therefore, the gate of a pull-up TFT should be floating only during the on-state, and it should be driven to the low supply voltage during the off-state [10], [11]. However, it is difficult to employ the previous approaches of the enhancement-mode TFTs in the backplane of oxide TFTs because the depletion-mode TFT is not turned off even with zero gate-source voltage. This letter demonstrates a robust two-phase clock oxide TFT shift register circuit over clock coupling

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noises for an integrated gate driver, which operates with two low supply voltages in both the depletion mode and enhancement mode.

II. Proposed Shift Register Circuit

As illustrated in Fig. 1(a), the proposed shift register circuit of the *n*-th stage is designed with three blocks: sampling block, *Q* generation block, and output generation block. The sampling block samples the output pulse of a previous shift register (C(*n*–1)) and holds that signal until the output pulse of the next shift register (C(*n*+1)) is asserted. The *Q* generation block provides a *Q*(*n*) signal, which is robust over clock coupling noises, to control pull-up TFTs (T8 and T10). The output

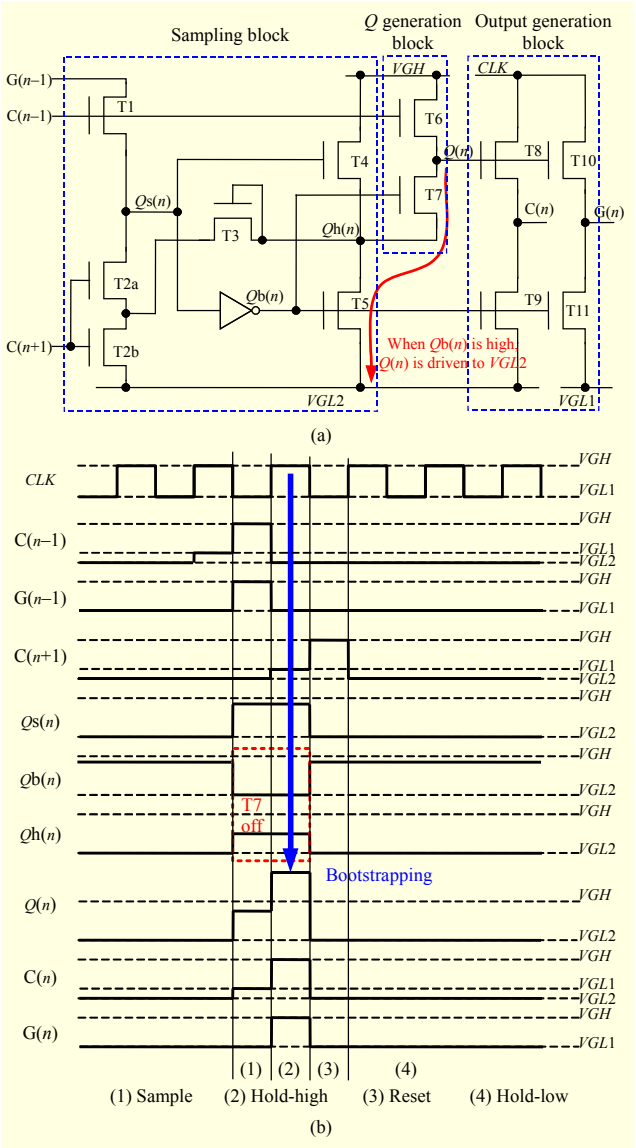

Fig. 1. Proposed robust oxide TFT shift register: (a) circuit schematic and (b) timing diagram.

generation block makes output and gate signals (C(*n*), G(*n*)) by means of a clock signal (*CLK*). *VGH* is the high supply voltage and *VGL*1 and *VGL*2 are the low supply voltages, where *VGL*1 is set to be higher than *VGL*2.

The operation is explained with four periods, as depicted in Fig. 1(b): sample, hold-high, reset, and hold-low. In the sample period, *Q*s(*n*) is asserted by the high pulses of C(*n*–1) and G(*n*–1). The high level of *Q*s(*n*) sets a *Q*b(*n*) node to the low level of *VGL*2 via a wide output dynamic range oxide TFT inverter [12] and a *Q*h(*n*) node to the high level by turning T4 on. Specifically, since *Q*h(*n*) and *Q*b(*n*) are connected to the source and gate of T7, respectively, *Q*h(*n*) must only be higher than *Q*b(*n*) by $|V_{TH}|$ to completely turn off T7. V_{TH} is the threshold voltage of the oxide TFT. Therefore, the size of T4, which determines the high level of *Q*h(*n*), is reduced for low power consumption, even though *Q*b(*n*) of *VGL*2 cannot turn off the depletion-mode T5. The *Q* generation block charges a *Q*(*n*) node to the high level through T6 by the high pulse of C(*n*–1) while T7 is turned off due to high *Q*h(*n*) and low *Q*b(*n*) even in the depletion mode. As a consequence, the output generation block establishes C(*n*) and G(*n*) with a low level of *CLK* at *VGL*1.

During the hold-high period, C(*n*–1) and C(*n*+1) signals cut off the current paths of *Q*s(*n*) to establish the high impedance state, in which the STT scheme [7] is adopted with T2a, T2b, and T3 to avoid the current leakage in the depletion mode. Since *Q*s(*n*) is maintained at a high level, *Q*h(*n*) and *Q*b(*n*) are driven to high and low levels, respectively. Consequently, both T6 and T7, which are turned off, make *Q*(*n*) a floating node and *Q*(*n*) is bootstrapped by the rising transition of *CLK*, which results in the output signals of *VGH* without any voltage losses.

The reset period discharges *Q*s(*n*) by the high pulse of C(*n*+1), which generates the high level of *Q*b(*n*) and the low level of *Q*h(*n*). C(*n*) and G(*n*) are pulled down to *VGL*2 and *VGL*1, respectively, due to the high level of *Q*b(*n*) and the low level of *Q*(*n*).

Finally, in the hold-low period, *Q*s(*n*) becomes a floating node at the low level. Notably, *Q*s(*n*) receives no clock coupling noises because the sampling block is implemented without any connections to *CLK*. As a result, the stable high *Q*b(*n*) and low *Q*h(*n*) signals are achieved, in which C(*n*) and G(*n*) are set to be *VGL*2 and *VGL*1. Specifically, it is of importance to avoid the abnormal operation and large fluctuations in output signals caused by the clock coupling noises from *CLK* through T8 and T10. Because the proposed scheme connects *Q*(*n*) to *VGL*2 through T7 and T5, the coupling effects on *Q*(*n*) are lessened.

III. Simulation Results

The proposed circuit is verified by SMART-SPICE with

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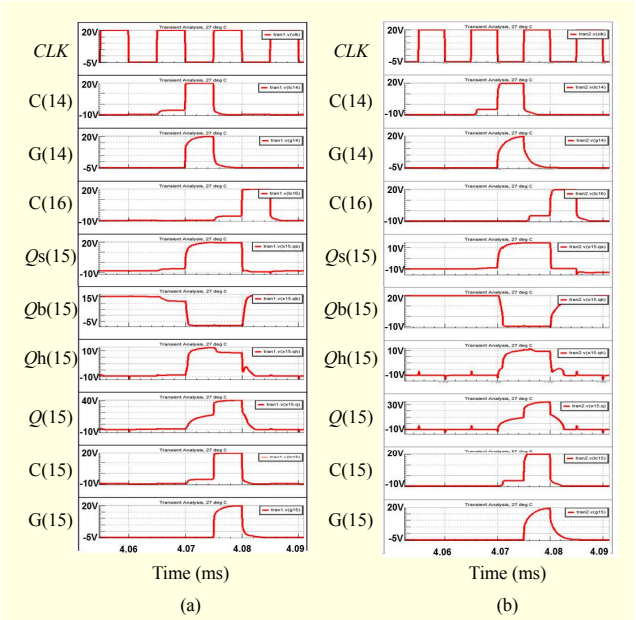

Fig. 2. Simulated waveforms in 15th stage of shift register at clock frequency of 100 kHz: (a) depletion mode (V_{TH} = –4 V) and (b) enhancement mode (V_{TH} = 5 V).

parameters extracted from fabricated *n*-channel amorphous InGaZnO TFTs. The mobility, threshold voltage, and subthreshold slope are 8.57 cm^2/Vs, –1.56 V, and 0.686 V/dec, respectively. The length of each oxide TFT is 10 μm and the widths are as follows: 10 μm, 20 μm, 20 μm, 30μm, 10 μm, 20 μm, 5 μm, 30 μm, 30 μm, 30 μm, 2,000 μm, and 2,000 μm for T1, T2a, T2b, T3, T4, T5, T6, T7, T8, T9, T10, and T11, respectively. The inverter [7] for *Q*b(*n*) is designed with channel widths of 20 μm, 5 μm, 60 μm, and 40 μm for T1p, T2p, T3p, and T4p, respectively. Shift registers consisting of 16 stages are connected with two non-overlapping clocks (*CLK*, *CLK*b) and a start pulse for simulation at the capacitive and resistive gate line loads of 150 pF and 10 kΩ, respectively [13].

The waveforms of some node voltages are presented in Figs. 2(a) and 2(b) at *VGH* = 20 V, *VGL*1 = –5 V, and *VGL*2 = –10 V in the depletion mode (V_{TH} = –4 V) and enhancement mode (V_{TH} = 5 V) at the 15th stage. *CLK* is provided at the frequency of 100 kHz with a 50% duty cycle, which is converted into the line time of 5 μs, applicable to the full high definition 180-Hz active matrix displays of high motion picture quality.

Figure 3 shows a conventional shift register for comparison regarding coupling noise and power consumption. The clock coupling noises of the *Q*(15) and *Q*b(15) nodes are measured for the conventional and proposed circuits at the frequency of *CLK* and in the depletion mode (V_{TH} = –1.56 V) by means of a fast Fourier transform (FFT), as illustrated in Figs. 4 and 5. The magnitudes of coupling noises on *Q*(15) and *Q*b(15) are

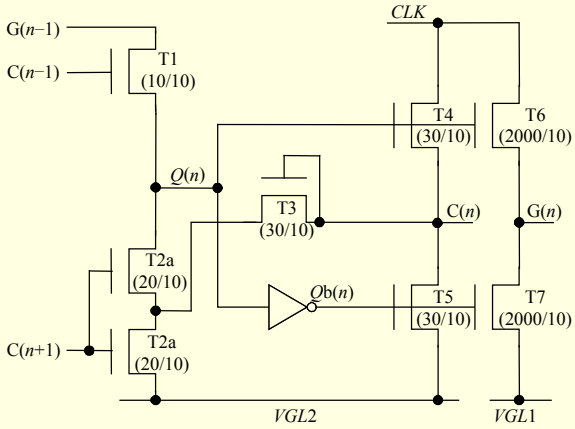

Fig. 3. Conventional shift register.

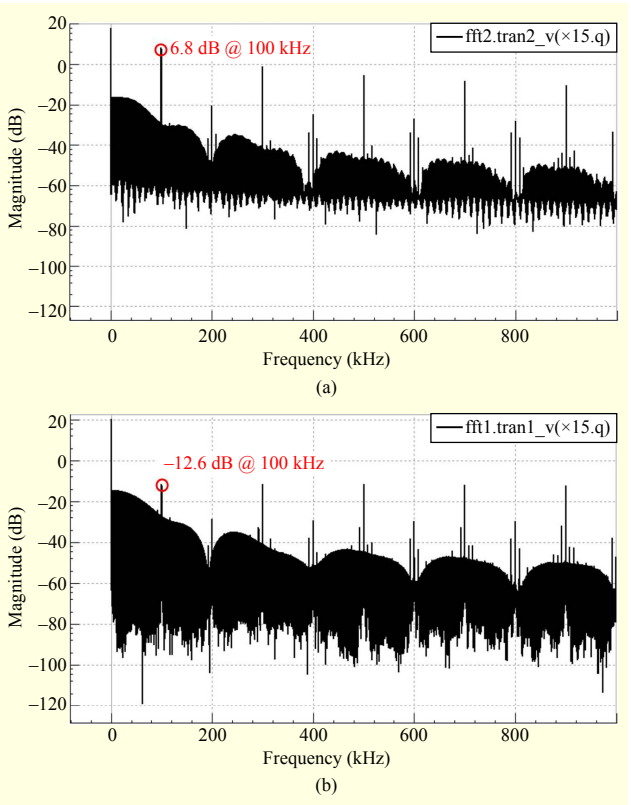

Fig. 4. FFT plots of *Q*(15) nodes: (a) conventional and (b) proposed.

–12.6 dB and –26.1 dB at 100 kHz in the proposed circuit, compared to 6.8 dB and 10.9 dB in the conventional one. When TFTs are set to enhancement mode, the conventional circuit has no current path between the *Q*-node and *VGL*2 during the period of low gate pulse. Consequently, the large amount of clock coupling on the floating *Q*-node through pull-up TFTs causes abnormal operations.

The power consumption of the proposed 16-stage gate driver is estimated to be 1.74 mW at V_{TH} = –1.56 V, whereas that of

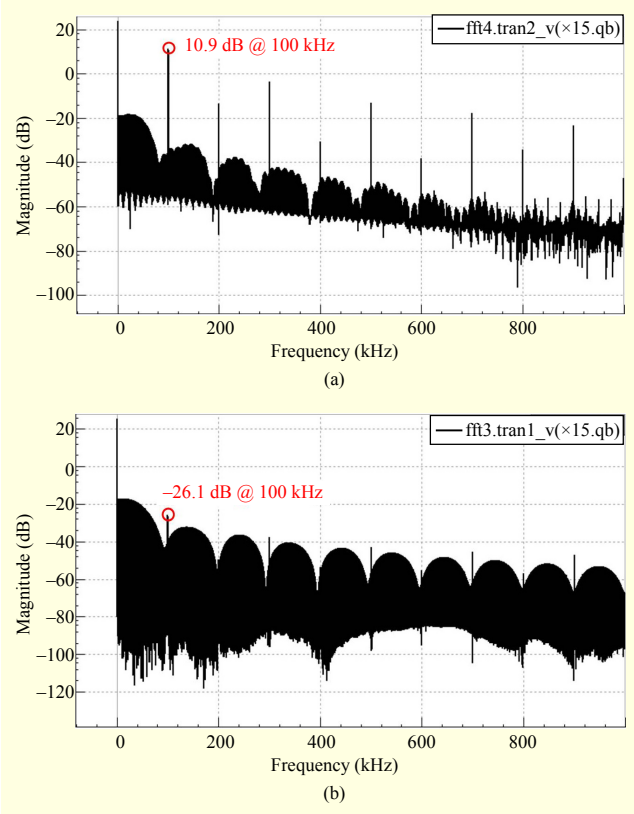

Fig. 5. FFT plots of *Q*b(15) nodes: (a) conventional and (b) proposed.

the conventional one is 11.5 mW due to current leakage through the depletion-mode TFTs. The increase in the circuit area is roughly estimated with the total channel width of the TFTs. The total channel width of the conventional shift register is 4,265 μm, and that of the proposed shift register is 4,330 μm. Therefore, the size of the proposed circuit is only a 1.5% increase over that of the conventional one.

IV. Conclusion

We presented a two-phase clock oxide TFT shift register circuit that is stable over clock coupling noises and a wide threshold voltage range. The proposed circuit adopts the additional *Q* generation block to avoid the abnormal operation and large voltage fluctuation caused by the clock coupling noise. The simulation results ensure the robust shift operation over coupling noises and threshold voltage variation from –4 V to 5 V. This reliable oxide TFT circuit technology will contribute to the lower cost and slim bezel flat panel display with high picture quality.

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