A New Multi-site Test for System-on-Chip Using Multi-site Star Test Architecture

Dongkwan Han, Yong Lee, and Sungho Kang

As the system-on-chip (SoC) design becomes more complex, the test costs are increasing. One of the main obstacles of a test cost reduction is the limited number of test channels of the ATE while the number of pins in the design increases. To overcome this problem, a new test architecture using a channel sharing compliant with IEEE Standard 1149.1 and 1500 is proposed. It can significantly reduce the pin count for testing a SoC design. The test input data is transmitted using a test access mechanism composed of only input pins. A single test data output pin is used to measure the sink values. The experimental results show that the proposed architecture not only increases the number of sites to be tested simultaneously, but also reduces the test time. In addition, the yield loss owing to the proven contact problems can be reduced. Using the new architecture, it is possible to achieve a large test time and cost reduction for complex SoC designs with negligible design and test overheads.

Keywords: Multi-site test, reduced pin count test, test cost reduction.

I. Introduction

Advances in manufacturing and design technologies have led to smaller transistor sizes and a higher level of integration, which require considerable effort and costs. Meanwhile, the emergence of new defect types and reliability problems require a variety of test methods and patterns to ensure a high quality [1]-[3].

To reduce the test costs, various test methods have been presented, including logic and memory built-in self tests (BISTs) [4]-[6], test data compression (TDC) [7]-[11], and multi-site testing utilizing reduced pin count testing (RPCT) [12]-[18]. The BIST method is used to test embedded memory function or logic gates such as combination or sequential logic operations at functional speed. A BIST reduces not only the number of test interface pins between the device under test (DUT) and the automatic test equipment (ATE), but also the test time owing to the use of high-speed testing. However, if the SoC design incorporates numerous design for testability (DFT) rules, it requires more time and effort for the design implementation. In addition, a BIST has testability issues such as low fault coverage. The TDC technique uses additional hardware that can compress the scan output data and decompress the scan input data. An SoC device is able to take a large number of virtual scan chains internally, resulting in less time required for scan shifting, which is the most time consuming process for scan testing using the scan channels of an ATE. There is a limited increase allowed for the number of internal scan chains with a restricted number of channels of the ATE.

Multi-site testing of several DUTs at the same time is one of the best means of reducing the overall test costs [16]. The multi-site test, which reduces the test time by simultaneously

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testing several DUTs using the ATE channel sharing method, takes advantage of the ATE infrastructure in regard to test data storage and test interface facilities. If an SoC device has a large number of test pins, it requires a large number of ATE channels. Therefore, the number of DUTs that can be tested simultaneously is highly dependent on the number of channels and the number of pins of the DUT. For this reason, RPCT is used for conducting a multi-site test, which reduces the number of required test interfaces to allow additional site testing with no extra costs. Therefore, it allows many device types to use multi-site test solutions to address failures within the DUT. In dynamic random-access memory, approximately 512 DUTs are tested simultaneously, with approximately 20 pins for a full function test in parallel test mode. However, in complex SoC designs, about four to sixteen DUTs are tested at the same time owing to the additional channels used for structural testing, which do not use the channel sharing methods [1]. Ideally, this multi-site test method can be applicable to SoC designs. However, it only focuses on a reduction of the required number of ATE channels. The problem here is that it increases the number of required probing needles for test application, and the cost of the probing needles of the probe cards cannot be ignored. It is therefore necessary to decrease the number of probing needles as well as the number of ATE channels for a reduction in the test costs.

The main objective of this paper is the development of an on-chip DFT test architecture to maximize a multi-site test. The proposed multi-site star test architecture (MSTAR) can efficiently utilize the test channels of ATE without affecting other test channels, and allows a test analysis through the ATE channel without disrupting the multi-site test. The advantages of MSTAR are as follows. One advantage is that it shows a negligible design and test overhead for complex SoC designs since it is compatible with IEEE 1149.1 [19] and 1500 [20]. Another advantage is that a high test cost reduction and test time reduction can be achieved since the bandwidth required for the interface between the ATE and one DUT is dramatically reduced.

The outline of this paper is as follows. Section II reviews previous works in this domain. Section III introduces the newly proposed multi-site test architecture (MTA). Section IV describes the proposed MTA structure in detail. Section V presents the experimental results. Finally, section VI provides some concluding remarks.

II. Previous Works

As SoC designs and associated tests become more complex, more complicated methods are required to handle embedded cores for testing and debugging. To reduce the test cost, the test time reduction with reasonable hardware overhead is one of the best solutions.

To reduce the test time and cost without complex implementation, several SoC test architectures have been proposed [14], [15]. In previous research, the use of a controller to reduce the pins for testing is commonly seen; moreover, most of the controllers are made in accordance with IEEE Standard 1149.1, which is more commonly known as the Joint Test Action Group (JTAG) standard. In JTAG, the test procedure and pin attribution are controlled by the test access port (TAP) controller, and a reduced number of pins are used to test each DUT. However, this still limits the efficiency since the number of input pins for delivering the test patterns is equal to the number of output pins for measuring the results.

In [17], [19], and [20], an on-chip DFT infrastructure for multi-site testing is developed for an SoC with heterogeneous cores, including the IEEE Standard 1149.1-wrapped, IEEE Standard 1500-wrapped, and BIST memory cores. An IEEE Standard 1149.1-based hierarchical test manager that can provide IEEE Standard 1500 test control signals was proposed. However, it does not include a parallel test scheme for simultaneous testing.

It is difficult to test complex core-embedded SoC designs without a specific core test method. Goel [14] focused on the design and optimization of an on-chip test infrastructure, called a design for test (DFT) to facilitate high-throughput, multi-site wafer testing of large SoCs. The author also presented a test throughput model and considered parameters such as the test time, index time, abort-on-fail, and contact yield to increase the test throughput and reduce the test cost. This requires a controlling method for the interface between the cores and the ATE. Massive parallel testing using network-on-a-chip (NoC) and an interconnection with a DUT on the test board were also devised [13]. However, it has numerous problems including the test pattern communication, protocol, and NoC architecture. A multi-site testing scheme using IEEE 1149.1 was also proposed, but it requires a lot of probing needles to test the DUT [21]. To solve these problems, a new test architecture that addresses the following issues is proposed in this paper:

1. Test methods with the limitation of an ATE for the simultaneous testing of hundreds of DUTs.
2. Test process for hierarchically embedded cores.
3. Test and design overhead for the RPCT.
4. Compliance with IEEE standards.
5. The feasibility of an existing debugging scheme.

III. Multi-site Star Test Architecture

In MSTAR, the ATE can act like a hub, and a node is considered as a DUT, as shown in Fig. 1. The most important

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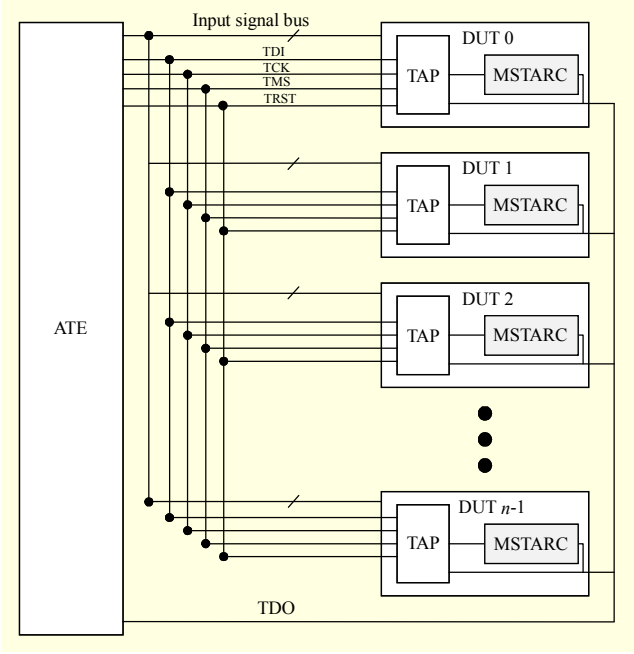

Fig. 1. MSTAR structure.

advantage of MSTAR is its response to a node failure. When an error occurs, only one node will be affected rather than the entire network. Owing to this feature, troubleshooting using a single point for an error connection is quite easy.

In MSTAR, the ATE broadcasts the test input data to several DUTs, and the ATE can easily identify a failed DUT using MSTAR. It is very easy to manage MSTAR using connected DUTs because of its simplicity in testability. Since failures can be logically and easily located in MSTAR, they are easily diagnosed. In addition, since MSTAR uses a very simple format, it can be easily expanded to several test types.

Figure 1 shows the proposed MSTAR structure, which has an ATE acting like a hub and the DUTs performing like nodes. All input and output pins use the same ATE channels. Therefore, all test signals are directly transferred to all DUTs in parallel. A direct addressable method for preventing drive conflicts among the DUTs is handled by MSTAR controllers (MSTARCs) located in the DUTs.

IV. Configuration

1. Structure

The MSTAR architecture consists of IEEE Standard 1149.1, test access mechanism (TAM) and an MSTARC. IEEE Standard 1149.1 and TAM are employed to communicate between the ATE and each DUT. An MSTARC is used to enable an ATE to test several DUTs in parallel without conflicts. IEEE Standard 1149.1 controls all activities pertaining to the test and handles the DUT selection process, and TAP is used to interface the ATE with DUT. Only one output pin, the test data output (TDO), is used to report the results. The TDO of a single DUT is activated when the data are measured after the test, but the others, which produce high-impedance values, are unable to communicate with the ATE. TAM connects the channel of the ATE with the test input ports of the embedded cores according to the IEEE Standard 1500 compliance protocol. However, TAM is composed of only input pins and is without output pins. The sink pins for TAM are removed to reduce the number of test pins. The TDO and test result compressor can cover some of the sink pins, which are used for test results.

An MSTARC selects a DUT and cores to be tested. To select the DUT, MSTARC controls the activation of the enable port of the TDO pad. If the DUT is selected, the TDO enabled port is activated, and the TDO pin drives the input value of the TDO to the ATE. Otherwise, the TDO enable port will be inactive to produce high-impedance values on the TDO pin to prevent the TDO bus contention.

2. MSTARC

Generally, an SoC includes many cores in a single chip, each of which is separately designed and verified before use. However, even if each core operates normally during testing, when the cores are combined in a chip, they may not operate properly. Multiple cores embedded in a single chip may be tested in accordance with IEEE Standard 1149.1, which states that three or four test input pins and one test output pin may be used for testing and debugging of the SoC cores.

The SoC has its own test or debug architecture compliant to IEEE Standard 1149.1. If the test architecture is not compliant with the IEEE standard, then the SoC may not work correctly. To solve the test and debugging problems at a chip level and at an embedded core level, a standard compliant test architecture is required.

The following requirements should be observed for compliance with IEEE Standards 1149.1 and 1500:

1. Use only five TAP pins, which are dedicated for testing and debugging purposes.
2. Use the same access method of a system at the chip and printed circuit board (PCB) levels so that no issues regarding the existence of the system on a single chip or a PCB arise with debugging.
3. Adhere to IEEE Standard 1149.1 to perform the standard interconnect testing using the existing ATE.
4. Allow multiple debugger tools to access the embedded TAP controller of a core without disturbing the current debug operations in other cores.

An MSTARC, which takes into account the considered

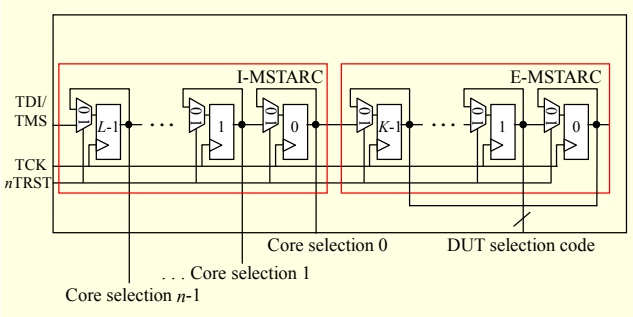

Fig. 2. MSTARC.

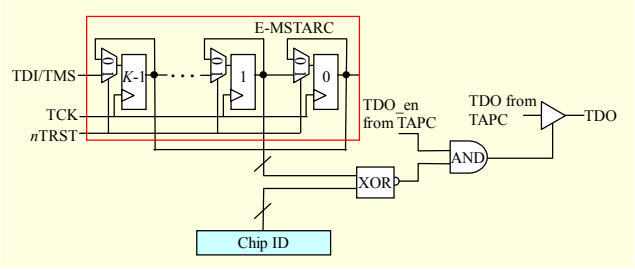

Fig. 3. External MSTAR configuration (DUT selection logic).

requirements, is shown in Fig. 2. The proposed controller, which uses only IEEE Standard 1149.1-dedicated pins, is composed of star test architecture (STAR) registers in the form of shift registers controlled by input TAP pins. The test-logic-reset state of IEEE Standard 1149.1 is configured not to interfere with the existing testing or debugging processes. When the state of the TAP controller is test-logic-reset with *n*TRST (*n*TRST = low), the MTA controller receives data from the test data in (TDI) or test mode select (TMS) pins in response to the test clock signal (TCK). After the data shift for the STAR registers is completed, the data for selecting a DUT and cores are stored in response to the *n*TRST (*n*TRST = high). The stored data then generate the selection signal.

This controller uses only a 5-pin TAP port defined by the IEEE Standard 1149.1. It does not matter if the controlling software and hardware are implemented on a single chip or on a wafer.

3. External Controller

An SoC generally includes a chip identification (chip ID) code register that uniquely identifies each DUT at the wafer level. The process and defect information are declared through the identification code. There are several methods to store the code at the chip level, and fusible elements and programmable elements such as electrically erasable programmable read-only memories are widely used.

Direct addressability is needed for task performance with MSTAR. This addressability is built into MSTARC. The external MSTARC (E-MSTARC) uses a chip ID code and an E-MSTAR register. We set the E-MSTAR register to the intended values using an IEEE Standard 1149.1-compliant method. The comparator always measures the value of the chip ID against the value of the E-MSTAR register. If the two register values are the same, then the comparator output will generate the output signal (matched = low), and a DUT will be selected. The TDO will be controlled by the chip-level TAP controller. Figure 3 shows the DUT selection logic, which includes E-MSTARC, chip ID, and comparator logic such as XOR gates.

4. Internal Controller

An SoC includes numerous cores within a single chip. Owing to the increase of time-to-market pressure, a large number of chip designers and integrators reuse existing designs to create complex SoCs within a limited time budget. The cores embedded in the SoC are designed separately and tested using IEEE Standards 1149.1 and 1500 before being combined into an SoC chip. Once an SoC chip is integrated with several TAP cores, the test and debugging scheme should be compatible with IEEE standards of the chip level test, using the boundary scan register. IEEE standard 1149.1 does not allow the use of multiple TAP controllers within a chip. In addition, embedded cores should be directly interfaced with TAPs so that the debugging schemes of the embedded cores can be used without modification. A management method that is compliant with the IEEE standard for multiple TAP controllers in a chip is needed to test and debug at the chip level.

The internal MSTARC (I-MSTARC) architecture shown in Fig. 4 can support the testing and debugging process at the chip level. I-MSTARC selects at least one TAP controller from the embedded cores and the chip-level TAP controller to be tested, as E-MSTARC selects one DUT that is connected to the ATE

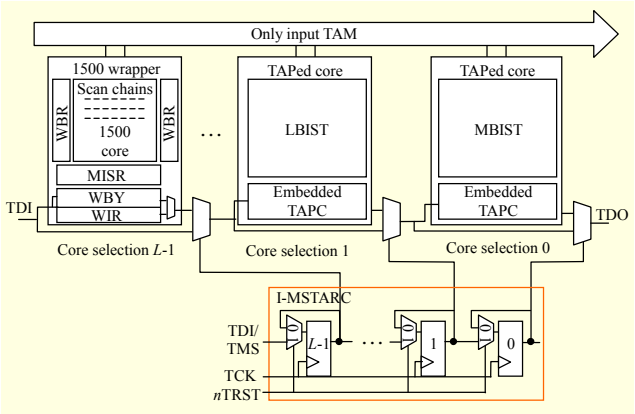

Fig. 4. Internal MSTAR configuration with the other DFT circuit.

to measure the test results. The test results of the selected core are evaluated through a daisy-chained TDI-TDO connection. I-MSTARC includes a shift register for the serial shift of data inputs with TMS or TDI in response to TCK and outputs the data in-parallel in response to *n*TRST. Specifically, I-MSTARC maintains the logic value selecting embedded cores to test or debug when the test reset signal has a high logic level at the test-logic-reset state.

The embedded cores using IEEE Standards 1149.1 and 1500 for testing or debugging are linked with daisy-chained TDI-TDO connections using the core selection values of I-MSTARC and the bypass logic. From a testing perspective, only one embedded core can be selected, while from a debugging perspective, one or multiple embedded cores can be selected. Only the input TAM can be linked to at least core chosen by I-MSTARC, and the sink TAM can be removed by taking a multiple-input signature register (MISR) into the compressor for the test data. If a core is not chosen, the core is bypassed with a multiplexer controlled by the core selection signal from the TDI-TDO daisy-chain and is isolated. This embedded core may be a 1149.1-compliant core or a 1500-compliant core and is controlled by the chip-level TAP controller, as shown in Fig. 4.

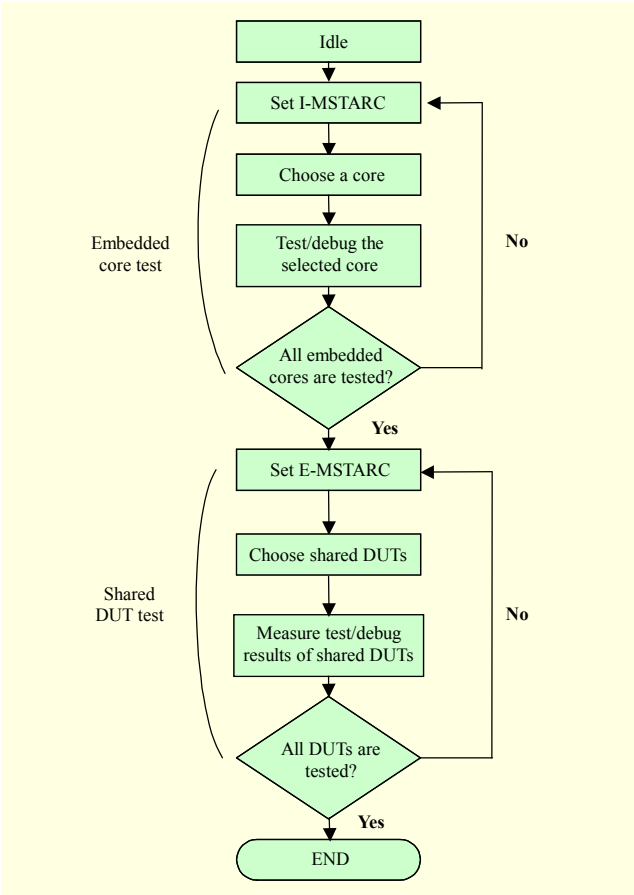

Fig. 5. MSTAR test flow.

5. Test Flow

The test flow of the manufacturing test using MSTAR is shown in Fig. 5. Using I-MSTARC, all cores are tested simultaneously. A series of these core test schemes is repeated until all cores are tested. After the testing of all cores is completed, the concurrently tested DUTs are verified with the E-MSTARC. Similarly, a series of repeated DUT evaluations are performed until all DUTs are verified.

V. Results

1. Test Time Reduction

The total test time of a single DUT is the sum of the index time and the test application time [14]. The index time, T_I is the time required to position the probe interface in contact with the bonding pads of the DUT. The application test time, T_A, is the time required for the inspection of manufacturing faults in the DUT. Only structural tests for logic and memory are considered in this paper.

The total test time for one DUT can be written as

$$T_1 = T_I + T_A.$$

Therefore, the total test time for N DUTs can be written as

$$T_N = N * (T_I + T_A).$$

When P DUTs can be tested in-parallel using a multi-site test method, T_{NP}, the total test time for N DUTs can be written as

$$T_{NP} = \left\lceil \frac{N}{P} \right\rceil (T_I + T_A) + T_M,$$

where T_M is the additional test time from the multi-site test owing to the additional MSTARC setting time and the DUT measurement time.

To compare the effectiveness of the proposed test architecture with the stimuli broadcast method [15], several ITC'02 SoC test benchmarks were used. Based on a target ATE with 1,024 channels, Tables 1 and 2 list the test time reduction ratio of the proposed test architecture over a stimuli broadcast method and hierarchical broadcast method. In Tables 1 and 2, the second column represents the time for testing 1,000 DUTs, the third column represents the number of DUTs tested in-parallel, the fourth column shows the test time per DUT, and the fifth column shows the test time reduction ratio compared to that in [15]. In the case of the stimuli broadcast method, the width of TAM has a correlation with the number of ATE channels used for a single SoC. The hierarchical broadcast method [21] is more efficient than stimuli broadcast, but has a bottleneck in the probe card.

For example, consider F2126 shown in Table 1. Using [15],

Table 1. Experimental results for multi-site testing using 16 TAM width.

ITC'02 benchmark	TAM width (16) used 1,000 probing needles			
	Stimuli broadcast [15]			
	Test time of 1,000 DUTs (cycle)	No. of tested DUTs in parallel	Test time per DUT (cycle)	Test time reduction ratio
F2126	40,571,000	8	40,571	N/A
P22810	54,847,875	8	54,847	N/A
P34392	116,993,250	8	116,993	N/A
P93791	219,498,750	8	219,498	N/A
T512505	1,313,027,500	8	1,313,027	N/A
Hierarchical broadcast [21]				
F2126	30,680,480	32	29,962	26.1%
P22810	38,663,456	32	37,757	31.2%
P34392	53,235,072	32	51,988	55.6%
P93791	100,765,440	32	98,404	55.2%
T512505	376,757,440	32	367,928	72.0%
Proposed method				
F2126	22,051,595	45	21,306	47.5%
P22810	27,789,359	45	26,850	51.0%
P34392	38,262,708	45	36,969	68.4%
P93791	72,425,160	45	69,976	68.1%
T512505	270,794,410	45	261,637	80.1%

Table 2. Experimental results for multi-site testing using 32 TAM width.

ITC'02 benchmark	TAM width (32) used 1,000 probing needles			
	Stimuli broadcast [15]			
	Test time of 1,000 DUTs (cycle)	No. of tested DUTs in parallel	Test time per DUT (cycle)	Test time reduction ratio
F2126	38,311,750	4	38,312	N/A
P22810	56,641,000	4	56,641	N/A
P34392	136,144,750	4	136,145	N/A
P93791	221,520,750	4	221,521	N/A
T512505	1,313,955,000	4	1,313,955	N/A
Hierarchical broadcast [21]				
F2126	31,067,792	18	30,821	19.6%
P22810	45,495,184	18	45,135	20.3%
P34392	55,721,624	18	55,279	59.4%
P93791	97,908,888	18	97,132	56.2%
T512505	338,333,520	18	335,649	74.5%
Proposed method				
F2126	21,636,498	26	21,338	44.3%
P22810	31,684,146	26	31,247	44.8%
P34392	38,806,131	26	38,271	71.9%
P93791	68,186,547	26	67,246	69.6%
T512505	235,625,130	26	232,372	82.3%

eight DUTs are tested in parallel, 125 repetitions are necessary to test 1,000 DUTs, and the total test time is 40,571,000 cycles. On the other hand, using the proposed method, 45 DUTs are tested in-parallel, 23 repetitions are necessary to test 1,000 DUTs, and the total test time is 22,051,595 cycles. The throughput can be represented as the number of tested DUTs in a given time unit. Therefore, the throughput is the inverse of the test time per DUT (given in the fourth column). The throughput of [15] is 1/40,571 = 0.0000246 DUT/cycle and that of the proposed method is 1/21,306 = 0.0000469 DUT/cycle. If we assume that the throughput of the method [15] is 1, the throughput of the proposed method is 1.91. The proposed method has the highest test time reduction ratio and the best throughput. The overhead comes from setting up the value of the MSTARC and measuring the test results of the embedded cores using MISR.

2. Design Consideration

MSTAR can be implemented with a very small design size. Because MSTARC is composed of a simple structure including STAR registers, a comparator, and bypass logic, substantially reduced gate counts can be achieved.

Table 3. Analysis of hardware overhead.

ITC'02 benchmark	Hardware overhead (gate counts)			
	I/O numbers	[15]	[21]	Proposed method
F2126	*I*:52, *O*:140, *B*:196	3,828	5,956	5,427
P22810	*I*:10, *O*:67, *B*:96	2,774	5,298	4,978
P34392	*I*:32, *O*:27, *B*:114	2,914	5,372	5,092
P93791	*I*:103, *O*:79, *B*:66	3,514	6,498	6,254
T512505	*I*:15, *O*:13, *B*:132	2,810	5,090	4,728

Table 3 shows an analysis of the extra hardware overhead, which means extra gate counts for the testing. It is mainly affected by the number of inputs and the TAP controller. In Table 3, *I* is the number of input pads, *O* is the number of output pads, and *B* is the number of the bidirectional pads. The hardware overhead of the proposed method is larger than in [15] owing to the size of the MSTARC hardware, but is smaller than that in [21]. The hardware overhead in [15] is the

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Table 4. Analysis of test cost factors.

	[15]	[17]	[21]	Proposed method
Test application time	Long	Medium	Short	Very short
Design complexity	Low	Medium	High	Low
Hardware overhead	Low	High	Medium	Medium

sum of the boundary scan and a TAP controller, and that in [21] is the sum of a boundary scan and a hierarchical controller. However, the overhead of the proposed method is the sum of I-MSTARC, E-MSTARC, and an MSTARC. In addition, this overhead is relatively small compared to the DUT.

MSTAR adapts the existing test and debug scheme without any modifications. Since it employs IEEE standard test methods with no additional test ports, no modification of the test scheme for the embedded cores is needed. Since it is a seamless implementation flow, hard macro cores can be used, which are unable to be modified. For this reason, the total design turnaround time can be reduced.

3. Test Cost Comparison

Table 4 shows an analysis of the test cost factors. The test application time means the test access time for the total DUT in the wafer, the design complexity indicates how difficult it is to design the circuitry in the probe cards, and the hardware overhead means extra gate counts for the testing. The main advantage of the MSTAR architecture is that it allows all complex SoC DUTs to be tested in-parallel with a very small hardware overhead, whereas the other approaches perform DUTs testing in-serial. By adding a small circuitry to the DFT circuitry included in a complex SoC, the MSTR provides a direct path from the ATE to each SoC. The proposed method shows an outstanding performance in terms of test application time with a small area overhead.

VI. Conclusion

Multi-site testing of several DUTs at the same time is one of the best means of reducing the overall test costs. The proposed MSTAR, which is compatible with IEEE Standards 1149.1 and 1500, does not require any additional test ports or the modification of embedded cores. In addition, a new seamless management method is proposed that can handle multiple embedded cores.

The experimental results, using benchmark circuits show that MSTAR can test multiple DUTs and cores simultaneously, thus reducing the test time drastically. The results show that the test time reduction ratio over the previous works is very high with relatively small overhead. Therefore, it is a practical solution for multi-site testing with a high test cost reduction.

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