

# An Efficient 5-Input Exclusive-OR Circuit Based on Carbon Nanotube FETs

Ronak Zarhoun, Mohammad Hossein Moaiyeri, Samira Shirinabadi Farahani, and Keivan Navi

The integration of digital circuits has a tight relation with the scaling down of silicon technology. The continuous scaling down of the feature size of CMOS devices enters the nanoscale, which results in such destructive effects as short channel effects. Consequently, efforts to replace silicon technology with efficient substitutes have been made. The carbon nanotube field-effect transistor (CNTFET) is one of the most promising replacements for this purpose because of its essential characteristics. Various digital CNTFET-based circuits, such as standard logic cells, have been designed and the results demonstrate improvements in the delay and energy consumption of these circuits. In this paper, a new CNTFET-based 5-input XOR gate based on a novel design method is proposed and simulated using the HSPICE tool based on the compact SPICE model for the CNTFET at the 32-nm technology node. The proposed method leads to improvements in performance and device count compared to the conventional CMOS-style design.

**Keywords:** Nanotechnology, carbon nanotube field-effect transistor, CNTFET, high-performance circuits, CNTFET-based inverter, exclusive-OR gate, XOR gate.

## I. Introduction

No one can imagine today's world without the influence and power of computer technology, which dominates many aspects of people's lives, from such simple details as cell phones to such important and critical projects as those in aeronautics. All computer-based technological improvements are possible through computational functions, which are made up of precise logic gates. Such logic gates as NOT, NAND, NOR, and XOR are the main building blocks of logical functions [1], [2]. Considering these gates, the XOR gate plays a significant role in computational processors with low-power purposes and arithmetic circuits [3], [4], such as full adder cells [5], [6]-[8], parity bit generators and parity checkers [9], multipliers such as the polynomial basis multiplier [10], and comparator circuits [8], [11], [12]. High-speed XOR gates are needed for summation of partial products in multiplier circuits, and they are also used in MUX modules in arithmetic circuits [12].

The most famous application of the XOR gate is in coding processes and data encryption or decryption, especially in AES (Advanced Encryption Standard) [1], which is sufficiently used in data communication. In design testing, it is used in built-in self-test structures [10] and is essential in cryptography [9], FPGAs, and high-performance structures. The XOR gate is even used in compressors, phase detectors, error detection, and error correction circuits [13]. Digital signal processor circuits with a logarithmic number system composed of several multipliers and adders benefits from XOR gates [14]. Moreover, the important role of this gate has even appeared in optical telecommunication networks for bit pattern recognition, operations related to address comparison, and so on [15], [16]. Design and development of XOR gates with conventional CMOS architecture is limited by the number of its inputs. As a

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result, XOR gates with two or three inputs were designed. However, the implementation of an XOR gate with four or more inputs is inconvenient because it can worsen the propagation time or delay of the charge or discharge of the load capacitor.

Besides the flexible behavior of CMOS technology and its significant capability in integration of the logical circuits, it encounters many critical difficulties. According to Moore's law, the number of transistors of an integrated chip doubles every 18 months. The scaling down of technology has closely reflected Moore's law. As the length of physical gates reaches the nanoscale, different destructive effects, such as short channel effects, affect the current-voltage characteristics of the MOSFET family, which limits the miniaturization of the feature size of this family [2], [17], [18]. Another negative effect of miniaturization is the exponential increase of leakage current involving subthreshold voltage caused by scaling down the supply voltage and threshold voltage [19]. The increase of leakage and OFF-current reduces the reliability of a circuit [20]. Massive process variation, critical power overhead, and a decrease in the gate control are other destructive challenges of MOSFET devices at the nanoscale [20]-[22]. According to Moore's law, it can be concluded that the bulk-silicon transistor should be replaced by a promising alternative device in the near future [19]. Therefore, possible replacements for CMOS technology, including the single-electron transistor, the quantum-dot cellular automaton, molecular devices (benzene rings), and the carbon nanotube field effect transistor (CNTFET), are under investigation [23]-[25]. Among these alternative technologies, the CNTFET is the most encouraging substitution for the conventional MOSFET family due to its similarities to MOSFET in terms of electrical properties and manufacturing process [26]. Up to now, many circuits have been successfully designed based on CNTFET technology, such as binary and ternary full adder cells, SRAM storage cells, multiple-valued logic circuits, and min-max circuits [27], [17]-[19], [21]-[24], [28]. The CNTFET can also be applied in polylactic acid structures [29]. Due to the structure of the conventional CMOS design, which consists of complementary pull-up and pull-down networks with pure and inverted inputs, the XOR gate is considered to have high power consumption [11]. Due to the wide range of applications of the XOR gate, different design techniques [13] have been introduced to overcome its high power consumption, such as the 3-input XOR gate proposed in [9]. In this work, a novel efficient CNTFET-based direct design for a 5-input XOR gate that improves the performance of the circuit is proposed.

The remainder of this paper is organized as follows. In section II, the CNTFET technology and its interesting attributes and benefits are reviewed. The conventional CMOS-like

5-input XOR is examined in section III. The proposed design is presented in section IV, and section V includes the simulation results and comparison. At last, section VI provides the final conclusions.

## II. CNTFET Review

One of the most promising alternatives to the MOSFET is the CNTFET [2]. The most important and significant attribute of CNTFET is its spectacular ability in current carrying or current driving, and experiments have shown that CNTFET is the best for this purpose [30]. CNTFET can operate five times faster than CMOS in the best case without any extra power overhead [26]. Another essential characteristic of CNTFET is its flexible behavior in manipulating the threshold voltage ( $V_{th}$ ) by adopting a proper diameter for CNTs [17]. There are three types of CNTFET: The first type is the MOSFET-like CNTFET (includes the p-type CNTFET [P-CNTFET] and n-type CNTFET [N-CNTFET]), which operates in a unipolar fashion; The second type is the Schottky barrier (SB) CNTFET, which demonstrates ambipolar characteristics [31] but is not proper for ultra high-performance applications because of the SB element; The third type of CNTFET, suitable for ultra low-power applications, is the band-to-band tunneling CNTFET and has significantly low current in its active mode [23]. The CNTFET has relatively low off-current whenever the transistor is inactive; in other words, when the CNTFET is off, leakage power consumption is very low [18]. CNTFETs have similar structure and electrical characteristics to MOSFETs, which facilitates the exploitation and reuse of previous MOSFET-based architectures and fabrication processes [21].

P-CNTFET and N-CNTFET are the MOSFET-like CNTFETs [23]. The structure of a MOSFET-like CNTFET is demonstrated in Fig. 1; however, the main difference is that the CNTFET does not have a physical channel in the substrate for current flow formed by electron or hole carriers; instead, the current flows through CNTs. The CNTs under the gate region are undoped or intrinsic to have semiconducting behavior and

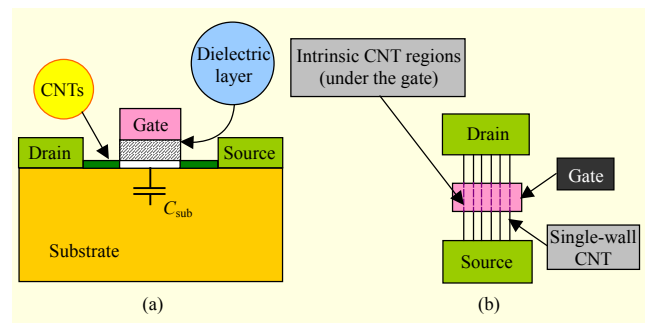


Fig. 1. (a) Cross section view of CNTFET structure; (b) top view of CNTFET.

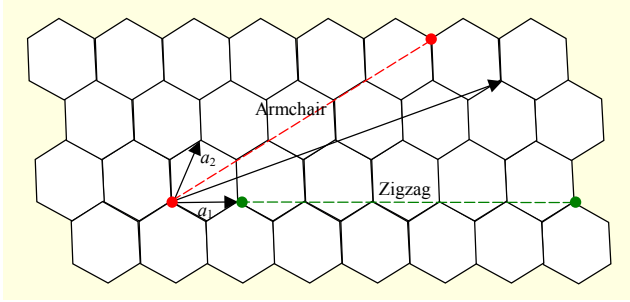


Fig. 2. Unrolled graphite sheet of CNT.

can be controlled by the gate input voltage [26]. The dielectric layer under the gate is deposited on the undoped CNTs (in the middle), and the metal gate layer covers it [18]. Single-wall CNT partitions between the gate and the drain and source are heavily doped to provide low resistors in a serial state whenever the transistor is in its active mode, as shown in Fig. 1 [18], [32]. The CNTFETs switch between active mode and inactive mode by manipulating the electrical potential of the gate. In reports on CNTFET fabrication, it was declared that a near-ballistic [23] or even ballistic transportation can be gained from an intrinsic CNT under low voltage with an approximately 1 micrometer mean free path needed for elastic scattering to obtain efficient improvement in performance [32]-[34]. The fabrication of single-wall CNT (SWCNT) transistors was reported in [18], [35]. An SWCNT, which is made up of a single cylinder of a rolled graphene sheet, can either be metallic or semiconducting [19], [21], [36]. This ability is due to the angle of atoms arranged along the nanotube, which can be represented by a two-dimensional vector known as the chirality vector (Fig. 2). As illustrated in Fig. 2, CNTs can be rolled around in two directions, shown as Armchair and Zigzag [30].

Based on the vector addition rule, it is clear that the chirality vector is composed of unit vectors in each dimension:  $(\vec{a}_1, \vec{a}_2) - |\vec{a}_1| = |\vec{a}_2| = a_0$ . As such, the chirality vector can be formulated as  $\vec{C}_h = n_1 \vec{a}_1 + n_2 \vec{a}_2$ , where the indices  $(n_1, n_2)$  are positive integers that specify the chirality of the nanotube [30]. Therefore, the length of the chirality vector, which is the circumference of the cylinder's base, is calculated according to (1) and CNT diameter  $D_{CNT}$  can consequently be extracted from it, according to (2).

$$|\vec{C}_h| = \sqrt{n_1^2 + n_2^2 + n_1 n_2 \cos 60}, \quad (1)$$

$$D_{CNT} = a_0 \frac{\sqrt{3}}{\pi} \sqrt{n_1^2 + n_2^2 + n_1 n_2}. \quad (2)$$

The parameter  $a_0$  ( $= 0.142$  nm) in (2) is the carbon-to-carbon bond length in a CNT [30]. The  $V_{th}$  of a CNTFET can be calculated according to (3). The  $V_{th}$  of a CNTFET is related to

the bandgap of the intrinsic CNTs lying under the metal gate and has an inverse relation with CNT's diameter [24], [31]:

$$V_{th} \approx \frac{a_0 V_{\pi}}{e D_{CNT}} \approx \frac{0.43}{D_{CNT} \text{ (nm)}}, \quad (3)$$

where  $V_{\pi}$  is the bond energy between two adjacent carbon atoms in a tight bonding model and is equal to 3.033 eV, and  $e$  represents the electric charge of a single electron [28]. The CNTFET current also has a direct relation with the number of its tubes. An increase in the number of tubes intensifies the CNTFET's current and improves the circuit speed [35]; however, to achieve efficient power consumption, the number of tubes should be adopted carefully because it can affect power consumption negatively. As reported in [33], the compact SWCNT model with an intrinsic channel region shows that the SWCNT (with  $n_1 = 19$  and  $n_2 = 0$ ) gains 13 times better CV/I than the n-type MOSFET at the 32-nm node. According to the CNTFET model presented in [34], even with such non-idealities as parasitic capacitors of the gate, the CNTFET performs significantly better than the MOSFET.

### III. Previous Work

Implementation of the XOR gate with five inputs based on the conventional CMOS architecture does not achieve appropriate speed due to the existence of five transistors along each critical path in different transitions. In most of the arithmetical circuits, the XOR gate is placed along its critical path and its poor speed can affect the total performance of the circuit [9]. In other words, the total performance of these circuits is limited to the performance of the XOR gate. On the other hand, the number of transistors of the CMOS structures increases significantly as the number of circuit inputs increase, and this unfortunately affects the circuit's power consumption. This increase is the product of the nature of the XOR gate, which uses its inputs and their complements to generate the desired products to create its correct function as the sum of products.

Obviously, when the number of gate inputs increases, the number of its corresponding inverter gates increases and the size of each product in its function (when the function is formulated as the sum of products) dramatically grows.

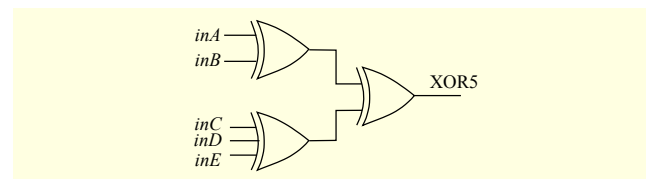


Fig. 3. Scheme of conventional 5-input XOR gate.

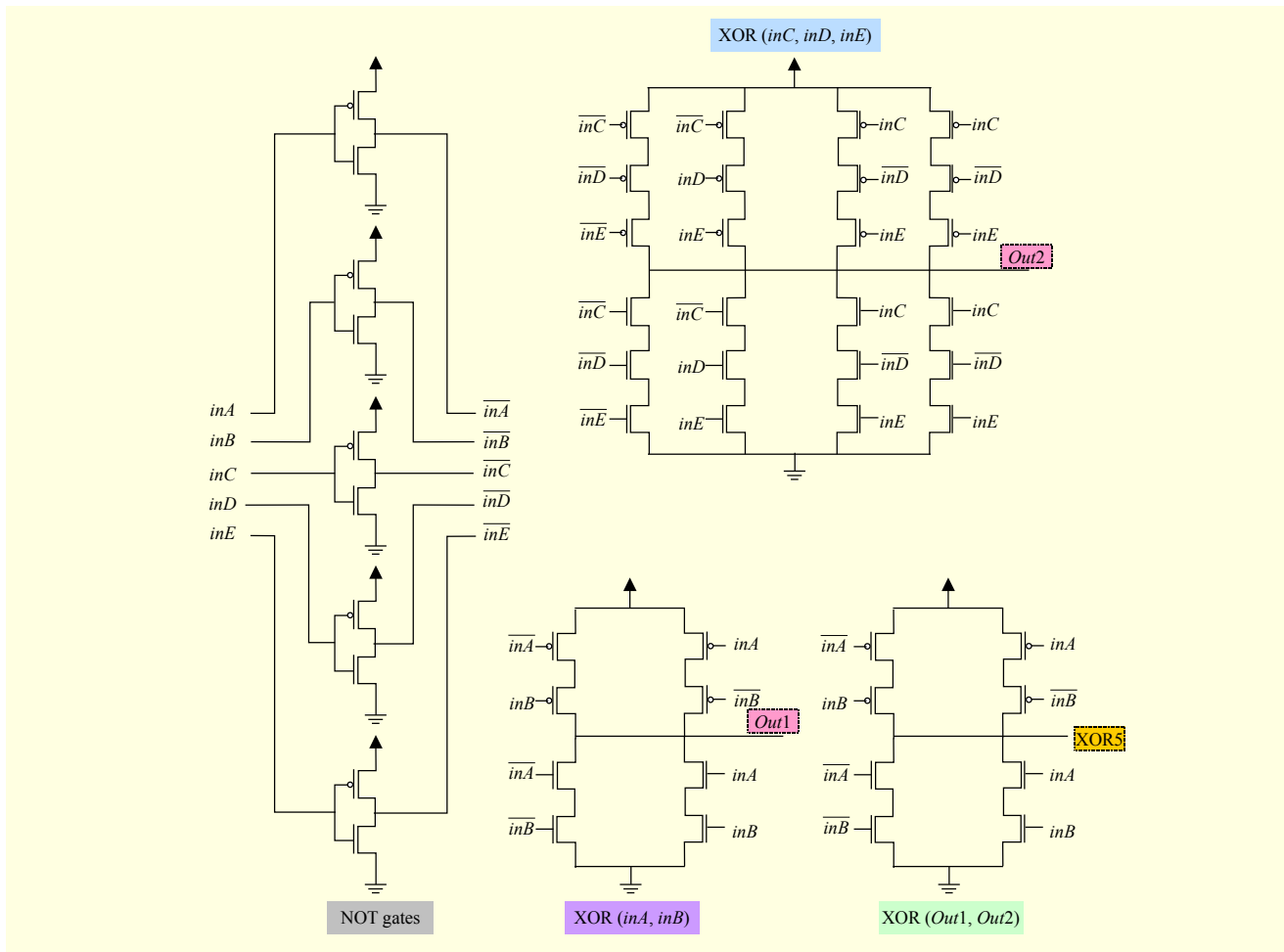


Fig. 4. Transistor structure of conventional 5-input XOR gate.

Implementation of each product of the desired function is achieved by the pass transistors placed in a serial manner, and the circuit's delay significantly increases if there are more than three pass transistors in a row. Therefore, the design of a 5-input XOR gate in a conventional CMOS-like design is unfavorable. To lower the delay and power consumption for a CMOS-like 5-input XOR circuit, MOSFETs are replaced with CNTFETs, and it is also better to implement a 5-input XOR gate by the help of 2-input and 3-input XOR gates in a cascaded structure instead of implementing a 5-input XOR gate directly. The gate level and transistor level schemes of this circuit are respectively illustrated in Fig. 3 and Fig. 4.

#### IV. Proposed Work

In the design of the proposed structure for a 5-input XOR circuit, a CNTFET device is utilized because it is more feasible to use multiple  $V_{th}$  values in this technology according to the relation of  $D_{CNT}$  and the  $V_{th}$ . First of all, it is necessary to design inverters with different  $V_{th}$  values. As mentioned in section II,

the  $V_{th}$  of CNTFET, whether it is P-CNTFET or N-CNTFET, is related to the CNT's diameter, and the diameter has a relation with the  $n_1$  and  $n_2$  parameters of the CNTs. To create the specified  $V_{th}$ , proper values for  $n_1$  and  $n_2$  parameters should be assigned. The difference between  $n_1$  and  $n_2$  parameters should not be divisible by 3 ( $|n_1 - n_2| \neq 3k, k \in \mathbb{Z}$ ); otherwise, the transistor's channel acts as a conductor [21].

The basic gates of the proposed design are three inverters with different thresholds: NOT1, NOT2, and NOT3. NOT1 is utilized to design a logical module, called Module1. In this module, there are five input sources ( $inA$ ,  $inB$ ,  $inC$ ,  $inD$ , and  $inE$ ), each one connected to a capacitor with value  $c$ . The other plates of capacitors are converged to one point, referred to as the  $m$  point (Fig. 5(a)). The benefit of the capacitor network is that the  $m$  point uses the scaled sum of input voltages as the main input for the NOT1 gate. Moreover, the redundant input states are eliminated and the size of the truth table is consequently minimized. By assigning dedicated values to  $n_1$  and  $n_2$  parameters of P-CNTFET and N-CNTFET of NOT1, the  $V_{th}$  of this gate is gained as desired. The configuration of

Module1 is presented in Fig. 5(a), and its functionality is indicated in the second column of the truth table in Fig. 5(b). The first column indicates the addition of logical inputs, as declared in (4) (when  $\Sigma in = 0$ , the voltage of each input is zero; when  $\Sigma in = 5$ , the voltage of each input is equal to  $V_{DD}$ ),

$$inA + inB + inC + inD + inE = \Sigma in, \quad (4)$$

and the corresponding voltage value of these states at  $m$  point can be driven from (5).

$$Voltage(\Sigma in) = V_{DD} \cdot \frac{\Sigma in}{N}. \quad (5)$$

Further,  $N$  indicates the total number of inputs, which is equal to 5 in this case. NOT1 in Module1 operates such that whenever the sum of logical inputs, as presented in (4), exceeds 1, the output value (marked as “Out1”) switches from “1” to “0.” Equation (6) shows the function of Module1.

$$Out1 = \begin{cases} 0, & \Sigma in > 1, \\ 1, & \text{otherwise.} \end{cases} \quad (6)$$

Module2 and Module3, which respectively utilize NOT2 and NOT3, can be designed in a similar way as described above. The structure of Module2 and Module3 are illustrated in Fig. 5(c) and Fig. 5(e) and their functions are declared in (7) and (8), respectively.

$$Out2 = \begin{cases} 0, & \Sigma in > 3, \\ 1, & \text{otherwise,} \end{cases} \quad (7)$$

$$Out3 = \begin{cases} 0, & \Sigma in > 4, \\ 1, & \text{otherwise.} \end{cases} \quad (8)$$

The truth tables of Module2 and Module3 are presented in Fig. 5(d) and Fig. 5(f), respectively.

The voltage transfer characteristics of NOT1, NOT2, and NOT3 are presented in Fig. 6. The truth table of the 5-input XOR can be constructed based on NOT1, NOT2, and NOT3, as shown in Table 1. In the second and third columns, the corresponding outputs of NOT1 and NOT2 are shown. The sums of values in these columns are displayed in the fourth column. Multiplying these amounts by two and adding their results with  $\Sigma in$  results in the values listed in the sixth and seventh columns, which represent the input and output of NOT3, respectively. The final result (5-input XNOR) is written

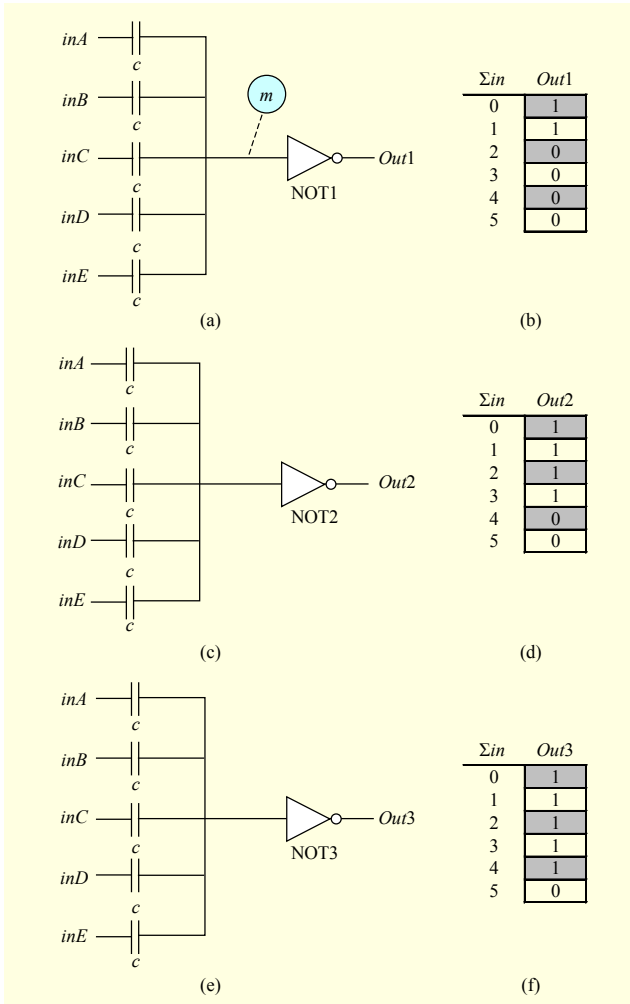


Fig. 5. Module1: (a) scheme; (b) truth table. Module2: (c) scheme; (d) truth table. Module3: (e) scheme; (f) truth table.

Table 1. Truth table of proposed 5-input XOR gate.

$\Sigma in$	NOT1	NOT2	NOT1+NOT2	$2(\text{NOT1}+\text{NOT2})$	$2(\text{NOT1}+\text{NOT2})+\Sigma in$	NOT3	XOR
0	1	1	2	4	4	1	0
1	1	1	2	4	5	0	1
2	0	1	1	2	4	1	0
3	0	1	1	2	5	0	1
4	0	0	0	0	4	1	0
5	0	0	0	0	5	0	1

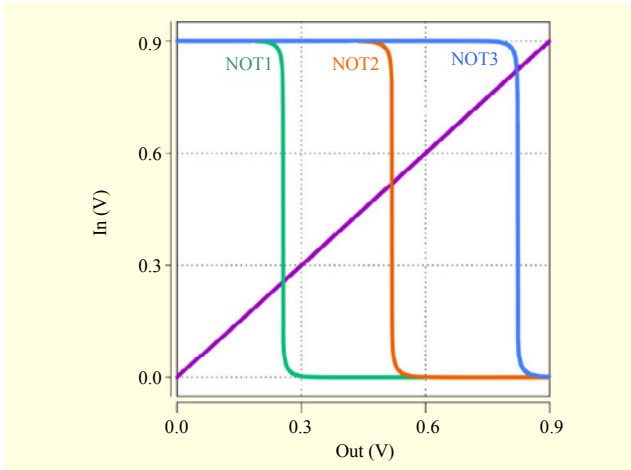


Fig. 6. Voltage transfer characteristics of NOT gates.

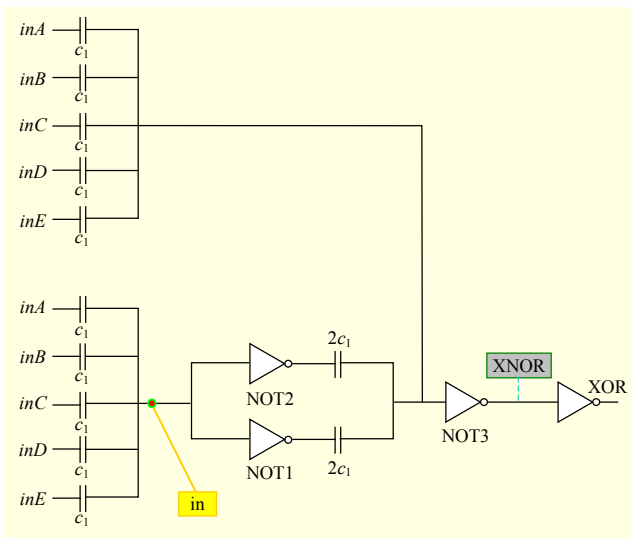


Fig. 7. Scheme of proposed 5-input XOR gate (I).

in the last column. The commensurate circuit's configuration represented in Table 1, which we refer to as the proposed 5-input XOR (I), is illustrated in Fig. 7. To implement the multiplication by two,  $2c$  capacitors are utilized at the outputs of NOT1 and NOT2.

The most inspiring aspect of this design is that this design has considerably less transistors in comparison with the conventional structure of the same function described in section III. As the input signals of NOT1 and NOT2 are generated by means of five equal capacitors and the same signal is also required for producing the input voltage of NOT3, only a single five-capacitor network is enough to generate the  $\Sigma in/5$  signal, which is fed to the NOT1, NOT2, and NOT3 inverters. Moreover, as the input voltage of NOT3 is in fact  $(\Sigma in + 2Out_{NOT1} + 2Out_{NOT2})/9$ , which can also be written as  $(5(\Sigma in/5) + 2Out_{NOT1} + 2Out_{NOT2})/9$ , the  $\Sigma in/5$ ,  $Out_{NOT1}$ , and

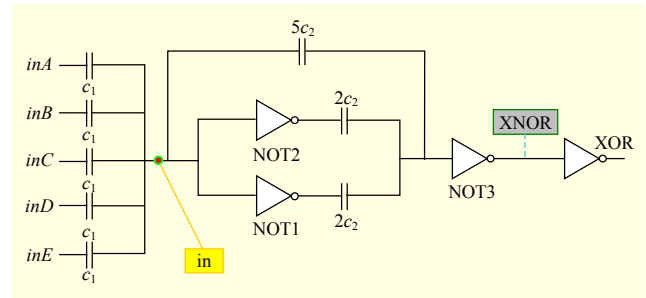


Fig. 8. Scheme of proposed 5-input XOR gate (II).

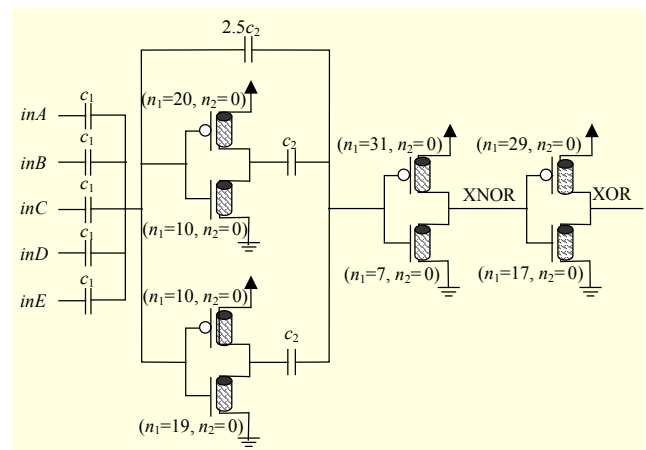


Fig. 9. Transistor structure of proposed 5-input XOR (II) gate with  $c_1 = 9$  fF and  $c_2 = 1$  fF.

$Out_{NOT2}$  signals should be fed into NOT3 by  $5c$ ,  $2c$ , and  $2c$  capacitors. The scheme of this promoted design (proposed 5-input XOR (II)) and its CNTFET-level implementation are illustrated in Fig. 8 and Fig. 9, respectively. This improvement leads to an even lower number of capacitors and interconnections, as well as better performance and energy efficiency.

## V. Simulation Results

The purpose of the proposed design is to gain effective improvements in terms of circuit energy consumption, that is, the production of power consumption and delay, which is the tradeoff between these two parameters [22]. It is significant to verify this product instead of measuring the power and delay separately.

The designs are evaluated using the HSPICE simulator tool based on standard 32-nm CMOS technology and the compact SPICE model for 32-nm CNTFET at the 250-MHz operating frequency, at the 0.9-V supply voltage, and with a 20-fF load capacitor at room temperature. The dedicated parameters of the CNTFET model are shown in Table 2 [23]. This model is created for the MOSFET-like CNTFET for unipolar

Table 2. Basic parameters of CNTFET transistor.

Name	Value	Description
$C_{sub}$	40 pF/m	Coupling capacitance formed between transistor's bulk and channel regions
Pitch	20 nm	Distance from center of one CNT to center of its nearest neighboring CNT
E <sub>fi</sub>	6 eV	Parameter specifies doped source-drain tube's Fermi level
$K_{gate}$	16	Type of dielectric layer's material
$L_{ch}$	32 nm	Length of physical channel
$L_{d1}$	32 nm	Doped CNT drain-side extension region's length
$L_{geff}$	100 nm	Length of mean free path of intrinsic CNT channel for effective elastic scattering
$L_{ss}$	32 nm	Doped CNT source-side extension region's length
$T_{ox}$	4 nm	Dielectric layer's thickness under gate's region
$K_{sub}$	16	Substrate's dielectric constant

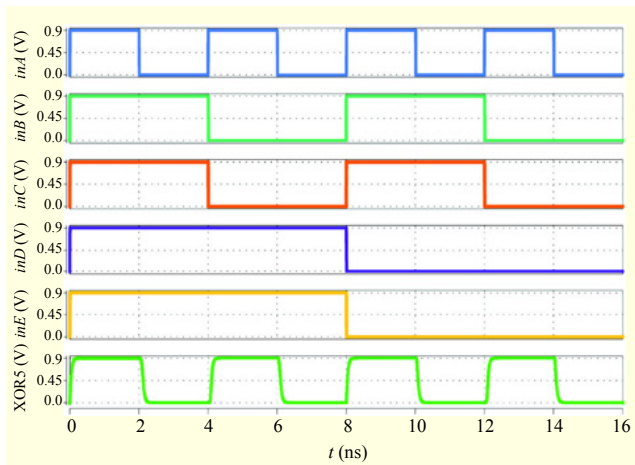


Fig. 10. Transient response of proposed 5-input XOR gate.

P-CNTFET and N-CNTFET devices, which can have more than one CNT in their channel region. This realistic model and circuit-compatible structure of the CNTFET considers non-idealities and various effects, such as inter-CNT charge screening effects, back-gate effects, SB effects at contacts, doped source-drain extension regions, and non-ideal near-ballistic transport and device parasitic resistances and capacitances (Table 2) [21], [23]. The parameters of the conventional CMOS and CNTFET designs are set as  $(L, W) = (32 \text{ nm}, 220 \text{ nm})$  and  $(D, N) = (1.5 \text{ nm}, 5)$ , respectively. The transient response of the proposed design is illustrated in Fig. 10. The simulation results are presented in Table 3. The results demonstrate the superiority of the proposed method, specifically in terms of device count, with respect to the conventional CMOS design.

Table 3. Simulation results.

Parameter	Proposed 5-input XOR gate (II)	Proposed 5-input XOR gate (I)	Conventional CMOS-style 5-input XOR gate
Power ( $\times 10^{-6} \text{ W}$ )	5.611	5.222	4.349
Delay ( $\times 10^{-12} \text{ s}$ )	93.66	107.1	191.1
Energy consumption ( $\times 10^{-16} \text{ J}$ )	5.2553	5.591	8.311
Number of devices	<b>16</b>	20	50

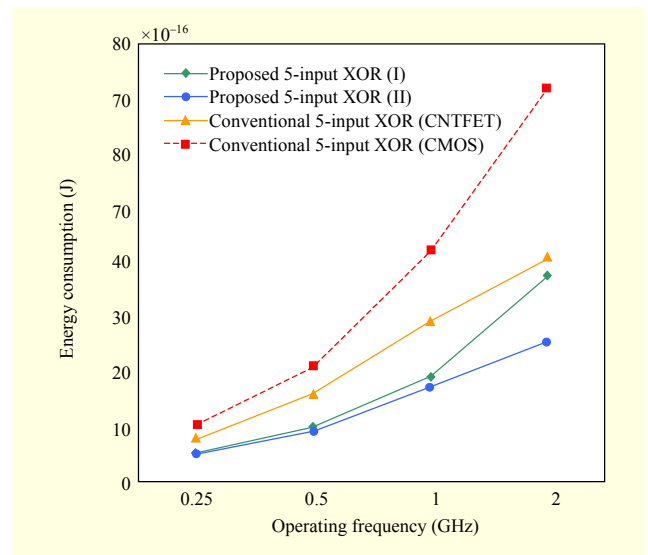


Fig. 11. Energy consumption vs. operating frequency.

The energy consumption curves of the proposed and the conventional 5-input XOR gates (32-nm CMOS and CNFET) simulated at different operating frequencies are presented in Fig. 11. According to the results, the superiority of the proposed design becomes more considerable by increasing the frequency. The load capacitor in the simulations is swept from 15 fF to 25 fF and the extracted curves of delay and energy consumption are presented in Fig. 12 and Fig. 13, respectively.

Delay of a circuit is an important performance metric that is mostly related to the critical path length and the driving capability of the circuit. As shown in Fig. 12, the delay of the proposed model is less than that of the conventional model of the 5-input XOR gate and consequently has significantly more driving power at its output node. The proposed circuit is simulated under different temperatures, varying from 0°C to 80°C, and nearly constant energy consumption for this circuit is demonstrated, which is a consequence of CNTFET's high

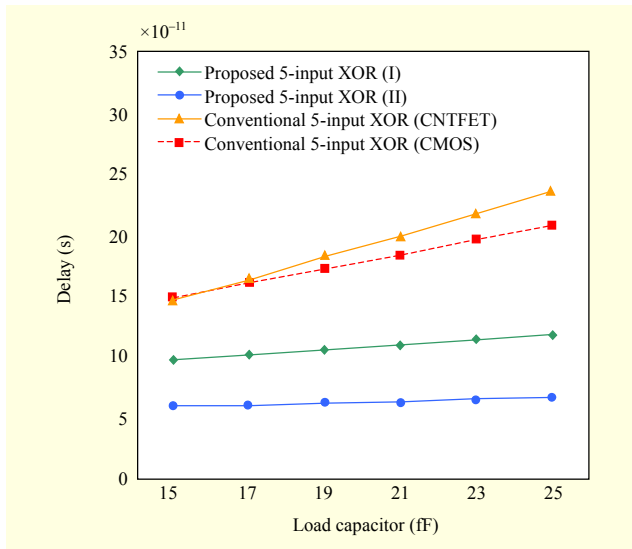


Fig. 12. Delay vs. load capacitor.

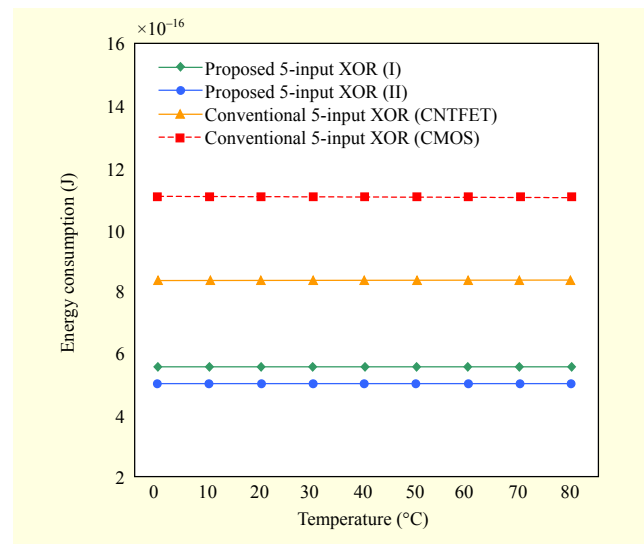


Fig. 14. Energy consumption vs. temperature.

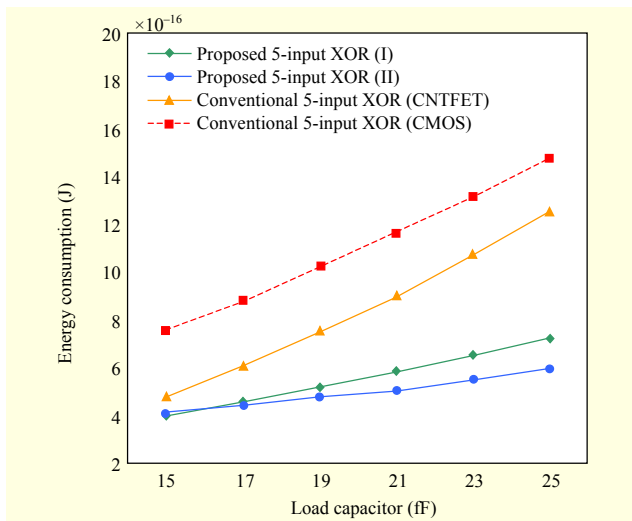


Fig. 13. Energy consumption vs. load capacitor.

thermal stability (Fig. 14) [37].

## VI. Conclusion

In this paper, a high-performance and energy-efficient 5-input XOR gate based on a novel method was proposed. According to reported challenges of scaling down the conventional CMOS technology and due to the significant advantages and flexible characteristics of the MOSFET-like CNTFET family, the proposed circuit was designed based on the unique properties of the CNTFET technology. The proposed design is composed of three CNTFET-based inverters and input capacitors and consequently has a simpler structure and lower number of required devices compared to the conventional CMOS method. The simulation results in an

HSPICE environment using 32-nm CMOS and CNTFET models also demonstrated improvements in terms of performance.

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