Regular paper http://dx.doi.org/10.13067/JKIECS.2014.9.11.1227

0.13㎛ 기술의 shrink에 따른 DC Parameter 매칭에 관한 연구

문성열[*] · 강성준[*] · 정양희[**]

A Study on the DC parameter matching according to the shrink of 0.13㎛ technology

Seong-Yeol Mun[*] · Seong-Jun Kang[**] · Yang-Hee Joung[**]

요 약

본 논문은 기존의 poly length만의 축소와 달리 입, 출력 소자를 포함한 core 디바이스의 0.13㎛ 디자인을 10% 축소하는 것으로 여러 채널 길이에 따른 body effect와 doping profile simulation을 해석하였다. 축소 전의 DC 파라미터 매칭을 위하여 게이트 산화막의 decoupled plasma nitridation 처리와 LDD(Lightly Doped Drain) 이온주입 전 TEOS(Tetraethylortho silicate) 산화막 100Å 그리고 LDD 이온주입을 22o tilt-angle(45o twist-angle)로 최적화하였고 그 결과 축소 전의 5%의 범위에서 매칭됨을 확인하였다.

ABSTRACT

This paper relates 10% shrink from 0.13㎛ design for core devices as well as input and output (I/O) devices different from previous poly length shrink size only. We analyzed body effect with different channel length and doping profile simulation. After fixing the gate oxide module process, LDD implant conditions were optimized such as decoupled plasma nitridation of gate oxide, TEOS oxide 100Å before LDD implant and 22o tilt-angle(45o twist-angle) LDD implant respectively to match the spice DC parameters of pre-shrink and finally matched them within 5%.

키워드

LDD Implant, Ion Implant, Gate Oxide, Shrink, Matching
LDD 임플란트, 이온 주입, 게이트산화막, 축소, 매칭

Ⅰ. Introduction

The scaling trend becomes accelerated in process technology, but there are a lot of problems. To overcome this problems, the shrink technology has been adopted by many chip makers. The target is spice performance matching after shrink (normally 10%) to the performance of pre-shrink, which is very challenging. That is the reason why the shrink technologies have been related to core transistors only excluding input & output (I/O) transistors, because the I/O shrink is much more challenging[1]. The major challenging items are hot carrier injection (HCI) lifetime degradation and

* 전남대학교 전기및반도체공학과(msyc1103@hanmail.net, ferroksj@jnu.ac.kr)
** 교신저자 : 전남대학교 전기및반도체공학과(jyanghee@jnu.ac.kr)
접수일자 : 2014. 09. 01 심사(수정)일자 : 2014. 10. 20 게재확정일자 : 2014. 11. 10

flicker noise[2-3].

The previous shrink technologies targeted matching the performance in the same active width and 10% shrunk poly length only. This make it difficult to use the pre-shrink circuit as it is after 10% direct shrink, requiring the circuit modification for actual performance matching.

Different from the previous shrink technologies, this shrink technology shrinks both the core logic and I/O without exceptions. Shrink is 10% from 0.13μm technology and spice DC parameters should be matched to that of pre-shrink. Operation voltage for core logic is 1.2V and for I/O circuit is 3.3V. We found many barriers by the shrink in terms of process, devices and reliabilities.

First, there were special requirements to be improved for the existing pre-shrink 0.13μm technology such as gate oxide integrity (GOI) especially for flicker noise[4-5]. It can be improved that thin transistor using decoupled plasma nitridation(DPN) process as a thin gate oxide in stead of NO annealed gate oxide using RTO process.

Second, hot carrier injection (HCI) degradation for I/O transistors is most concerning part when shrink[6]. It can be improved that thick transistor (3.3V MOS) using additional liner oxide before LDD implant and the optimization of LDD implant.

In this paper, after fixed the fundamental process such as gate oxide and implant conditions, body effect analysis and DC parameter matching performance was evaluated.

Ⅱ. Experimental

There are a lot of barriers for shrink processes. For flicker noise improvement, decoupled plasma nitridation (DPN) as gate oxidation in stead of rapid thermal nitridation oxide (RTNO) can reduce the nitrogen in $Si-SiO_2$. The DPN process changes the nitrogen location from $Si-SiO_2$ to SiO_2-Poly-Si interface far from the $Si-SiO_2$ interface. The DPN process flow is as follows; oxidation using rapid temperature oxidation (RTO) and then nitridation using nitrogen plasma in DPN reactor and then rapid temperature anneal (RTA) with 1100℃. The detail condition is as follows; 200sccm N_2, 300W, 20mT, 90rpm of stage rotation, 25sec. If skip or reduce the RTA temperature, V_{th} is seriously unstable due to the plasma damage on oxide. The RTA is for the plasma damage curing.

To improve HCI lifetime, increase of effective channel length (L_{eff}) was tried using liner TEOS oxide of 680℃ CVD process before LDD implant and LDD implant tilt-angle reduction for IO transistors. By adding 100Å TEOS right before the LDD implant, the L_{eff} can be increases by that thickness for thick n- ,p-MOS transistor. The TEOS deposition temperature 680℃, thermal budget, doesn't affect the device performance. However, L_{eff} for p-MOS should be increased more, because the HCI lifetime margin is more narrower than n-MOS. For this, LDD implant tilt-angle, processed to minimize the channeling, was tried to reduce and optimum angle was determined considering E-field and L_{eff} by TCAD simulation. Tilt-angle of LDD implant was reduced for additional L_{eff} increase by changing from B3.0E13, 17KeV, 30° tilt-angle and 45° twist-angle, with quadrupole to B3.0E13, 17KeV, 22° tilt-angle and 45° twist-angle, with quadrupole, resulting in 15nm increase of L_{eff}. We evaluated DC parameter matching performance such as V_{th} roll off curve, I-V characteristics for all different channel width and length with 10% shrink[7-8].

Ⅲ. Results and Discussion

3.1 Body effect analysis

In case of I/O N-MOS without punch-preventive

implant, the body effect was not shown in short channel device as shown in Fig. 1.

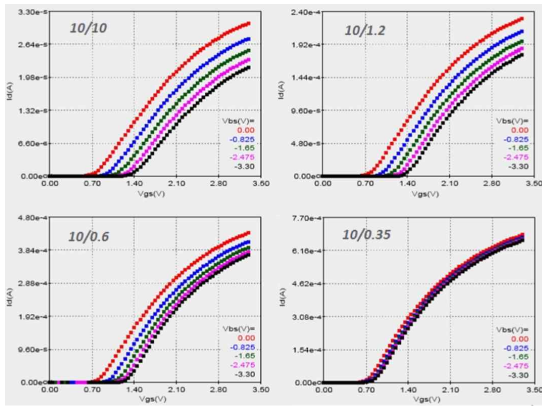


Fig. 1 Back bias effect with different poly channel length for I/O(3.3V) n-MOS transistor

So, if the space is too little to form depletion layer under the channel in short channel as shown TCAD simulation profile Fig. 2, the body effect can't be seen. In case of medium poly channel length as described in Fig. 1, body effect is very clear, due to enough space between source and drain [9].

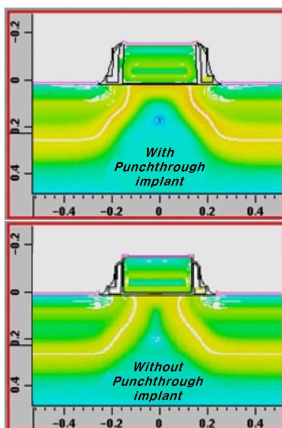


Fig. 2 TCAD simulation for doping profile of I/O(3.3V) n-MOS

The reason why the pre-shrink process has clear body-effect even in short channel is because it has punch-preventive implant that can make enough space between source and drain. If the space between source and drain is enough, the back bias can make a clear depletion, which shift the V_{th}. However, if there is no enough space, the depletion was not changed by the different back bias, resulting in no V_{th} shift even by the changes of back bias [10-11]. If use long channel devices, the narrow space between source and drain can be avoided and a clear back bias effect can be seen in Fig. 3. The back bias effect can affect the circuit performance normally in analog circuit such as band gap reference circuit. But, normally big transistor is used for the back biased transistor, resulting in no critical issue. And, if need target back bias for transistor, designer can adjust the transistor size based on the spice model.

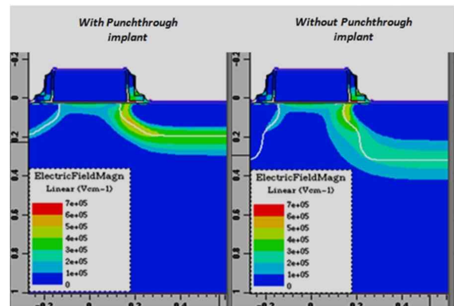
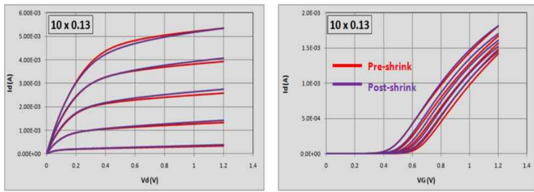


Fig. 3 TCAD simulation for E-field profile of I/O(3.3V) n-MOS

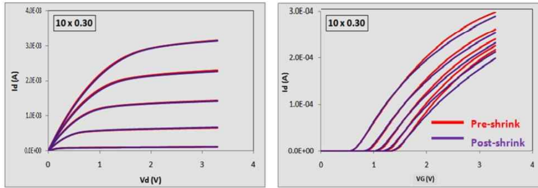
3.2 DC spice parameter matching performance

3.2.1 I-V curve

I_D-V_G curve was measured using HP4156. Bias condition was V_G sweep from 0V to VDD (1.2V for core and 3.3V for I/O) with 0.1V step with different back bias at 0.1V of V_D and I_{DS} current was measured. I_D-V_G curve of 10% shrink process is comparable to that of pre-shrink process within 5% as shown in Fig. 4 and Fig. 5.

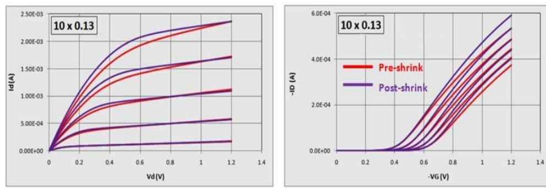


(a)

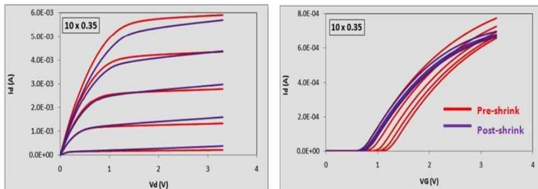


(b)

Fig. 4 I-V(I_D-V_D, I_D-V_G) curve for 1.2V transistor
(a) n-MOS and (b) p-MOS



(a)



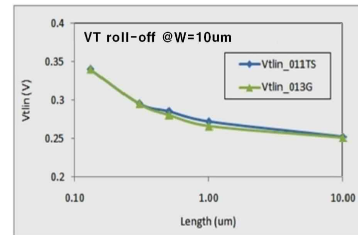
(b)

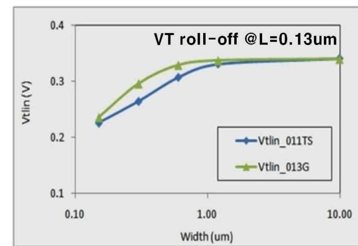
Fig. 5 I-V (I_D-V_D, I_D-V_G) curve for 3.3V I/O transistor
(a) n-MOS and (b) p-MOS

I_D-V_D curve was measured using HP4156. Bias condition was V_D sweep from 0V to VDD (1.2V for core and 3.3V for I/O) with 0.1V step with different V_G (0V~VDD) and I_{DS} current was measured. I_D-V_D curve of 10% shrink process is comparable to that of pre-shrink process within 5%. The reason for the mismatch of I_D-V_G for 3.3V n-MOS is well explained in the back bias effect.

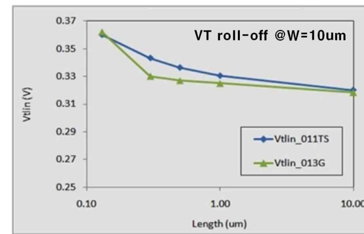
3.2.2 Threshold voltage (V_{th}) roll-off curve matching for each device

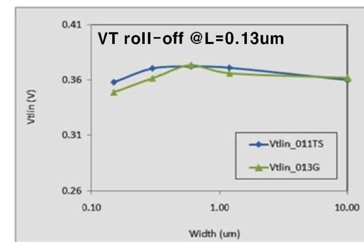
The V_{th} and I_{DSAT} roll-off curve with different length at 10μm width and with different width at short channel length was evaluated for all devices. The performance of the short channel effect and inverse narrow width effect was comparable to that of pre-shrink process as shown in Fig. 6 and Fig. 7.





(a)





(b)

Fig. 6 V_{th} roll-off curve with different gate length for 1.2V transistor
(a) n-MOS and (b) p-MOS

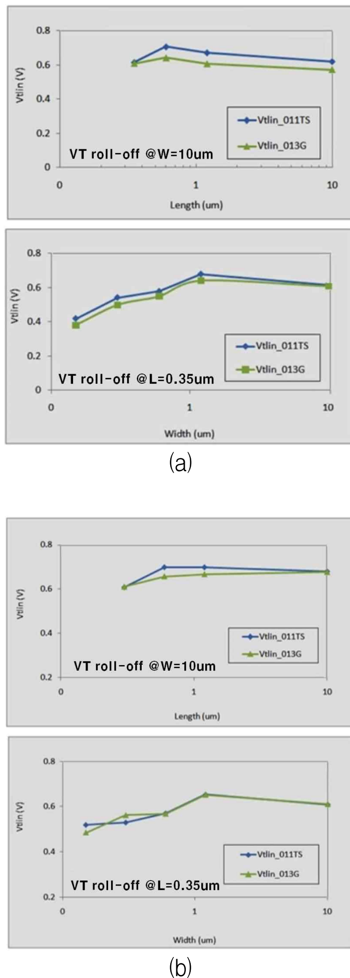


Fig. 7 V_{th} roll-off curve with different gate length for 3.3V I/O transistor
(a) n-MOS and (b) p-MOS

Ⅵ. Conclusions

In this paper, the matching performance of DC spice parameter investigated for the device of 10% shrink from 0.13μm technology. This shrink targets the spice DC parameters matching to pre-shrink in 10% shrunk active width and poly length size, different from previous poly length shrink size only. Decoupled plasma nitridation is used as gate oxidation for flicker noise according to the shrink, TEOS oxide before LDD implant and LDD implant optimization are applied to match the DC para-meters of pre-shrink and finally matched them within 5%.

References

[1] R. R. Troutman, "VLSI limitation from drain-induced barrier lowering," *IEEE Trans. Electron Devices*, vol. ED-26, no. 4, 1979, pp. 461-468.

[2] Y. Tsividis, "The Book," *IEEE, Solid-State Circuits Magazine*, vol. 6, no. 1, 2014, pp. 37-38.

[3] C. Hu, G. P. Li, E. Worley, and J. White, “Consideration of low-frequency noise in MO-SFET”s for analog performance,” *IEEE Electron Device Lett.*, vol. 17, no. 12, 1996, pp. 552 - 554.

[4] I. Bloom and Y. Nemirovsky, “1/f noise reduction of metal-oxide-semiconductor trans-istors by cycling from inversion to accum-ulation,” *Appl. Phys. Lett.*, vol. 58, no. 15, 1991, pp. 1664 - 1666.

[5] B. Dierickx and E. Simoen, “The decrease of ”random telegraph signal” noise in metal - oxide-semiconductor field-effect transistors when cycled from inversion to accumulation,” *J. Appl. Phys.*, vol. 71, no. 4, 1992, pp. 2028 - 2029.

[6] T. Kuroi, S. Shimizu, A. Furukawa, S. Komori, Y. Kawasaki, S. Kusunoki, Y. Okumura, M. Inuishi, N.Tsubouchi, and K. Horie, “Highly Reliable 0.15μm MOSFETs with Surface Pro-ximity Gettering (SPG) and Nitrided Oxide Spacer Using Nitrogen Implantation,” *1995 Symp. on VLSI Tech. Dig.* 1995, pp. 19-20.

[7] H. J. Chung, "5-TFT OLED Pixel Circuit Compensating Threshold Voltage Variation of p-channel Poly-Si TFTs," *J. of the Korea Institute of Electronic Communication Sciences*, vol. 9, no. 3, 2014, pp. 279-284.

[8] H. J. Chung, "A Voltage Programming AMOLED Pixel Circuit Compensating Threshold Voltage

Variation of n-channel Poly-Si TFTs," *J. of the Korea Institute of Electronic Communication Sciences,* vol. 8, no. 2, 2013, pp. 207-212.
[9] J. Wei-Han and B. Kan, "The Design and Realization of Basic nMOS Digital Devices," *Proc. of The National Conf. on Undergraduate Research(NCUR) 2004, Indiana University, Indianapolis, Indiana,* Apr. 15-17, 2004, pp. 1-7.
[10] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits 2nd ed. (1999).* New York: McGraw Hill, 1999.
[11] S.-Y. Mun, S.-J. Kang, and Y.-H. Joung, "A Study on the Hot Carrier Injection Improvement of I/O Transistor," *J. of the Korea Institute of Electronic Communication Sciences,* vol. 9, no. 8, 2014, pp. 847-852.

저자 소개

문성열(Seong-Yeol Mun)

1994년 경기대학교 물리학과졸업(공학사)
2006년 전남대학교 대학원 전기및반도체공학과 졸업(공학석사)
2011년 전남대학교 전기및반도체공학과(공학박사)
현재 Globalfoundries Ltd., USA, manager
※ 관심분야 : 소자 공정 개발

강성준(Seong-Jun Kang)

1989년 인하대학교 응용물리학과 졸업(공학사)
1994년 인하대학교 대학원 전자재료공학과 졸업(공학석사)
1999년 인하대학교 대학원 전자재료공학과 졸업(공학박사)
현재 전남대학교 전기및반도체공학과 교수
※ 관심분야 : 기능성박막, 반도체공정 및 재료

정양희(Yang-Hee Joung)

1983년 단국대학교 응용물리학과 졸업(공학사)
1985년 인하대학교 대학원 응용물리학과 졸업(공학석사)
1993년 인하대학교 대학원 전자재료공학과 졸업(공학박사)
1995년~현재 전남대학교 전기및반도체공학과 교수
※ 관심분야 : 반도체 공정 및 물성