JPE 14-6-16

http://dx.doi.org/10.6113/JPE.2014.14.6.1224
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Asymmetrical Pulse-Width-Modulated Full-Bridge Secondary Dual Resonance DC–DC Converter

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Abstract

A full-bridge secondary dual-resonant DC–DC converter using the asymmetrical pulse-width modulated (APWM) strategy is proposed in this paper. The proposed converter achieves zero-voltage switching for the power switches and zero-current switching for the rectifier diodes in the whole load range without the help of any auxiliary circuit. Given the use of the APWM strategy, a circulating current that exists in a traditional phase-shift full-bridge converter is eliminated. The voltage stress of secondary rectifier diodes in the proposed converter is also clamped to the output voltage. Thus, the existing voltage oscillation of diodes in traditional PSFB converters is eliminated. This paper presents the circuit configuration of the proposed converter and analyzes its operating principle. Experimental results of a 1 kW 385 V/48 V prototype are presented to verify the analysis results of the proposed converter.

Key words: APWM, PSFB converter, Secondary dual-resonance, Soft-switching technique

I. INTRODUCTION

The traditional phase-shifted full-bridge (PSFB) converter shown in Fig. 1(a) benefits from zero-voltage switching (ZVS) for all switches without the help of any auxiliary circuits [1], [2]. However, this PSFB converter suffers from a narrow ZVS range of lagging-leg switches under wide load variation, which severely affects its light load efficiency [2]. Given the resonance between transformer leakage inductance and parasitic junction capacitance of a rectifier diode, serious voltage spikes across the diode rectifier are generated [3], which increases the diode voltage rating and causes electromagnetic interference problems. Excessive circulating current in the primary side during the freewheeling interval also increases the primary side conduction and turn-off switching losses of the lagging-leg switches [4]-[6]. From the corresponding waveforms of a traditional PSFB converter shown in Fig. 1(b), duty losses exist in the traditional PSFB converter, which increase the turns ratio of the transformer and current stress in the diodes [2].

Manuscript received Apr. 30, 2014; accepted Aug. 22, 2014
Recommended for publication by Associate Editor Bor-Ren Lin.
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Many studies have attempted to overcome the said problems in a traditional PSFB converter [2], [4]-[21]. In order to extend the ZVS range and eliminate voltage spike of diode rectifier, additional auxiliary circuits are required [2], [4]-[6], [8]-[11], [14], which increase complexity of the converter and cause additional conduction losses.

A new PSFB converter proposed in [4] always operates at a maximum duty ratio of 50% by varying the primary turns of the transformer, thus eliminating the circulating current and decreasing primary-side conduction losses. The power rating for switches decreased and the efficiency improved in the input-series-connected FB converter proposed in [17], [18]. However, this technique increases the controller complexity.

The transformer secondary side resonance technique is proposed in [22]-[29] to achieve zero current switching (ZCS) for the diode. The ZCS for the output diode is achieved with the resonant tank in the secondary side, whereas the ZVS for switches is realized through the active clamp technique [22]-[28]. However, such resonant technique results in an increased current stress of power switches. A hybrid switching mode step-down resonant-PWM converter is proposed in [29] to decrease the current stress of the power switch. It operates in PWM mode when the switch is turned on, whereas it operates in resonant mode when the switch is turned off. This condition decreases the current stress of the power switch.

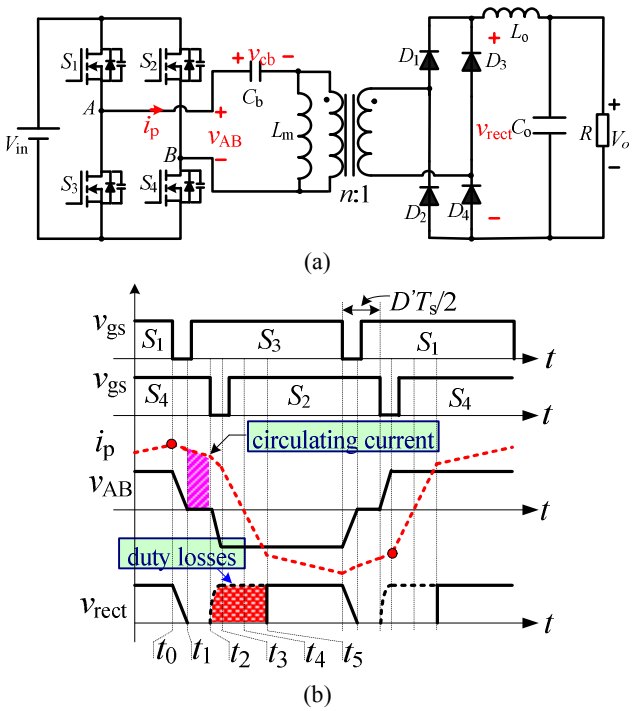


Fig. 1. (a) Traditional PSFB converter. (b) The corresponding waveforms.

This paper presents a full-bridge secondary dual-resonant (FB-SDR) DC–DC converter using the asymmetrical pulse width modulated (APWM) strategy, as shown in Fig. 2. A magnetizing inductor current is used in the proposed converter to achieve the ZVS for switches. The ZCS for the rectifier diodes is achieved because of the resonance between the leakage inductor and capacitor in the secondary side. Therefore, switching losses and diode reverse-recovery losses are eliminated. Circulating current losses that exist in traditional PSFB converters are largely eliminated because of the APWM strategy. Unlike traditional PSFB converters, the proposed converter can eliminate secondary voltage spikes and voltage oscillation across the rectifier diodes and clamp the diode voltage to the output voltage.

The circuit configuration and operation principle of the proposed converter are presented in Section II. The analysis results are provided in Section III. The performance of the proposed converter is verified by the experimental results of a 1 kW 385 V/48 V prototype in Section IV. The conclusion is presented in Section V.

II. Proposed Secondary Side Dual-Resonant Full Bridge Converter

A. Circuit Configuration

Fig. 2 shows the circuit configuration of the proposed converter. The proposed converter is composed of a full bridge configuration with a blocking capacitor C_b on the primary side, a resonant network that consists of a leakage inductor L_{lk},

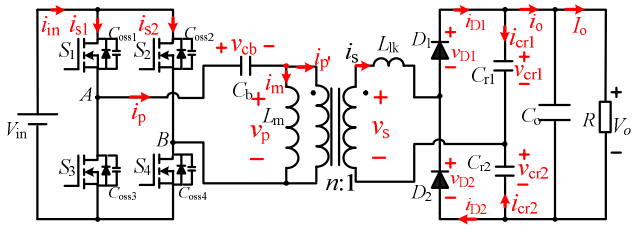


Fig. 2. Proposed FB-SDR converter.

capacitors C_{r1} and C_{r2} in the secondary side, output filter capacitor C_o, and load R. When the transformer secondary voltage v_S is positive, the leakage inductor L_{lk} and resonant capacitor C_{r1} constitute a resonant tank, capacitor voltage v_{cr1} increases, and capacitor voltage v_{cr2} decreases. When the transformer secondary voltage v_S is negative, the leakage inductor L_{lk} and resonant capacitor C_{r2} constitute a resonant tank, capacitor voltage v_{cr1} decreases, and capacitor voltage v_{cr2} increases.

B. Operating Principle

The following assumptions are made to simplify the analysis of the proposed converter: power switches S_1, S_2, S_3, and S_4 are ideal except for their anti-paralleled diodes and output capacitances; the output capacitances of switches S_1, S_2, S_3, and S_4 are equal, *i.e.* $C_{oss}= C_{oss1}= C_{oss2}= C_{oss3}=C_{oss4}$; capacitors C_b and C_o are large enough that voltages V_{cb} and V_o can be considered constants in a switching cycle; the transformer is modeled as an equivalent circuit composed of a magnetizing inductor L_m, leakage inductor L_{lk}, and an ideal transformer with a turns ratio of n:1, with $L_m >> n^2L_{lk}$. The converter operates in a steady state and $C_{r1} = C_{r2} = C_r$.

Fig. 3 illustrates key waveforms of the proposed converter in a switching cycle. The operation of power switches S_1 and S_4, as well as S_2 and S_3, are the same. Switches S_1 and S_3 are asymmetrical and complementary to the duty ratio D of power switch S_1. Dead time exists between the on/off states of switches S_1, S_3 and S_2, S_4 to ensure safe operation of the power switches in the inverter leg. The proposed converter has seven operational modes in a switching cycle with their corresponding equivalent circuits in each operation mode as shown in Fig. 4.

Mode 1 ***[$t_0 \sim t_1$]***: At $t = t_0$, as $i_P(t)$ is negative, the anti-paralleled diodes of switches S_1 and S_4 are conducted to provide the flowing path for $i_P(t)$. The magnetizing inductor current $i_m(t)$ increases linearly from negative with the current slope of $(V_{in} - V_{cb})/L_m$. As v_s is positive, diode D_1 is turned on, and leakage inductor L_{lk} and capacitor C_{r1} are resonant. Thus, the current through the transformer secondary and voltage across the resonant capacitor C_{r1} increase, whereas the voltage across resonant capacitor C_{r2} decreases. $i_m(t)$ can be expressed as follows:

$$i_m(t) = i_m(t_0) + \frac{V_{in} - V_{cb}}{L_m}(t - t_0) \quad (1)$$

where $i_m(t_0)$ is negative as shown in Fig. 3.

The following equation can be derived from the secondary side of the transformer:

$$L_{lk}\frac{di_S(t)}{dt} = \frac{V_{in} - V_{cb}}{n} - v_{Cr1}(t) \quad (2)$$

$$\begin{aligned} i_S(t) &= i_{cr1}(t) + i_{cr2}(t) = C_r\frac{dv_{Cr1}(t)}{dt} - C_r\frac{d(V_o - v_{Cr1}(t))}{dt} \\ &= 2C_r\frac{dv_{Cr1}(t)}{dt} \end{aligned} \quad (3)$$

From Equations (2) and (3), the following can be derived:

$$\begin{aligned} i_S(t) &= \frac{(V_{in} - V_{cb})/n - v_{cr1}(t_0)}{Z_r}\sin[\omega_r(t - t_0)] \\ &= I_{sp1}\sin[\omega_r(t - t_0)] \end{aligned} \quad (4)$$

$$\begin{aligned} v_{cr1}(t) &= (V_{in} - V_{cb})/n \\ &\quad -[(V_{in} - V_{cb})/n - v_{cr1}(t_0)]\cos[\omega_r(t - t_0)] \end{aligned} \quad (5)$$

where $\omega_r = 1/\sqrt{2LlkCr}$ is the resonant angle frequency and $Z_r = \sqrt{Llk/(2Cr)}$ is the characteristic impedance, $I_{sp1} = [(V_{in} - V_{cb})/n - v_{cr1}(t_0)]/Z_r$.

$i_P(t)$ and diode current $i_{D1}(t)$ can be expressed as follows:

$$i_P(t) = i_m(t) + \frac{i_S(t)}{n} \quad , \quad i_{D1}(t) = i_S(t) \quad (6)$$

Mode 2 ***[t_1 ~t_2]***: As the anti-paralleled diodes of S_1 and S_4 are conducted in mode 1, the zero voltage turn-on of switches S_1 and S_4 are guaranteed. At $t = t_1$, $i_P(t)$ increases to zero and switches S_1 and S_4 are turned on. $i_m(t)$ increases linearly, diode D_1 continues to conduct, and the resonant tank remains resonant. All the circuit equations in this operation mode are the same as those in operation mode 1.

Mode 3 ***[t_2 ~t_3]***: At $t = t_2$, switches S_1 and S_4 are turned off, and $i_P(t)$ charges the output capacitors of switches S_1 and S_4 as well as discharges the output capacitors of switches S_3 and S_2. The voltages across S_1 to S_4 can be expressed as follows:

$$v_{ds1}(t) = v_{ds4}(t) = Z_1 \cdot I_{p1}\sin[\omega_1(t - t_0)] \quad (7a)$$

$$v_{ds2}(t) = v_{ds3}(t) = V_{in} - Z_1 \cdot I_{p1}\sin[\omega_1(t - t_0)] \quad (7b)$$

where I_{p1} represents the transformer primary-side current $i_p(t)$ at $t = t_2$ as shown in Fig. 3. $Z_1 = 1/(\omega_1 C_{oss}) = 1/(2\pi f_s C_{oss})$, where $\omega_1 = 1/2\sqrt{L_{kp}C_{oss}}$, f_s is the switching frequency, and $C_{oss} = C_{oss1} = C_{oss2} = C_{oss3} = C_{oss4}$. Note that L_{kp} is the primary-side leakage inductor of the transformer (i.e., $L_{kp} = n^2 L_{lk}$).

From Equations (7a) and (7b), the time interval T_{c1} for the ZVS commutation of S_1 to S_4 can be expressed as follows:

$$T_{c1} = \frac{1}{\omega_1}\cdot\arcsin\left(\frac{V_{in}}{Z_1 I_{p1}}\right) \le t_{2-3} \quad (8)$$

where $t_{2\text{-}3}$ is the dead time of the gate signals of S_1/S_3 and S_2/S_4.

Mode 4 ***[t_3 ~t_4]***: After the resonance between capacitors

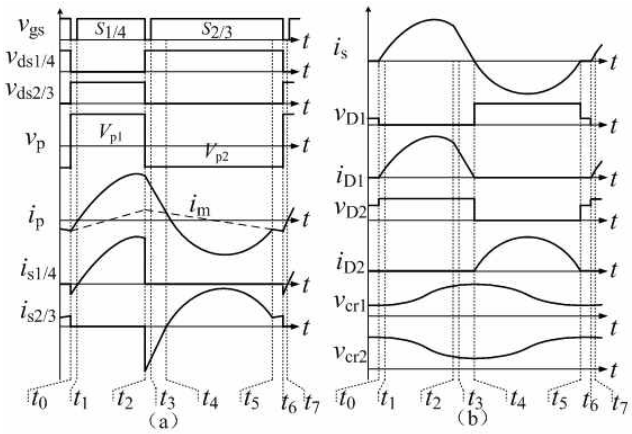


Fig. 3. Key waveforms of the proposed converter.

C_{oss1} to C_{oss4} and primary side leakage inductor L_{kp}, the anti-paralleled diodes of S_2 and S_3 are forward biased. The gates of S_2 and S_3 are triggered during this time interval, and the ZVS for switches S_2 and S_3 are achieved. $v_p(t)$ is negative (i.e., $v_p(t) = V_p = -V_{in} - V_{cb}$). $i_m(t)$ decreases linearly from positive to negative with the slope of $-(V_{in} + V_{cb})/L_m$. The transformer secondary voltage is $v_s(t) = v_p(t)/n = -(V_{in} + V_{cb})/n$.

The following equation can be derived from the secondary side of the transformer:

$$L_{lk}\frac{di_s(t)}{dt} = -(V_{in} + V_{cb})/n - v_{cr1}(t) \quad (9)$$

$$i_s(t) = i_{cr1}(t) + i_{cr2}(t) = 2i_{cr1}(t) = 2C_{r1}\frac{dv_{cr1}(t)}{dt} \quad (10)$$

Solving Equations (9) and (10) obtains the following:

$$i_s(t) = \frac{-(V_{in} + V_{cb})/n - v_{cr1}(t_3)}{Z_r}\sin[\omega_r(t - t_3)] + i_s(t_3)\cos\omega_r(t - t_3) \quad (11)$$

$$\begin{aligned} v_{cr1}(t) &= -(V_{in} + V_{cb})/n \\ &\quad + [(V_{in} + V_{cb})/n + v_{cr1}(t_3)]\cos[\omega_r(t - t_3)] \\ &\quad + [2(V_{in} - V_{cb})/n - 2v_{cr1}(t_0)]\sin(\omega_r DT_s)\sin[\omega_r(t - t_3)] \end{aligned} \quad (12)$$

Currents $i_P(t)$ and $i_{D1}(t)$ can be expressed as follows:

$$i_P(t) = i_m(t) + \frac{i_S(t)}{n} \quad , \quad i_{D1}(t) = i_S(t) \quad (13)$$

Mode 5 ***[t_4 ~t_5]***: As the anti-paralleled diodes of S_2 and S_3 are conducted, the zero voltage turn-on for switches S_2 and S_3 is guaranteed. At $t = t_4$, $i_P(t)$ decreases to zero, switches S_2 and S_3 are turned on, and $i_{D1}(t)$ decreases to zero. Diode D_2 is conducted to provide the current flowing path with leakage inductor L_{lk} and capacitor C_{r2}.

The circuit equation in this mode can be expressed as follows:

$$L_{lk}\frac{di_s(t)}{dt} = -(V_{in} + V_{cb})/n - v_{cr2}(t) \quad (14)$$

$$i_s(t) = i_{cr1}(t) + i_{cr2}(t) = -2i_{cr2}(t) = -2C_{r2}\frac{dv_{cr2}(t)}{dt} \quad (15)$$

Thus,

$$i_s(t) = -\frac{(V_{in}+V_{cb})/n + v_{cr2}(t_4)}{Z_r}\sin[\omega_r(t-t_4)] = -I_{sp2}\sin[\omega_r(t-t_4)] \quad (16)$$

$$v_{cr2}(t) = (V_{in}+V_{cb})/n - [(V_{in}+V_{cb})/n + v_{cr2}(t_4)]\cos[\omega_r(t-t_4)] \quad (17)$$

Currents $i_P(t)$ and $i_{D2}(t)$ can be expressed as follows:

$$i_P(t) = i_m(t) + \frac{i_S(t)}{n} \quad , \quad i_{D2}(t) = -i_S(t) \quad (18)$$

When $i_{D2}(t)$ is equal to zero, diode D_2 is turned off and the ZCS for diode D_2 is achieved.

Mode 6 ***[t_5 ~ t_6]***: The ZCS condition of diodes D_2 is achieved at the beginning of this mode, which eliminates the reverse recovery loss of diode D_2. The transformer secondary side in this mode is separated from the primary side, no power is transferred from the primary to the secondary side (Fig. 4*f*), and $i_P(t)$ decreases.

Mode 7 ***[t_6 ~ t_7]***: At $t = t_6$, switches S_2 and S_3 are turned off, and $i_P(t)$ charges the output capacitors of switches S_2 and S_3 and discharges the output capacitors of switches S_1 and S_4. The voltages across S_1 to S_4 in this mode are written as follows:

$$v_{ds2}(t) = v_{ds3}(t) = Z_2 \cdot I_{p2}\sin[\omega_1(t-t_0)] \quad (19a)$$

$$v_{ds1}(t) = v_{ds4}(t) = V_{in} - Z_2 \cdot I_{p2}\sin[\omega_1(t-t_0)] \quad (19b)$$

where I_{p2} is the transformer primary side current $i_p(t)$ at $t = t_6$. $Z_2 = 1/(\omega C_{oss}) = 1/(2\pi f_s C_{oss})$, $\omega_1 = 1/2\sqrt{L_{kp}C_{oss}}$.

From Equation (19), the time interval T_{c2} for the ZVS commutation of S_1 to S_4 can be expressed as follows:

$$T_{c2} = \frac{1}{\omega_1}\cdot\arcsin\left(\frac{V_{in}}{Z_2 I_{p2}}\right) \le t_{6-7} \quad (20)$$

where $t_{6\text{-}7}$ represents the dead time of the gate signals for S_1/S_3 and S_2/S_4 .

When the output capacitors of power switches S_1 and S_4 are charged to the input voltage V_{in}, the anti-paralleled diodes of switches S_1 and S_4 are conducted and the next switching cycle begins.

III. Characteristics Analysis

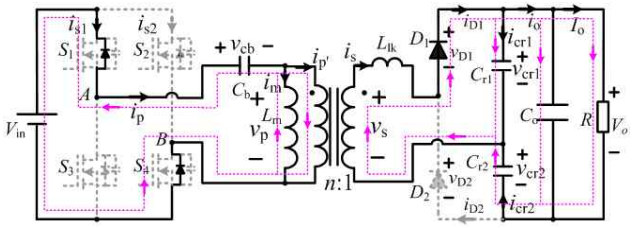
A. Voltage Transfer Gain

Assume that the dead times in modes 3 and 7 are short enough that they can be neglected. The voltage across the transformer primary side in modes 1 and 2 is V_{p1} (i.e., $V_{p1} = V_{in} - V_{cb}$). The voltage across the transformer primary side in modes 4, 5, and 6 is V_{p2}, i.e., $V_{p2} = -V_{in} - V_{cb}$, where V_{cb} is the average voltage across the blocking capacitor C_b.

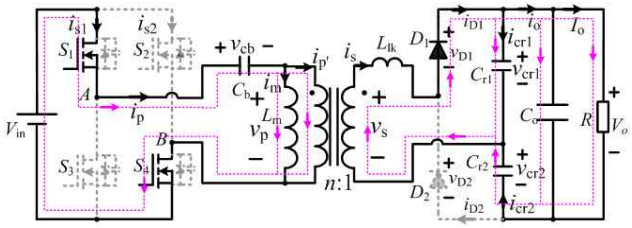
Applying volt-second balance to the magnetizing inductor L_m in steady state ensures that the average voltage across the clamp capacitor is expressed as follows:

$$V_{cb} = (2D-1)V_{in} \quad (21)$$

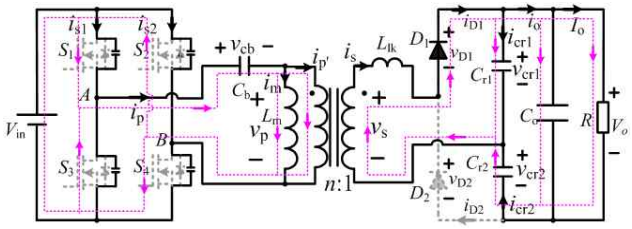
The transformer primary side voltage can then be obtained



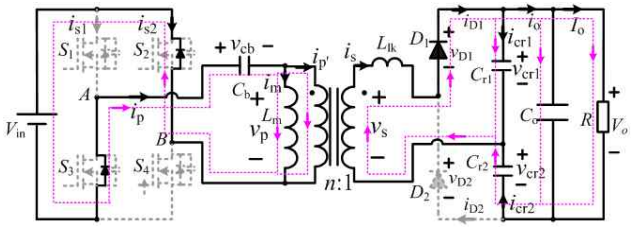
(a) *Mode* 1 [t_0~t_1].



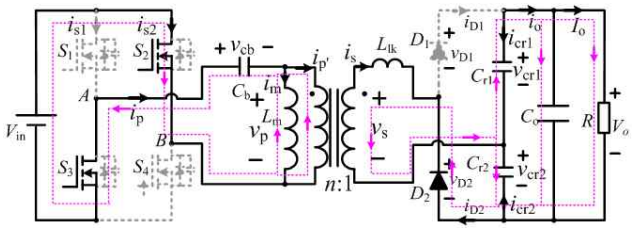
(b) *Mode* 2 [t_1~t_2].



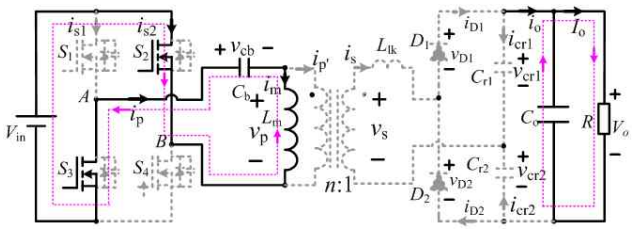
(c) *Mode* 3 [t_2~t_3].



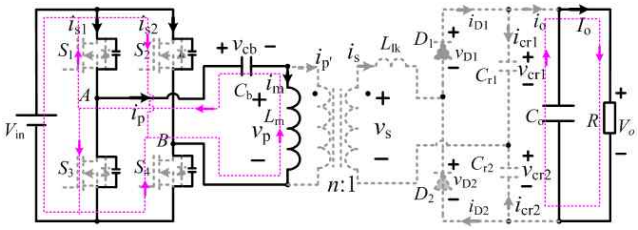
(d) *Mode* 4 [t_3~t_4].



(e) *Mode* 5 [t_4~t_5].



(f) *Mode* 6 [t_5~t_6].



(g) *Mode* 7 [t_6~t_7].

Fig. 4. Operational modes of the proposed converter.

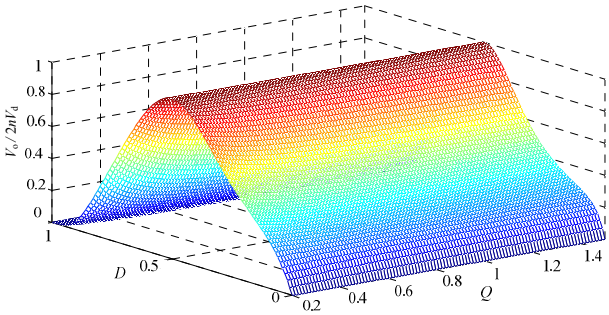


Fig. 5. Voltage gain of the proposed converter (F = 1).

as follows:

$$V_{p1} = 2(1-D)V_{in}\ ,\quad V_{p2} = -2DV_{in} \tag{22}$$

The average input power in a switching cycle is equal to the output power. Therefore,

$$\frac{V_o^2}{R} = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} v_{in}\cdot i_{in}(t)\mathrm{d}t = \frac{1}{T_s}[\int_{t_0}^{t_2}\frac{V_{p1}}{n}i_{s1}(t)\mathrm{d}t + \int_{t_2}^{t_6}\frac{-V_{p2}}{n}i_{s2}(t)\mathrm{d}t] \tag{23}$$

As the transformer magnetizing inductor is large enough that the current ripple flowing through L_m is close to zero, the current ripple of i_{Lm} can be neglected. From Equations (4), (6), (11), (13), (16), and (18), Equation (23) can be solved to obtain the following:

$$(\frac{nV_o}{2V_{in}})^2 + f_1(Q,D)(\frac{nV_o}{2V_{in}}) + f_2(Q,D) = 0 \tag{24}$$

where

$$\begin{aligned} f_1(Q,D) \approx\ & -D - 2\pi FQ(1-D)(\frac{1}{4\pi FQ}-1)[1-\cos(2\pi FD)] \\ & -2\pi FQD(\frac{1}{4\pi FQ}-1)\cos(2\pi FD)\times \\ & [1-\cos[2\pi F(0.5-D)]] - 2\pi FQ(\frac{1}{4\pi FQ}-1)\times \\ & \sin(2\pi FD)\sin[2\pi F(0.5-D)] \end{aligned} \tag{25}$$

$$\begin{aligned} f_2(Q,D) \approx\ & -2\pi FQ(1-D)[1-\cos(2\pi FD)] + 2\times \\ & \pi FQD[1-\cos(2\pi F(0.5-D))][1- \\ & \cos(2\pi FD)] - 2\pi FQD\sin(2\pi FD)\times \\ & \sin[2\pi F(0.5-D)] \end{aligned} \tag{26}$$

with $F = f_r/f_s$, $Q = 8\omega_r L_{lk}/R$.

Voltage transfer gain can then be derived as follows:

$$\begin{aligned} M(F,Q,D) &= \frac{nV_o}{2V_{in}} \\ &= 0.5(-f_1(Q,D) + \sqrt{f_1(Q,D)^2 - 4f_2(Q,D)}) \end{aligned} \tag{27}$$

Fig. 5 shows the voltage gain of the proposed converter at F = 1. The maximum voltage gain can be achieved when D = 0.5.

A. Comparison between the Proposed and Traditional PSFB Converters

The traditional PSFB converter shown in Fig. 1(a) is compared with the proposed converter shown in Fig. 2 in this section. The output inductor current is assumed to be a constant current source in the traditional PSFB converter to simplify the analysis. Figs. 1(b) and 3 show the key operating waveform of these two converters.

Fig. 1(b) reveals that when switch S_1 is turned off, S_3 and S_4 are turned on simultaneously. Thus, a circulating current exists in the traditional PSFB converter, which results in additional conduction losses as shown in the shadow area in Fig. 1(b). Fig. 3 shows that when switch S_1 is turned off, S_2 and S_3 are turned on simultaneously. The freewheeling of the primary magnetizing inductor current in a traditional PSFB converter is eliminated in the proposed converter. A small magnetizing inductor is required to achieve a wide ZVS range for all switches in the traditional PSFB converter, which results in a large current ripple and leads to additional conduction losses. It will also lose the ZVS for switches S_2 and S_4 at a light load because of insufficient energy fed by the transformer leakage inductor. However, the proposed converter uses the energy fed by magnetizing inductor L_m to achieve the ZVS for all the switches. Thus, enough energy is available for the ZVS operation over the full load range.

B. ZVS Condition

As enough energy is fed by the magnetizing inductor current and output current, the ZVS operation for switches S_2 and S_3 can be easily achieved over a wide load range (Fig. 4c). Fig. 4(g) shows that the ZVS for switches S_1 and S_4 can be achieved with energy fed by magnetizing inductor L_m. Thus, the ZVS condition for the switches in dead time t_{dead} can be expressed as follows:

$$|i_m(t_6)| > \frac{2C_{oss}V_{in}}{t_{dead}} \tag{28}$$

From the key waveform of the proposed converter, $i_m(t_6)$ can be expressed as follows:

$$i_m(t_6) = -\frac{1}{2}\Delta I_m = \frac{D(1-D)V_{in}T_s}{L_m} \tag{29}$$

Thus:

$$L_m < \frac{D(1-D)t_{dead}}{2C_{oss}f_s} \tag{30}$$

If Equation (30) is satisfied, all the switches in the proposed converter will turn on with the ZVS over full load conditions.

C. Design of Switches S_1 to S_4 and Diodes D_1 to D_2

Fig. 2 shows that the voltage stresses of all switches are V_{in} and the voltage of diodes D_1 and D_2 are clamped to the output voltage V_o. The average current that flows through diodes D_1, D_2 in a switching cycle is equal to the output current as follows:

$$I_{D1.avg}=I_{D2.avg}=I_o \tag{31}$$

Then,

$$I_o \approx \frac{1}{T_s}\int_{t_0}^{t_2} I_{sp1}\sin\omega_r(t-t_0)\mathrm{d}t \tag{32a}$$

$$I_o=\frac{1}{T_s}\int_{t_4}^{t_5} I_{sp2}\sin\omega_r(t-t_4)\mathrm{d}t \tag{32b}$$

From Equation (32), the current stress of diodes D_1 and D_2 can be obtained as follows:

$$I_{D1.peak}=I_{sp1}\approx\frac{I_oT_s\omega_r}{1-\cos(2\pi FD)} \tag{33a}$$

$$I_{D2.peak}=I_{sp2}=\frac{I_oT_s\omega_r}{2} \tag{33b}$$

D. Design of Resonant Tank (L_{lks} and C_{r1}, C_{r2})

Fig. 6 shows the key current waveforms of the proposed converter with different resonant frequencies. As shown in Fig. 6, when $T_r/2 > DT_s$, where T_r is the resonant period and T_s is the switch period, the turn-off currents of switches S_1 and S_4 decrease and the zero-current turn-off for the diode rectifier can be achieved. This condition lowers the turn-off loss of switches S_1 and S_4 and reverse recovery loss of the diode rectifier. However, the peak current of switches S_1 and S_4 as well as the conduction loss increase. When $T_r/2 > (1 - D)T_s$, the ZCS for the diode rectifier cannot be achieved and the turn-off current of switches S_1 and S_4 also increases. This condition increases the reverse recovery loss of the diode rectifier and turn-off loss of switches S_1 and S_4. Therefore, having $T_r/2 > DT_s$ and $T_r/2 > (1 - D)T_s$ is not preferred. Consider the tradeoff between the reverse recovery loss of the diode rectifier and turn-off loss of switches S_1 and S_4, T_r should be designed such that $DT_s < T_r/2 < (1 - D)T_s$. C_r can then be obtained according to $T_r = 2\pi\sqrt{2LlksCr}$.

IV. Experimental Results

Experimental studies of the proposed converter have been performed to verify the above analysis results of the following converter parameters:

1) input voltage V_{in} = 385 V;
2) output voltage V_o = 48 V;
3) maximum output power P_o = 1 kW;
4) switching frequency f_s = 50 kHz.

With these parameters, the maximum output current is determined as I_o = 20.8 A. f_r is designed such that $f_s/[2(1 - D)] \le f_r < f_s/(2D)$. From the voltage gain given by Equation (27) and considering the dead time, the duty cycle D = 0.45 is designed. TDK EE55/21 core is used for the transformer design. The primary and secondary turns of the transformer are n_p = 38T and n_s = 3T. According to Equation (30), the magnetizing inductance L_m = 1010 μH is designed to ensure the ZVS condition for all switches over the whole load conditions. The secondary leakage inductance of the transformer is L_{lk} = 1.29 μH. According to the condition $f_s/[2(1 - D)] \le f_r < f_s/(2D)$, the resonant capacitor is designed as C_r = 4 μF and the resonant frequency is $f_r = 1/2\pi\sqrt{2L_{lk}C_r}$ = 51.4 kHz. The blocking capacitor C_b is added to set the average current that flows through primary magnetizing inductor to zero, thereby avoiding transformer saturation. Notably, C_b does not participate in resonance with L_m because the resonant frequency $f_m(f_m = 1/2\pi\sqrt{2L_mC_b})$ of capacitor C_b and magnetizing inductance L_m is much lower than the switching frequency f_s. $f_m = (\frac{1}{5} \sim \frac{1}{10})f_s$ is generally selected. Thus, C_b = 1 μF is designed in the experimental circuit. The dead time of switches S_1/S_3 and S_2/S_4 is selected as 300 ns in the experimental circuit according to Equations (8) and (20). The ZVS operation for switches is fed by a magnetizing inductor current and output current. Thus, the ZVS operation can be easily achieved over a wide load range. The parameters of passive components and semiconductors are shown in Fig. 7 with the circuit parameters given in Table I.

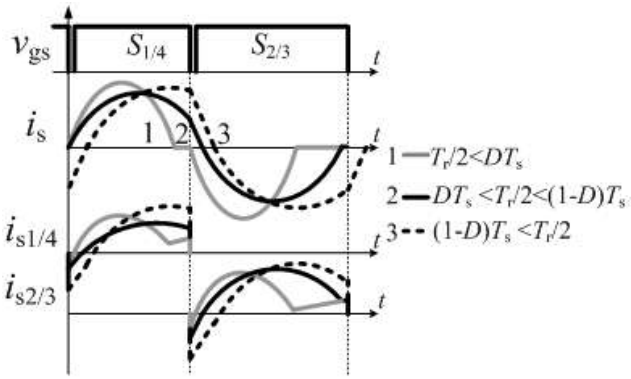


Fig. 6. Key current waveforms of the proposed converter under different T_r.

A. Experimental Results

Fig. 8 shows key waveforms of the proposed converter at a nominal input voltage (i.e., 385 V) and under a full load of 20.8 A. All measured waveforms in the figure closely follow the theoretical waveforms described in Fig. 3. Figs. 8(d) and 8(e) also show that the secondary diode voltages $v_{D1}(t)$ and $v_{D2}(t)$ have no voltage overshoot and oscillation. The ZCS for diodes D_1 and D_2 can also be achieved. Fig. 9 shows the switch voltage and switch current of the proposed converter at full and 10% loads, respectively. Fig. 9 shows that all the switches in the proposed converter are turned on with the ZVS over full load conditions. Unlike PSFB converters, the circulating current and turn-off switching losses are

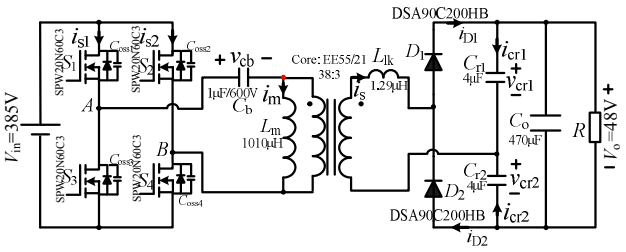
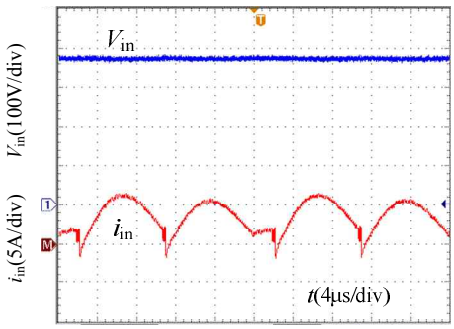


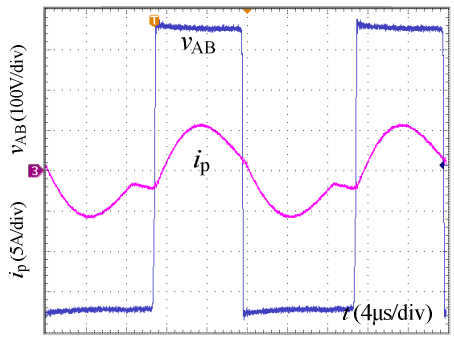
Fig. 7. Laboratory prototype circuit of the proposed converter.

TABLE I
PARAMETERS OF THE PROPOSED CONVERTER

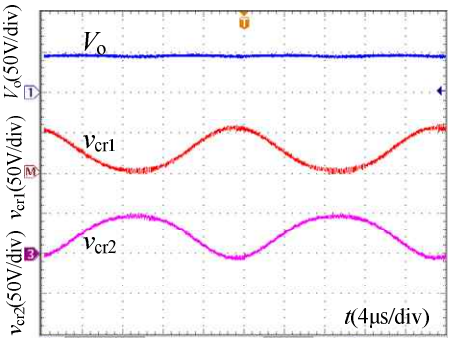
Components	Parameters
Switches (S_1–S_4)	SPW20N60C3 (20 A, 600 V)
Diodes (D_1–D_2)	DSA90C200HB (2×45 A, 200 V)
Main Transformer (T)	Core: EE55/21 PC40 Turn Ratio: 38 : 3 *Magnetizing inductance* L_m: 1010 μH Secondary leakage L_{lk}: 1.29 μH
Blocking Capacitor (C_b)	1 μF/600 V
Output Capacitor (C_o)	470 μF/100 V
Resonant Capacitor (C_{r1}–C_{r2})	4 μF



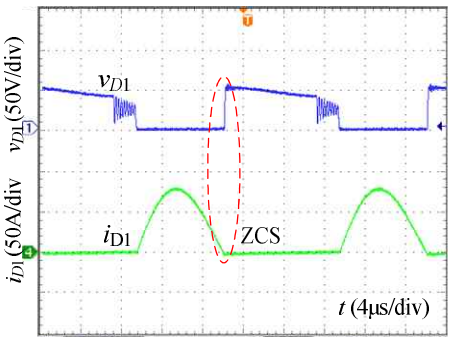
(a)



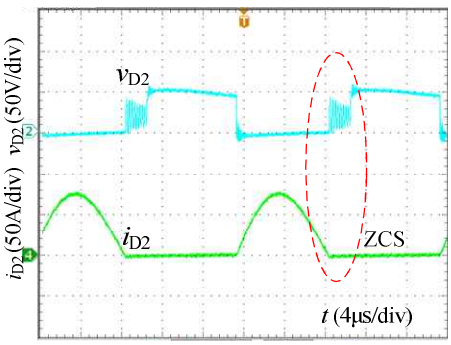
(b)



(c)



(d)



(e)

Fig. 8. Key experimental waveforms of the proposed converter at a full load of 20 A. (a) V_{in} and $i_{in}(t)$; (b) $v_{AB}(t)$ and primary current $i_p(t)$; (c) V_o, $v_{Cr1}(t)$, and $v_{cr2}(t)$; (d) $v_{D1}(t)$ and $i_{D1}(t)$; (e) $v_{D2}(t)$ and $i_{D2}(t)$.

decreased.

B. *Efficiency*

Fig. 10 shows the efficiency at an input voltage of 385 V. The proposed converter has higher efficiency than a PSFB converter, especially under light load conditions. At light loads, the ZVS operation of traditional PSFB converter switches is difficult to achieve. The efficiency improvement of the proposed converter is achieved because of the ZVS operation over a whole load range as well as decreased circulating current and turn-off switching losses. Without secondary-voltage overshoot and oscillation, a low voltage-rating diode can be used, which also contributes to the efficiency improvement.

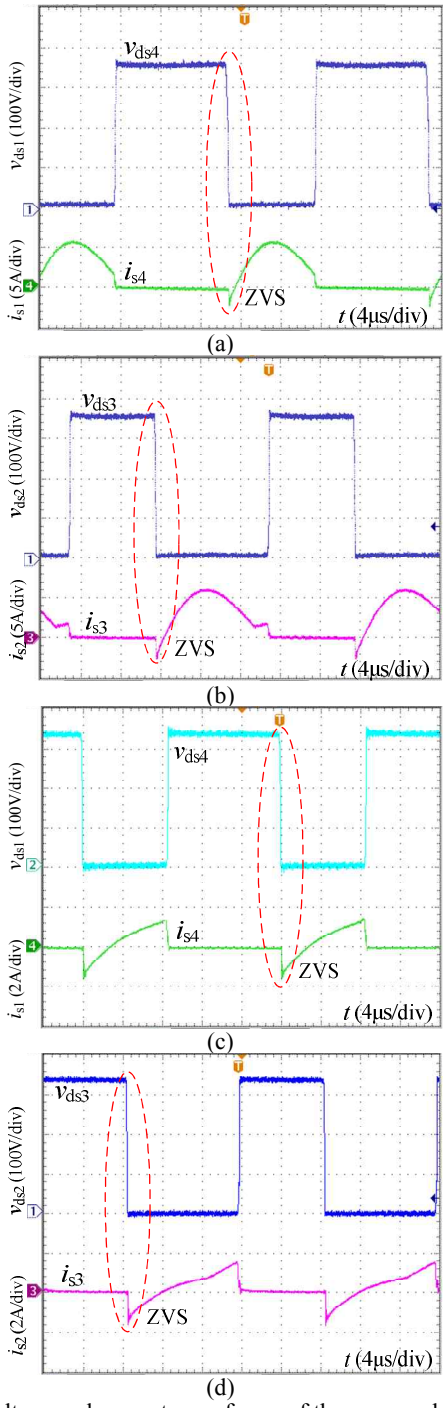


Fig. 9. Voltage and current waveforms of the proposed converter: (a) and (b): at full load; (c) and (d): at 10% of the full load.

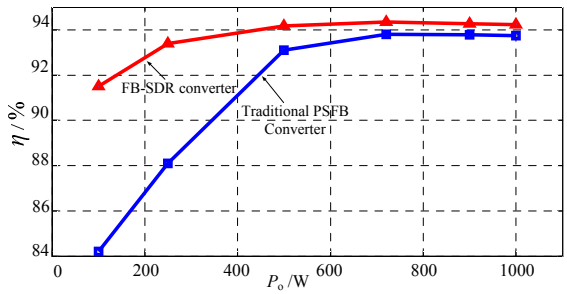


Fig. 10. Efficiency of the proposed converter.

IV. Conclusions

This paper presents an FB-SDR DC–DC converter that solves the drawbacks of PSFB converters, such as a narrow ZVS range against load variation, large circulating current, and serious secondary-voltage overshoot and oscillation. The theoretical analysis results show the advantage of the proposed converter over a traditional PSFB converter. The experiment results of a prototype converter verify the results of the theoretical analysis. However, given that the APWM strategy obtains the current stress of the switches, the proposed converter is available for applications in a narrow input voltage range and is also applicable to high-voltage applications such as high-voltage battery chargers (200 V–400 V).

Acknowledgment

This research is supported by the National Natural Science Foundation of China under grant no. 51177140, the Fundamental Research Funds for the Central Universities under project number SWJTU11CX029, and the 2014 Doctoral Innovation Funds of Southwest Jiaotong University.

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