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Quasi-Fixed-Frequency Hysteresis Current Tracking Control Strategy for Modular Multilevel Converters

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Abstract

This study proposes a quasi-fixed-frequency hysteresis current tracking control strategy for modular multilevel converters (MMCs) on the basis of voltage partition principle. First, by monitoring the grid voltage and the deviation between the output and reference currents, the output voltage is determined, thus prompting the output current to quickly and efficiently track the given current. Second, the voltages of the upper/lower capacitor of the arm and the voltages between the upper and lower arms are balanced by combining these arms with virtual loop mapping and arm voltage balance control, respectively. In particular, the proposed method is designed for any level and number of sub-modules. The validity of the proposed method is verified by simulations and experimental results of a five-level MMC prototype.

Key words: Dynamic voltage balance, Modular multilevel converter (MMC), Quasi-fixed-frequency hysteresis current tracking control, Virtual loop mapping

I. INTRODUCTION

Modular multilevel converter (MMC) is an innovative multilevel technology that was first used in a high voltage direct current (HVDC) transmission project in 2010 [1]. Compared with conventional multilevel topologies, MMC offers several advantages, including low switching frequency, low harmonic, and favorable redundancy. Also, as a new topology based on double-star chopper cell, MMC presents numerous desirable features, such as adaptability to high -voltage and high-power applications, excellent four-quadrant performance, and modular structure and redundant design [2], [3].

To fully utilize the favorable features of MMC, considerable effort has been exerted to extend the applications of MMC from HVDC [4]-[6] to various fields, including high-power motor drives [7], medium-voltage STATCOM [8], [9], and renewable energy generation [10]. However, only a few reports have been published on MMC for active power filters (APFs). As a type of static power converter, APF is normally controlled to compensate for the current harmonics drained from non-linear loads, reactive power, and imbalances of load terminals [11]. The dynamic performance of APF essential and largely depends on two factors, namely, real-time harmonic detection and rapid output current response. The former has been efficiently solved by instantaneous power theory, whereas the latter still requires sophisticated modulation methods.

This specific challenge has been addressed in the related literature with the implementation of several advanced modulation methods for APF. These methods include the nearest level modulation (NLM) [12], phase-shifted PWM modulation (PSPWM) [13] and phase disposition PWM modulation (PDPWM) [14]. Nevertheless, NLM has limited applications because it cannot be used for multilevel converters with below 21 levels [15]. Meanwhile, PSPWM and PDPWM exhibit good performances in low-level converters, but require additional PI controllers to transfer the current reference to the output voltage, which may reduce the robustness of the system [16]. Moreover, these three methods have other disadvantages, including overshooting in current errors, sub-harmonic components in the current, limiting cycle oscillations, and non-optimum switching vector selection [17].

Hysteresis current tracking control has an inherent

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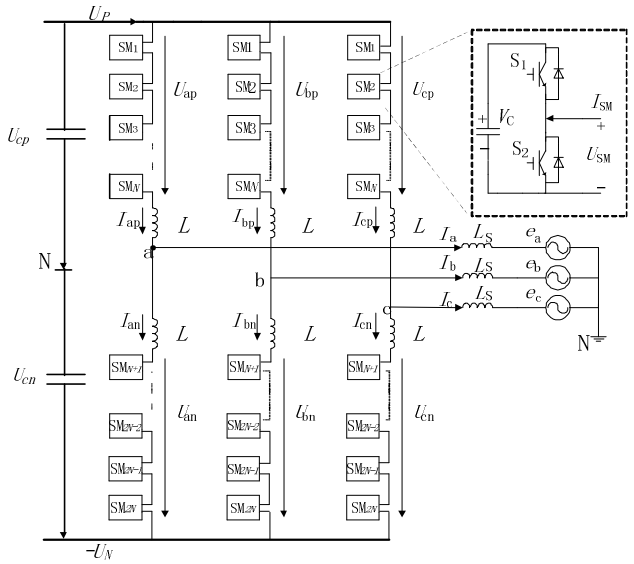


Fig. 1. Structure of a modular multi-level converter.

simplicity and rapid dynamic response, thus facilitating its wide use in many situations that require high harmonic current and current response rates, such as low-voltage APF [18] and reactive power compensation [19]. In this method, the output current of the converter, instead of the PI controllers of the inner loop in PSPWM and PDPWM, can be directly compared with the current reference. Hysteresis current tracking control is also a closed-loop control and has the advantages of high current response rate, fast real-time ability, and no need of carriers. Accordingly, applying this control in MMC is promising and can facilitate the implementations of MMC in middle and high voltage power systems.

However, due to the different topologies of MMC and common two-level inverters, applying the hysteresis current control in MMC may induce certain problems, including the unbalanced voltage of the capacitor, unbalanced voltage between the upper and lower arms, partition of the grid side voltage, and spectral characteristics of the current ripple.

This study intends to solve the above issues by proposing a quasi-fixed-frequency hysteresis current tracking control (QHCTC) strategy for MMC. In this novel strategy, the frequency of MMC output current is fixed, whereas the switching frequency of sub-module (SM) is quasi-fixed. In particular, the quasi-fixed-frequency is realized via virtual loop mapping (VLM), in which the SM switching frequency is similar to the output current frequency. This design can benefit the selection of switching devices and the assessment of system performances. The contributions of the proposed QHCTC are briefly described below.

First, by monitoring grid voltage and the deviation between the output and reference currents, the designed MMC can generate corresponding levels to force the output current to track the given current quickly and efficiently. In particular, the non-average voltage partition principle is used for the current tracking to prevent the overlap of the output and grid voltages in every voltage region.

TABLE I
HALF-BRIDGE SUB-MODULE WORKING STATES

Mode	S_k	S_{k1}	S_{k2}	U_{sm}	I_{sm}	*State*	*Capacitor*
1	1	1	0	*Vc*	>0	on	charge
2	1	1	0	*Vc*	<0	on	discharge
3	0	0	1	0	>0	off	no change
4	0	0	1	0	<0	off	no change

Second, varied hysteresis-band current tracking control is adopted by implementing fixed output current frequency on the basis of the above non-average voltage partition principle.

Third, the capacitor voltage of the upper/lower arm and the voltage between these arms are considered in the MMC design and are efficiently balanced with VLM and arm voltage balance (AVB), respectively. Accordingly, a balance control system and a quasi-frequency switching device driver are achieved.

Furthermore, the proposed method is validated with the simulations and experimental results of a five-level prototype of MMC.

II. STRUCTURE AND OPERATION PRINCIPLES OF MMC

A. Basic Structure

A basic three-phase four-leg MMC topology is shown in Fig. 1, in which the MMC is composed of three legs and six arms; each leg consists of one upper arm and one lower arm, and each arm contains a buffer inductor L and N series -connected SMs [21]. Also, phase voltages U_a, U_b, and U_c, are outputs from the intermediate connection point of the upper and lower arms, and their values depend on the difference between these arms.

In Fig. 1, SMs adopt the half–bridge sub-module (HBSM) design, which consists of a DC capacitor and two controllable power switches. HBSM is widely used in practice; its working status is shown in Table I where S_{k1} and S_{k2} are the driving signals of the upper and lower devices, respectively, whereas *Vc* is the average capacitor voltage of the k^{th} SM.

Table I particularly illustrates that each SM has "1" and "0" statuses, and the corresponding output voltages U_{sm} are *Vc* and 0. In this case, "1" and "0" imply that SM is inserted and bypassed, respectively. When HBSM is inserted, the direction of I_{sm} signifies the working status of the capacitor. If $I_{sm}>0$, the capacitor is charging, whereas if $I_{sm}<0$, the capacitor is discharging.

B. Operation Principles

Since the operation principles of three legs (phase j = *a, b, c*) are comparable, this research selects and analyzes only one leg (phase *a*) of MMC. The Kirchhoff's voltage law demonstrates the below equations.

$$\begin{cases} U_P - U_{aN} = U_{ap} + L\dfrac{dI_{ap}}{dt} \\ U_{aN} - U_N = U_{an} + L\dfrac{dI_{an}}{dt} \\ U_P = -U_N \end{cases} \tag{1}$$

$$I_{ap} = I_{an} + I_a \tag{2}$$

where U_P and U_N are DC bus voltages, U_{ap} and U_{an} are the sum of the upper and lower arm capacitor voltages, respectively, I_{ap} and I_{an} are the instantaneous current of the upper and lower arms, respectively, and I_a is the output current of MMC.

By substituting (2) in (1), the below expressions are obtained.

$$U_{aN} = \frac{1}{2}(U_{an} - U_{ap}) - \frac{L \cdot dI_a}{2dt} \tag{3}$$

$$U_{aN} = L_s\frac{dI_a}{dt} + e_a(t) \tag{4}$$

In traditional modulation methods, control systems provide the MMC modulation signals, which can be normalized and expressed as follows:

$$U_{mj} = m\cos(\omega t + \varphi_j) \tag{5}$$

where m is the modulation index ($0 \le m \le 1$), and φ_j is the angular displacement of the fundamental frequency.

Without considering the circulating current suppression, the normalized reference voltage signals of the upper/lower arm should be demonstrated as follows:

$$U_{mu} = \frac{1}{2}\left[1 - m\cos(\omega t + \varphi_j)\right] \tag{6}$$

$$U_{md} = \frac{1}{2}\left[1 + m\cos(\omega t + \varphi_j)\right] \tag{7}$$

These signals, in which the effects of buffer inductor L are ignored, have been widely used in MMC modulations such as NLM, PSPWM, and PDPWM. However, L has to be considered in the hysteresis current tracking control. This condition will be analyzed in the next section.

III. Hysteresis Current Tracking Control Strategy

A. Hysteresis Current Tracking Control

In general, grid-connected inverters have two control loops, namely, the outer voltage and inner current control loops, in which DC voltage regulation and current reference tracking are implemented, respectively. This research focuses on the latter and applies the hysteresis current tracking method to MMC.

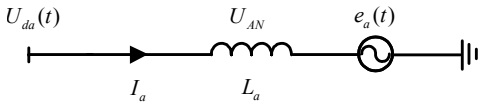


Fig. 2. Simplified single-phase MMC circuit.

In particular, this study illustrates the principle of hysteresis current tracking control by simplifying the MMC model shown in Fig. 1 into the model depicted in Fig. 2, where $U_{da}(t)$ is the equivalent output voltage, L_a is the equivalent inductance, and U_{AN} denotes the deviation between $U_{da}(t)$ and grid voltage $e_a(t)$.

The simplified model above can be expressed by taking (3) into (4), as specified below.

$$\frac{1}{2}(U_{an} - U_{ap}) - \frac{L}{2}\frac{dI_a}{dt} = L_s\frac{dI_a}{dt} + e_a(t) \tag{8}$$

$$U_{AN} = U_{da}(t) - e_a(t) \tag{9}$$

$$L_a = L_s + \frac{L}{2} \tag{10}$$

$$U_{da}(t) = \frac{1}{2}(U_{an} - U_{ap}) \tag{11}$$

$$U_{AN} = L_a\frac{dI_a}{dt} \tag{12}$$

Based on (8) to (12), Fig. 3 is generated to illustrate the principle of the hysteresis current tracking control, where h is the hysteresis width, 0.5 and $-0.5h$ denote the upper and lower thresholds, respectively, and Δi_j is the deviation between output I and reference currents I_{j_ref}, as displayed in (13).

$$\Delta i_j = I_{j\_ref} - I_j, \quad j = a, b, c \tag{13}$$

As signified in Fig. 3, when $\Delta i_j > 0.5h$, I_a holds a downward trend with $U_{AN}<0$. Similarly, when $\Delta i_j < -0.5h$, I_a holds an upward trend with $U_{AN}>0$. Thus, I_a is bounded within the hysteresis band, which is centered by the reference current. In practice, these operations can be implemented with the trigger signal of converter $D(t)$, which is defined below.

$$\begin{cases} D(t) = 0, & \Delta i_j > 0.5h \\ D(t) = 1, & \Delta i_j < -0.5h \\ D(t) = unchange & -0.5h \le \Delta i_j \le 0.5h \end{cases} \tag{14}$$

Moreover, Fig. 3 indicates that U_{AN} is critical to the performance of the hysteresis current tracking control because it determines the trend of I_a and helps control the current within hysteresis bands. According to (9), generating the optimal U_{AN} requires an effective design of the equivalent output voltage $U_{da}(t)$ and grid voltage $e_a(t)$. In this research, the optimal U_{AN} for $U_{da}(t)$ is a staircase in (11) and is further expressed in (15). Meanwhile, the optimal U_{AN} for $e_a(t)$ is partitioned into N+1 regions because converter output voltage U_{da} has N+1 levels with N+1 level modulation from L_1 to

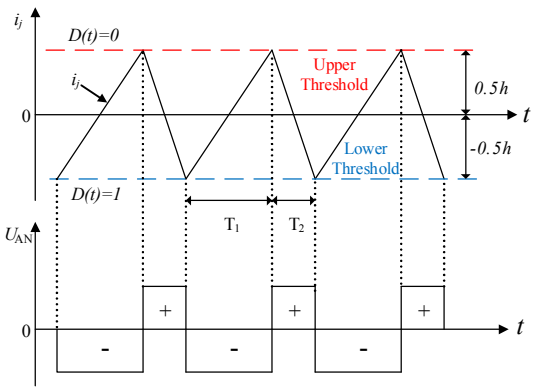


Fig. 3. Principle of hysteresis current tracking control.

L_{N+1}.Partitioned $e_a(t)$ is expressed with the intermediate symbol $D(t)$ in (16).

$$\begin{cases} U_{da}(t)=\dfrac{1}{2}(U_{an}-U_{ap}) \\ U_{an}=\sum_{K=N+1}^{2N} S_K \cdot V_c \\ U_{ap}=\sum_{K=1}^{N} S_K \cdot V_c \end{cases} \tag{15}$$

$$\begin{cases} \dfrac{-U_{dc}}{2} \le e_a(t) < \dfrac{V_c}{2}-\dfrac{U_{dc}}{2}, & V(t)=1 \\ \dfrac{V_c}{2}-\dfrac{U_{dc}}{2} \le e_a(t) < \dfrac{3V_c}{2}-\dfrac{U_{dc}}{2}, & V(t)=2 \\ \quad\cdots\cdots & \\ (M-\dfrac{3}{2})V_c-\dfrac{U_{dc}}{2} \le e_a(t) < (M-\dfrac{1}{2})V_c-\dfrac{U_{dc}}{2}, & V(t)=M \\ \quad\cdots\cdots & \\ (N-\dfrac{1}{2})V_c-\dfrac{U_{dc}}{2} \le e_a(t) < \dfrac{U_{dc}}{2}, & V(t)=N+1 \end{cases} \tag{16}$$

Notably, the width of 1^{st} and $N+1^{th}$ regions is 0.5 V_C, while that of the others is V_C. This arrangement is designed to prevent misjudging the region of $e_a(t)$, particularly at the vicinity of the converter output level.

An example of five-level converter is shown in Fig. 4 to demonstrate the relationship between the output voltage levels and grid voltage regions. In this figure, e_{amax} and e_{amin} are the peak and trough values of $e_a(t)$, respectively; L_0 to L_4 are the five output voltage levels of the MMC; and $V(t)$ represents the corresponding regions. The adjacent levels generating U_{AN} in a specific region are grouped in common parentheses (e.g., working levels (L_2, L_4) implies $V(t)$ = 4).

In addition, Fig. 4 presents the operation of the designed five-level MMC under the hysteresis current tracking control. When grid voltage $e_a(t)$ exists in certain regions, the following cases emerge: 1) if Δi_j exceeds the upper threshold ($D(t)$ = 0), the MMC output voltage will be controlled to $U_{da2}(t)$ to reverse the current rising trend; 2) if Δi_j decreases below the lower threshold ($D(t)$ = 1), the MMC output voltage will be set to $U_{da1}(t)$. Hence, the relationships of $D(t)$, $V(t)$, and $U_{da}(t)$ can be summarized as denoted in Table II,

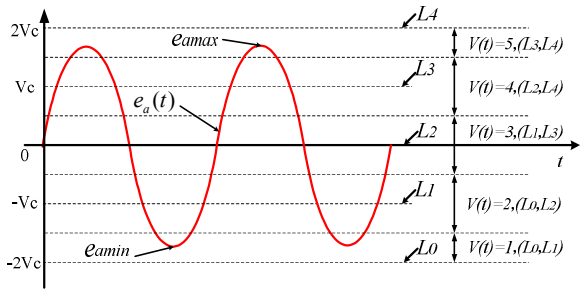


Fig. 4. Output voltage levels and grid voltage regions of five-level converter.

TABLE II
RELATIONSHIPS OF D(T), V(T), AND U_{DA}(T)

V(t)	D(t)	$U_{da}(t)$
1	0	$U_{da2}(t)=-U_{dc}/2$
	1	$U_{da1}(t)=-U_{dc}/2+U_{dc}/N$
2,3,…, N	0	$U_{da2}(t)=[V(t)-2]\cdot U_{dc}/N-U_{dc}/2$
	1	$U_{da1}(t)=V(t)\cdot U_{dc}/N-U_{dc}/2$
N+1	0	$U_{da2}(t)=U_{dc}/2-U_{dc}/N$
	1	$U_{da1}(t)=U_{dc}/2$

where $U_{da1}(t)$ and $U_{da2}(t)$ ($U_{da1}(t) > U_{da2}(t)$) in each voltage partition represent the MMC output levels during the rise T_1 and fall times T_2, respectively.

Table II suggests that the number of the inserted lower arm SMs of the MMC is equal to $N(t)$ [21].

$$\begin{cases} N(t)=0, & V(t)=1, D(t)=0 \\ N(t)=1, & V(t)=1, D(t)=1 \\ N(t)=V(t)+2D(t)-2, & V(t)\ne 1, N+1 \\ N(t)=N-1, & V(t)=N+1, D(t)=0 \\ N(t)=N, & V(t)=N+1, D(t)=1 \end{cases} \tag{17}$$

B. Performance Analysis

The proposed method is further analyzed by evaluating the hysteresis control in a short-term period T, which consists of T_1 and T_2. By assuming that the switching frequency is sufficiently high and that the influence of fundamental frequency is ignored, the switching rise and fall times can be expressed as follows:

$$\begin{cases} T_1=\dfrac{h\cdot L_a}{U_{AN}}=\dfrac{h\cdot L_a}{U_{da1}(t)-e_a(t)} \\ T_2=\dfrac{-h\cdot L_a}{U_{AN}}=\dfrac{h\cdot L_a}{e_a(t)-U_{da2}(t)} \end{cases} \tag{18}$$

$$T=T_1+T_2=\frac{(h\cdot L_a)[U_{da1}(t)-U_{da2}(t)]}{[U_{da1}(t)-e_a(t)][e_a(t)-U_{da2}(t)]} \tag{19}$$

Accordingly, the output current frequency is

$$f=\frac{1}{T}=\frac{[U_{da1}(t)-e_a(t)][e_a(t)-U_{da2}(t)]}{(h\cdot L_a)[U_{da1}(t)-U_{da2}(t)]} \tag{20}$$

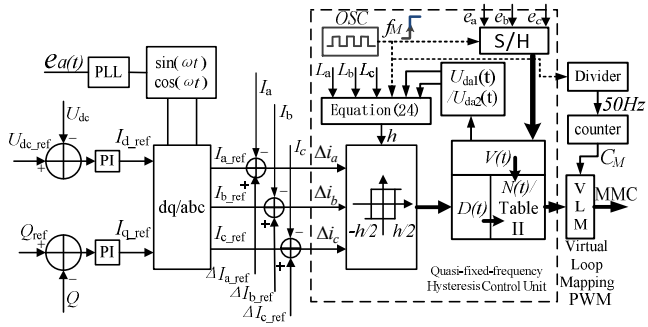


Fig. 5. Scheme of the quasi-fixed-frequency hysteresis current tracking control.

By combining the previous analysis in Table II, the below expressions are derived.

$$V(t)=1, \quad with$$

$$\begin{cases} U_{da1}(t)-U_{da2}(t)=V_c=U_{dc}/N \\ f=\dfrac{\left[U_{da1}(t)-e_a(t)\right]\left[e_a(t)-U_{da1}(t)+V_c\right]}{\left(h\cdot L_a\right)V_c} \\ 0.5V_c<U_{da1}(t)-e_a(t)\le V_c-0.5U_{dc}-e_{a\min} \end{cases} \tag{21}$$

$$V(t)=2,3,...,N \quad with$$

$$\begin{cases} U_{da1}(t)-U_{da2}(t)=2V_c=2U_{dc}/N \\ f=\dfrac{\left[U_{da1}(t)-e_a(t)\right]\left[e_a(t)-U_{da1}(t)+2V_c\right]}{\left(h\cdot L_a\right)2V_c} \\ 0.5V_c<U_{da1}(t)-e_a(t)\le 1.5V_c \end{cases} \tag{22}$$

$$V(t)=N+1, \quad with$$

$$\begin{cases} U_{da1}(t)-U_{da2}(t)=V_c=U_{dc}/N \\ f=\dfrac{\left[U_{da1}(t)-e_a(t)\right]\left[e_a(t)-U_{da1}(t)+V_c\right]}{\left(h\cdot L_a\right)V_c} \\ 0.5U_{dc}-e_{a\max}\le U_{da1}(t)-e_a(t)\le 0.5V_c \end{cases} \tag{23}$$

Equations (21) to (23) indicate that the switching frequency of PWM signals for hysteresis control shows great uncertainty with a constant hysteresis width *h*. This issue induces difficulties in selecting switching devices and assessing system performance.

C. Quasi-Fixed-Frequency Hysteresis Current Tracking Control

The above challenges are tackled in this section by presenting the proposed QHCTC, which aims to obtain a fixed output current ripple frequency by controlling hysteresis width *h* in real-time. A brief scheme of QHCTC is illustrated in Fig. 5, where S/H represents the sample and hold function.

As depicted in Fig. 5, the MMC control system has two control loops, which are the outer DC voltage and the inner current control loops. The outer loop provides current references for the inner loop to utilize QHCTC, which adjusts the closed-loop current and transforms the current reference signals into corresponding PWM switching signals. These tasks can be performed with the following procedures: 1) calculate the deviation currents Δi_a, Δi_b, *and* Δi_c with (13); 2) generate *D(t)* by comparing the deviation currents and hysteresis width *h* in (24); 3) obtain *N(t)* with (17). *D(t)*, *V(t)* , and *N(t)* are all available; hence, the proposed QHCTC can be implemented. From (20), hysteresis width *h* can be acquired as follows:

$$h=\frac{\left[U_{da1}(t)-e_a(t)\right]\left[e_a(t)-U_{da2}(t)\right]}{\left(f_M\cdot L_a\right)\left[U_{da1}(t)-U_{da2}(t)\right]} \tag{24}$$

where f_M is a fixed-frequency square wave similar to the system sample frequency.

In this study, the control process is simplified by expressing the calculation of (17) with the true value table. Consequently, the system efficiency is expected to be improved. In this case, the Virtual Sub-Module (VSM) [14, 20] is implemented, in which the driving signals are directly mapped from VSMs to RSMs. An N = 4 example is illustrated, where the PWM signals of VSMs are arranged according to (17) and are listed in Table III. The VSMs of lower/upper arms are numbered from *1*' to *2N*'; 0 and 1 stand for "OFF" and "ON" status, respectively. The hysteresis result *D(t)* is assigned to VSM 5' and VSM 6' when V(t) is equal to 2 to 4, and */D(t)* denotes the negated *D(t)*.

TABLE III
TRUE VALUE TABLE OF THE LOWER ARM VSMS

V (t)	1'	2'	3'	4'	5'	6'	7'	8'
1	*/D(t)*	1	1	1	*D(t)*	0	0	0
2	*/D(t)*	*/D(t)*	1	1	*D(t)*	*D(t)*	0	0
3	*/D(t)*	*/D(t)*	0	1	*D(t)*	*D(t)*	1	0
4	*/D(t)*	*/D(t)*	0	0	*D(t)*	*D(t)*	1	1
5	*/D(t)*	0	0	0	*D(t)*	1	1	1

IV. BALANCE CONTROL SCHEME

In this section, the issue of balancing arm capacitor voltages, which has not been covered in the above analysis, is solved by balancing the capacitor voltage of the upper/lower arm and the voltage between the upper and lower arms with VLM and AVB, respectively.

A. Capacitor Voltage Balance Control

VLM is applied to balance the arm capacitor voltage in each arm. VLM has been successfully used with PDPWM to balance the capacitor voltages of SMs [20]. The principle of VLM is to use a count-up counter C_M for mapping VSMs to RSMs. The working frequency of C_M can be set as required (in this paper, it is set as 50 Hz), and its counting range is from 0 to *N*-1. The entire mapping process has been technically addressed by [14] and [20]. With this method, the capacitor voltage can be efficiently balanced in case of system symmetry (Selective Virtual Loop Mapping can also

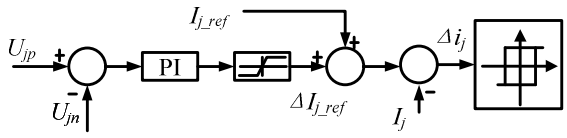


Fig. 6. Arm voltage balance control.

be used to acquire the capacitor voltage dynamic balance even if MMC loses its symmetry, but this issue is not the focus of this research).

After implementing VLM, the PWM signals will periodically combine the components of the fundamental and high order frequencies (e.g., fixed frequency f_M). This instance is the reason why the proposed method is named as "quasi-fixed-frequency hysteresis current tracking control."

B. Arm Voltage Balance Control

Apart from the unbalance voltage issue of a single arm, the unbalance voltages over the upper and lower arms should also be considered in MMC design. The unbalance voltages over the arms are mainly derived from the difference of energy losses among the arms and the zero drift error of MMC output current. Traditionally, the voltages of the arms are balanced by adding compensation into modulation signals [7]. This method, however, has the following disadvantages: 1) it is complex; 2) it requires PI controllers, which may reduce the robustness of the system; 3) its output waveform can be easily distorted; 4) it cannot be applied in hysteresis control. Therefore, this study implements the AVB [23]-[25] control method to address the abovementioned drawbacks. The block diagram of AVB is displayed in Fig. 6, where U_{jp} and U_{jn} are the sum of the upper and lower arm capacitor voltages (j = *a, b, c*), respectively, and they can be replaced by capacitor voltages U_{cp} and U_{cn} in the single phase MMC.

In Fig. 6, the arm voltage balance correction signal $\triangle I_{j\_ref}$ is generated by a PI controller, the input of which is the difference between U_{jp} and U_{jn}, and is added to the current reference I_{j_ref}, that can acquire the balance between U_{jp} and U_{jn}.

V. SIMULATIONS

The proposed method is validated by implementing a simulation on the single-phase five-level MMC model. The schematic figure of the tested prototype is shown in Fig. 7 [20]. As depicted in Fig. 7, the model has four SMs in one arm, and the ground point is directly connected to the midpoint of two DC sources. In this case, $e_a(t)$ can be the grid voltage or the voltage across the load. The related system parameters are those specified in Table IV, in which the SM capacitor voltage is set as an average value and the influence of voltage ripple is neglected.

Fig. 8 shows the relationships of grid voltage $e_a(t)$, corresponding $V(t)$, and hysteresis width h during 0.03 s to

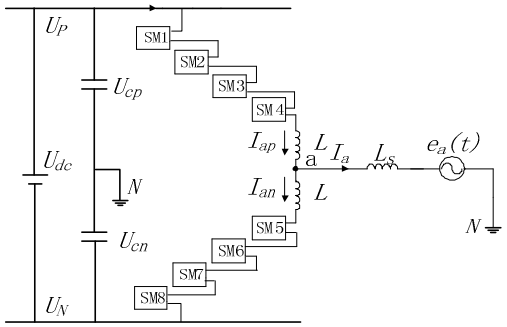


Fig. 7. Prototype of a single phase MMC.

TABLE IV
SIMULATION PARAMETERS

Parameters	*Values*	*Parameters*	*Values*
DC link voltage U_{dc}	800 V	Arm inductor L	2 mH
No. of SMs in each arm	4	Equivalent resistance of arm R	0.5 Ω
SM capacitor voltage Vc	200 V	Output current amplitude	20 A
SM capacitor C	2200 uF	Counter frequency	50 Hz
DC bus capacitor C_{up}, C_{un}	4700 uF	Sample frequency f_M	5 kHz
Output inductance L_S	6 mH	Grid voltage amplitude	311 V

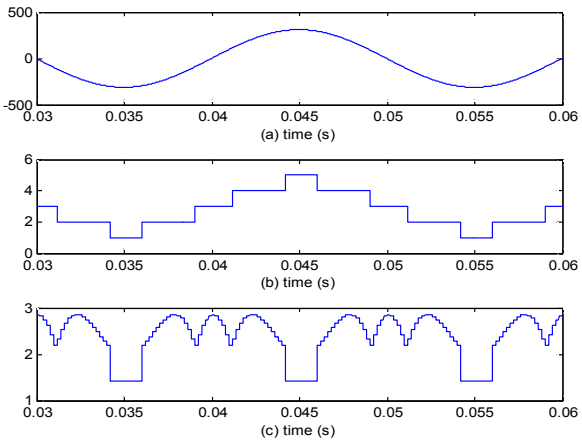


Fig. 8. Relationships of $e_a(t)$, $V(t)$, and h.

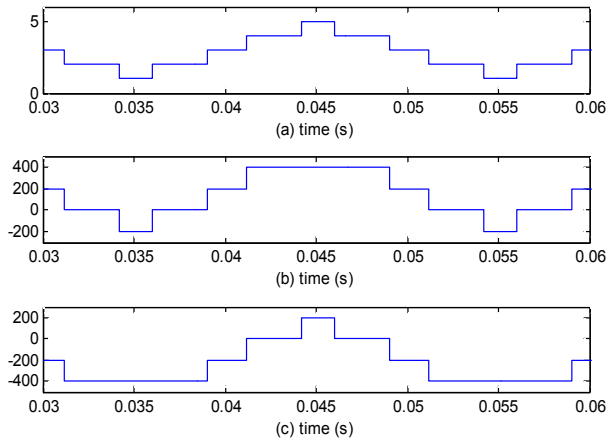


Fig. 9. $V(t)$ and the corresponding MMC output levels $U_{da1}(t)$ and $U_{da2}(t)$.

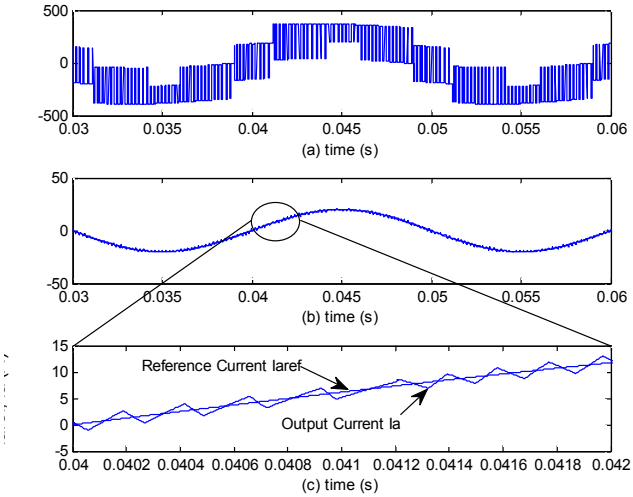


Fig. 10. Consequence of QHCTC: (a) *Ua(t)*, (b) I_{aref}, and I_a, (c) and zoomed results between 0.04 and 0.042 s.

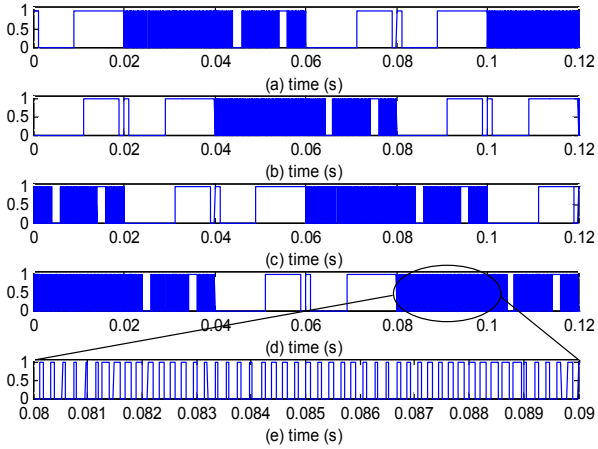


Fig. 11. PWM signals of SMs 1 to 4 between 0 and 0.12 s. (a) PWM1; (b) PWM2; (c) PWM3; (d) PWM4; (e) Zoomed PWM4 between 0.08 and 0.09 s.

0.06 s. Hysteresis width *h* is variable; thus, five regions (–400, –300), (–300, –100), (–100, 100), (100, 300), (300, 400) evidently exist, as indicated by *V(t)* = 1 to *V(t)* = 5, respectively.

Fig. 9 indicates the relationships among *V(t)*, $U_{da1}(t)$, and $U_{da2}(t)$. In particular, this figure demonstrates that $U_{da1}(t)>U_{da2}(t)$ holds in general, but the difference between $U_{da1}(t)$ and $U_{da2}(t)$ varies. Moreover, if *V(t)* is equal to 1 or 5, the voltage difference is V_c; otherwise, the voltage difference is $2V_c$.

Fig. 10 presents the consequences of the proposed QHCTC. In particular, the MMC output voltage with reference current I_{a_ref} and MMC output current I_a are shown in Figs. 10(a) and (b), respectively. Meanwhile, Fig. 10(c) is the zoomed results of Fig. 10(b) from 0.04 s to 0.042 s, indicating that the actual current can efficiently follow the reference current with a fixed-frequency.

Figs. 11(a) to (d) exhibit the PWM signals of RSMs 1 to 4 in the upper arm. These figures particularly illustrate that the frequency components in each PWM signal have two kinds, namely, the low-frequency and fixed high-frequency components. The low-frequency component depends on the PWM signals continuity, as specified in Table III. For example, when *V(t)* is equal to 1, 2, and 3, the PWM signals of VSMs 4' are all working in "1" state, whereas the PWM signals of VSMs 4' are working in "0" statewhen *V(t)* is equivalent to 4 and 5. Meanwhile, the high frequency component of PWM 4 is zoomed in Fig. 11(e), and its frequency is about 5 kHz, which is equal to f_M. A 0.02 s delay exists among these PWM signals due to the 50 Hz counter frequency of VLM.

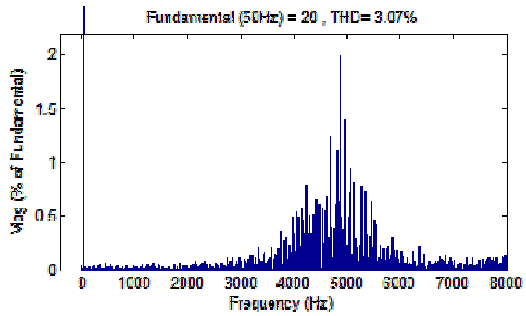


Fig. 12. Spectrum of output current I_a.

Fig. 12 is the spectrum of I_a. In this case, THD is about 3.07%, and the main frequency component is concentrated at nearly 5 kHz.

VI. Experiments

The feasibility of the proposed method is further verified by conducting single-phase experiments under low voltage on an MMC test bench. This time, grid voltage source $e_a(t)$ is replaced with a 15 Ω resistor. The experimental parameters are listed in Table V.

Fig. 13(a) shows the output voltage and current of the MMC in the case of five-level modulation, and Fig. 13(b) depicts the corresponding zoomed region of Fig. 13(a).

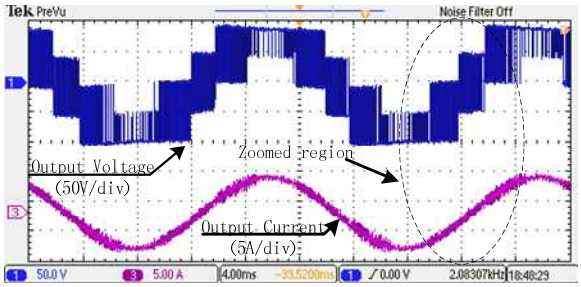
Fig. 14 reveals the output waveforms between PDPWM (VLM is used) and QHCTC. In particular, this figure evidently demonstrates that the latter has a smoother current waveform, particularly in the vicinity of the peak output current.

Fig. 15(a) describes the output voltage and corresponding PWM signal of one SM, and Fig. 15(b) is the corresponding zoomed region.

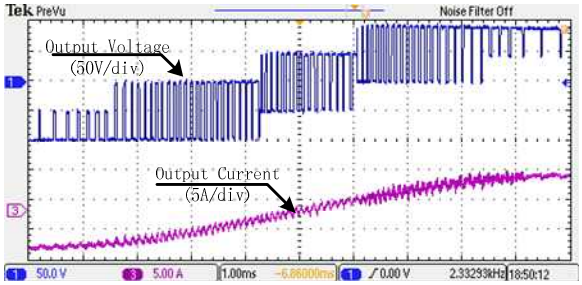
Meanwhile, Fig. 16 shows the MMC output voltage and current waveforms when the reference current amplitude and phase transitions simultaneously occur. The reference current amplitude changes from 6.2 A to 4 A, accompanied by a 90° phase shift. The result of the test indicates that the actual output current can rapidly track the reference current and demonstrates the high dynamic response capability of the proposed method.

TABLE V
EXPERIMENTAL PARAMETERS

Parameters	*Values*	*Parameters*	*Values*
DC link voltage U_{dc}	200 V	Arm inductor L	1.2 mH
No. of SMs in each arm	4	Load resistor	15 Ω
Capacitor voltage Vc	50 V	Sample frequency f_M	5 kHz
SM capacitor C	2200 uF	Output current amplitude	6.2 A
Output inductance L_S	4 mH	Counter frequency	50 Hz



(a)



(b)

Fig. 13. (a) Output voltage and current of the experimental system. (b) Zoomed voltage and current waveforms of the experimental system.

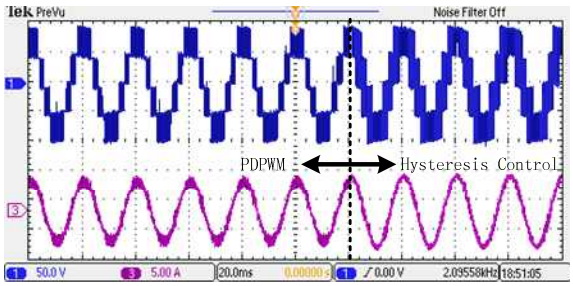
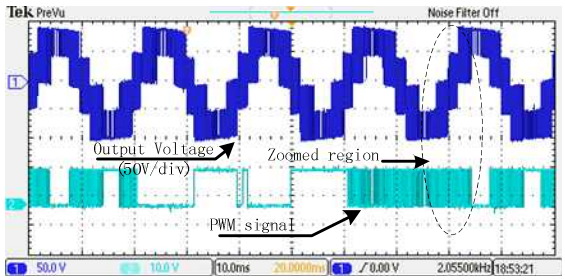
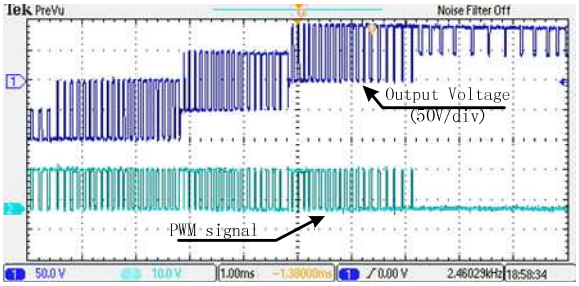


Fig. 14. Output voltage and current of the experimental system.



(a)



(b)

Fig. 15. (a) Output voltage and PWM signal. (b) Zoomed voltage and PWM signal waveforms.

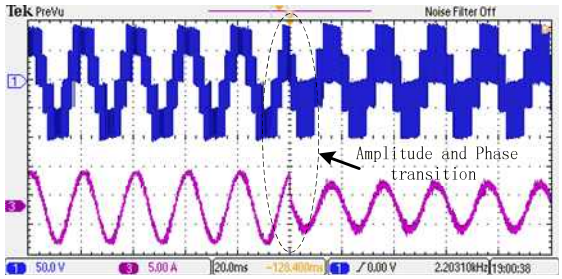
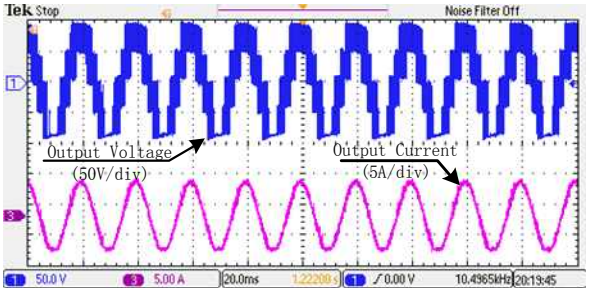
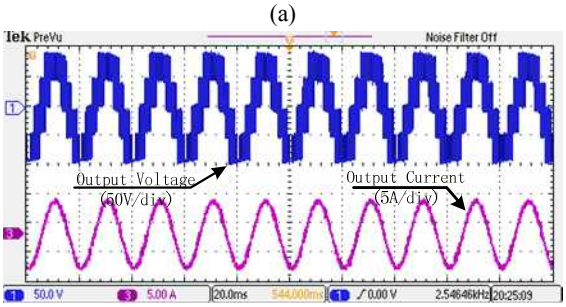


Fig. 16. Output voltage and current of the experimental system in the condition of the reference current's amplitude and phase transition



(a)



(b)

Fig. 17. (a) Output voltage and current when arm voltage loses balance. (b) Output voltage and current when arm voltage control is adopted.

In this experiment, the arm voltage balance control is also tested with the existence of some zero drift in the output current sensor. Fig. 17(a) illustrates the output voltage and current when the lower arm voltage is greater than the upper arm voltage. The output voltage and current distortion

evidently occur in 17(a). Meanwhile, Fig. 17(b) presents the variation processes of the output voltage and current when the arm voltage control is applied. The results of the test show that the unbalance voltage of arms is effectively corrected.

VII. CONCLUSIONS

This study proposes a new QHCTC strategy for MMCs based on the non-average voltage partition principle. The inserted number of the MMC lower arm SMs *N(t)* is presented by derivation. By implementing both VLM and AVB, the capacitors' voltages of the upper/lower arms are efficiently balanced.

The proposed method is designed for any number and levels of SMs, and its validity is verified with the experimental results on a single-phase five-level MMC prototype.

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