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Implementation of a No Pulse Competition CPS-SPWM Technique Based on the Concentrated Control for Cascaded Multilevel DSTATCOMs

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Abstract

Digital signal processor (DSP) and field programmable gate array (FPGA) based concentrated control systems are designed for implementing CPS-SPWM strategies. The self-defined universal asynchronous receiver/transmitter (UART) protocol is used for communication between a master controller and an individual module controller via high speed links. Aimed at undesired pulse competition, this paper analyzes its generation mechanism and presents a new method for eliminating competition pulses with no time delay. Finally, the proposed concentrated controller is applied to a 10kV/10MVar distribution static synchronous compensator (DSTATCOM) industrial prototype. Experimental results show the accuracy and reliability of the concentrated controller, and verify the superiority of the proposed elimination method for competition pulses.

Key words: Cascaded DSTATCOM, Concentrated control system, CPS-SPWM, FPGA, Pulse competition elimination

I. INTRODUCTION

Cascaded H-bridge multilevel inverters (CHBMLIs) are receiving increased attention recently for medium-voltage and high-power electronic applications, since an improved high output voltage can be obtained with a respective harmonic content reduction. In particular, CHBMLIs have been reported for use in applications such as medium voltage industrial drives, electric vehicles, and the grid connection of photovoltaic generation systems [1]-[3].

Various pulse width modulation (PWM) strategies for CHBMLIs have been reported in the literature. The unipolar carrier phase shifted SPWM (CPS-SPWM) strategy seems to be superior to others due to its excellent output performance as well as its relatively simple implementation [3]-[7].

To implement a CPS-SPWM technique for CHBMLI systems, there are two major approaches that can be used. 1) The controller and PWM references are generated in a single central processing unit in the concentrated control. 2) Individual processors are used for each inverter module for producing the voltage/current command generated from the central processor controller in the distributed control [8]-[11]. The distributed control method can distribute the computational load to the individual processors in the modules. However, real-time control and PWM synchronization are complex and difficult. This can cause reliability issues and reduce engineering superiority since the theoretical harmonic cancellations and common-mode voltage reductions of CPS-SPWM techniques can only be achieved in practice with the proper synchronization of carriers and waveforms within a cascaded system. The potential problems of distributed control can be solved with a concentrated control in which PWM synchronization can be simply achieved. However, since the centralized processor must handle the computation and data transmission for the entire system, the computational requirements are so intense that they may easily exceed the capability of the majority of digital signal processors (DSPs).

In this paper, a DSP and field programmable gate array (FPGA) based master controller is designed for implementing concentrated control. After the real-time control and CPS-SPWM generation are performed, the master controller sends PWM pulses to each individual module controller, receives DC-link voltage data and fault status observed by the module controller, and a high speed link made of optical

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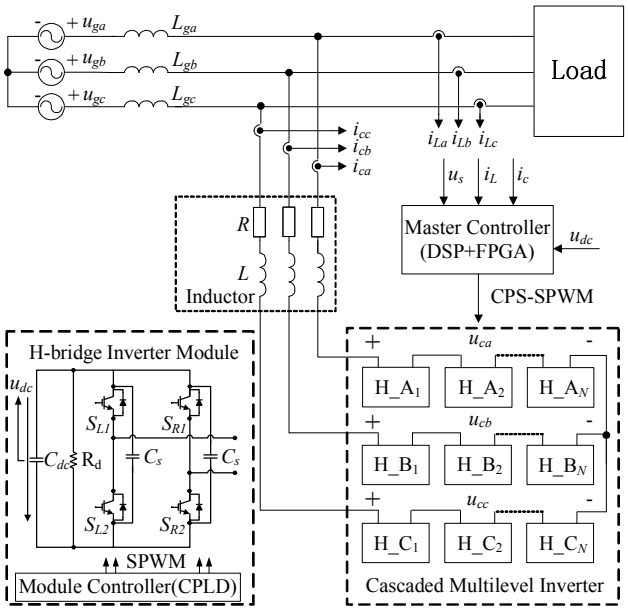


Fig. 1. Main structure of a cascaded DSTATCOM.

cables is applied for communication between the master controller and each of the module controllers. The rest of this paper is organized as follow. Section II describes the main structure of a CHBMLI based cascaded distribution static synchronous compensator (DSTATCOM) and introduces a switching scheme for a CPS-SPWM. Section III describes the detailed design of the proposed concentrated control system. Section IV presents experiments carried out on a cascaded DSTATCOM industrial prototype to verify the accuracy and reliability of the concentrated control. Section V summarizes the results of this paper and draws some conclusions.

II. Main Structure of a Cascaded DSTATCOM and the CPS-SPWM Switching Scheme

A. Main Structure of Cascaded DSTATCOM

Fig. 1 shows the main structure of a cascaded DSTATCOM which has a three-phase three-wire configuration. The inverter of the DSTATCOM consists of several H-bridge power inverter modules connected in series per phase. Each inverter module is made up of an IGBT based H-bridge inverter, a DC-link capacitor (C_{dc}), a discharge resistor (R_{dc}) and the peak absorption capacitors (C_s). In addition, it has its own module controller. The DSTATCOM is connected to the point of common coupling (PCC) though an inductor L (with an equivalent resistance R) which makes an essential contribution to the filtering out of switching ripples. When in operation, the DC-link voltage is stabilized at a given value (u_{dc}), and the bridge arms switch according to the pulses generated by the CPS-PWM technique to obtain the desired fundamental AC output voltage.

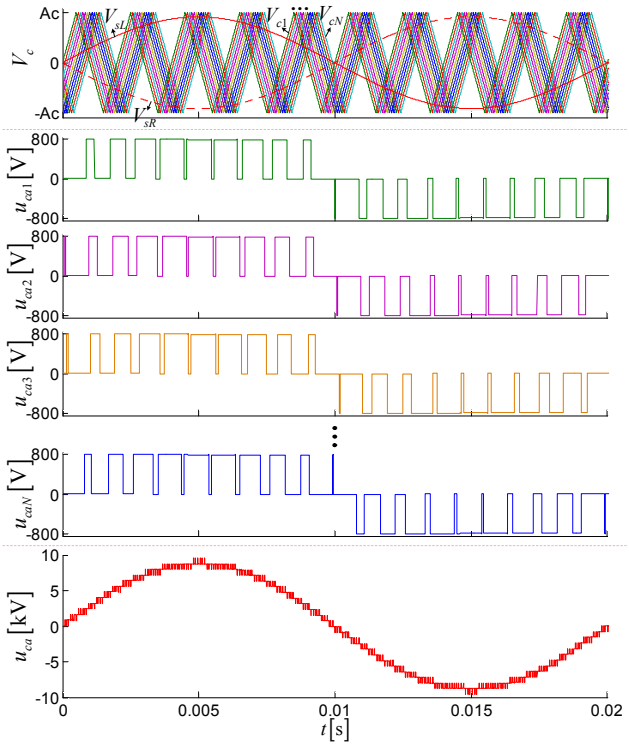


Fig. 2. CPS-SPWM switching scheme.

B. CPS-SPWM Switching Scheme

A so-called carrier phase shifted (CPS) unipolar sinusoidal pulse width modulation (SPWM) switching scheme applied to cascaded multilevel inverters is briefly described with the aid of Fig. 2. N triangle carriers (V_{c1}, V_{c2}, … and V_{cN}) are for N H-bridge inverters in a particular phase. The carriers have the same frequency (f_s) and the same peak-to-peak amplitude. They are time shifted by $T_s/2N$, where T_s is the period of the carriers ($T_s=1/f_s$). All of the H-bridge inverters share the same modulating sinusoidal signals, V_{sL} and V_{sR}, which are in phase opposition by 180° from each other. They are responsible for the switches on the left and right arm of a particular H-bridge inverter. The output voltage of a particular phase named as u_{ca} is the sum of all of the H-bridge inverter output voltages (u_{ca1}, u_{ca2}, … and u_{caN}).

One of the main advantages of this switching scheme is that the harmonics of the resultant CHBMLIs output voltage only appear at the sidebands centered around the frequency of $2Nf_s$ and its multiples, provided that the voltage across the dc capacitor of each inverter is the same (N is the number of H-bridge inverters, and f_s is the frequency of the triangle carrier signals). Therefore, the resultant CHBMLI output voltage has a quite high equivalent switching frequency, even if the switching frequency of the individual switches is not very high.

This is demonstrated with the output voltage spectrums of a single H-bridge inverter and DSTATCOM cascading 12 H-bridge inverters per phase as shown in Fig 3. The switching frequency of an individual switch is 1 kHz. It can be seen from

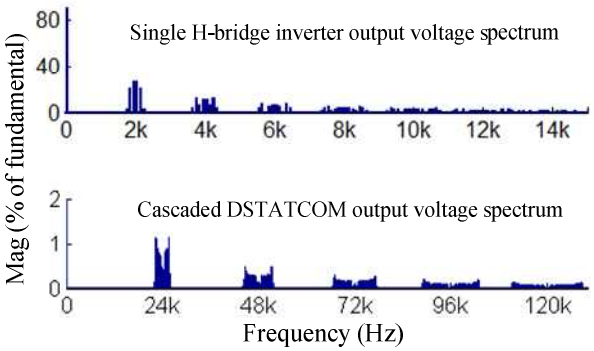


Fig. 3. Spectrums of single H-bridge inverter and cascaded DSTATCOM output voltage.

the figure that the harmonics of a single H-bridge inverter output voltage only appear at the sidebands centered around the frequency of 2 kHz and its multiples, while the harmonics of the cascaded DSTATCOM output voltage only appear around 24 kHz, 48 kHz, and so on.

III. Design of Concentrated Control System

To implement the CPS-SPWM technique for a cascaded DSTATCOM, a concentrated control system based on a DSP and a FPGA is designed. The FPGA is a standard integrated circuit that can be programmed by users to perform a variety of complex logical functions. The high level of integration available with these devices means that they can be used to implement complex electronic systems. Furthermore, there are many advantages due to the rapid design process and reprogrammable functions. Therefore, it is possible to create, implement and verify a new design.

The control strategy for the DSTATCOM, as well as the system configuration and features of the concentrated controller are summarized in Fig. 4.

As the main controller, the DSP is responsible for the current control as well as the DC-link voltage balancing control. It also generates modulation commands and writes them to FPGA through data bus. The current control for the DSTATCOM employs a PI controller in the DQ rotating frame, with a repetitive controller which can introduce an infinite open loop gain at the periodic signal's fundamental frequency and its harmonics, particularly when compensating for harmonic loads.

The FPGA generates SPWM signals based on modulation commands for each of the H-bridge inverters from the DSP and it sends these PWM pulses to the individual module controller using universal asynchronous receiver/transmitter (UART) communication via a high speed link made of optical cables.

The concentrated controller also performs observation, diagnosis, protection and other auxiliary functions at a system level. The module controller, located in each module, makes

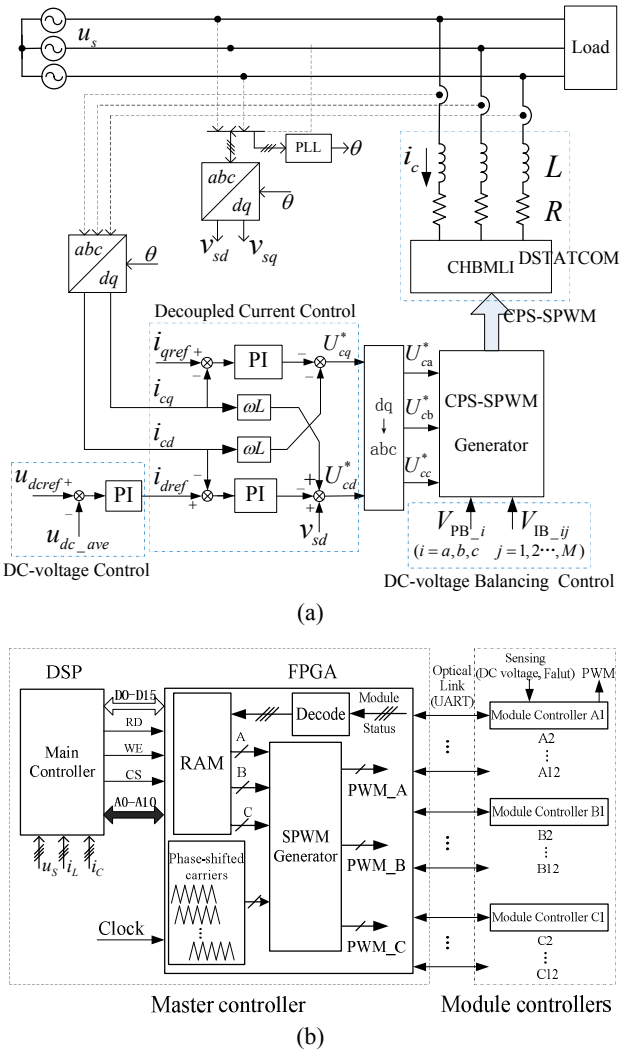


Fig. 4. Concentrated control system for cascaded DSTATCOM. (a) Block diagram of DSTATCOM control strategy. (b) Schematic diagram of DSP+FPGA based concentrated controller.

its own observation and sends the DC-link voltage data and fault status of that particular module to the concentrated controller via the high speed link. In the proposed design, the self-defined UART communication protocol is used for data transmission between the concentrated controller and the module controllers.

A. Phase Shifted Carriers

Phase shifted carriers are embedded in the FPGA. Each triangular carrier is in general a counter as shown in Fig. 5. The counter repetitively increases from zero to its peak value by adding 1 to the counter value for each clock pulse, and then it decreases to zero with the same counter step. Where P is the peak value of the counter, T_s is carrier period namely the switching period, and t_{clk} is period of the FPGA work clock.

$$P = \frac{T_s}{2t_{clk}} \tag{1}$$

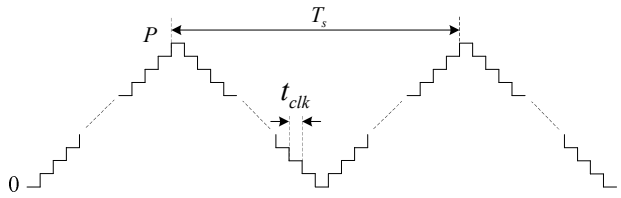


Fig. 5. Schematics of single triangular carrier.

Theoretically, the time shift t_{shift} of each individual carrier from the first carrier for the CPS-SPWM is in accordance with (2). K and N represent the K-th individual and the total carrier number, respectively.

$$t_{shift} = (K-1)\frac{T_s}{2N} \tag{2}$$

Then the phase shifted carriers can be achieved by setting a series of counters as in Fig. 6. The initialization conditions of the counters essential to the phase shift characteristic should be accurately calculated. Take the peak time t_0 of the first carrier as the start time for all of the counters, the initial value $t_0(K)$ of the individual carrier is calculated using the following:

$$u_0(K) = \frac{N-K+1}{N}P \tag{3}$$

Meanwhile, the initial count direction of the first carrier is the decrease direction, while other carriers all increase at the next count clock.

Generally, all of the counters share the same count clock, and the carrier misalignment which may occur in distributed control due to the possible drifting of individual clock counting does not appears in concentrated control systems. Thus, the carrier synchronization is achieved easier with a higher reliability.

B. PWM Pulse Competition and its Elimination

As stated previously, the equivalent switching frequency of the cascaded multilevel inverter output is quite high, even if the frequency of the individual switches is not very high. In practical applications, the switching frequency of the individual switches is generally lower than 1 kHz. In addition, the considerably high sampling frequency of the digital control system responsible for control precision and system robustness is selected. Unusually it is higher than two times the switching frequency. Thus, the DSP refreshes the modulation signals several times per switching period. In this case, the asymmetric uniformly sampling SPWM method for which the modulation signal just updates at peaks and troughs of the triangular carrier every switching period would not only sacrifice the sampling frequency but also introduce a large time delay in the PWM.

The other method for which a FPGA updates the modulation signal at each clock pulse can introduce no time delay in the PWM but generates pulse competitions. Fig. 7 shows the schematic diagram of the SPWM pulse competitions, where

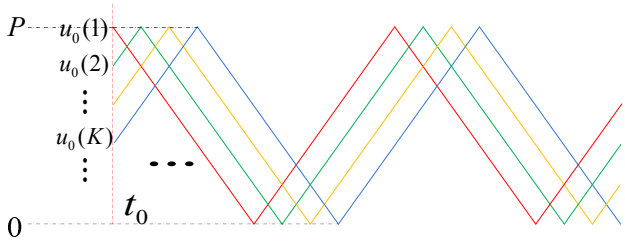


Fig. 6. Schematics of phase-shifted carriers.

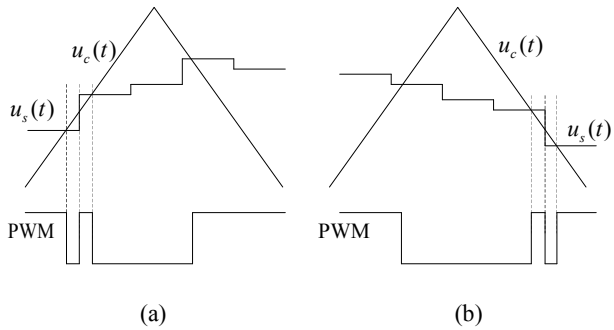


Fig. 7. Demonstration of pulse competitions (a) Rising half cycle and (b) Falling half cycle.

$u_s(t)$ is a modulation signal refreshed by the DSP, and $u_c(t)$ is a triangular carrier signal counted in the FPGA. During the rising half cycle of the triangular carrier signal, the modulation signal intersect with the carrier signal two times and the PWM signal changes three times as shown in Fig. 7(a). The PWM signal also changes several times during the falling half cycle of the triangular carrier signal as shown in Fig. 7(b). The phenomenon that the PWM signal changes more than once during a triangular carrier's rising half cycle or falling half cycle is called PWM pulse competition in this paper.

Fig. 8 shows the experimental results of the pulse competitions. In this picture, the narrow PWM pulses of the pulse competition can be up to 6μs which is longer than the common dead time of devices. These pulse competitions will lead to frequently action of IGBTs in a switching period. This will increase the switching loss, produce interference in the multilevel output and introduce additional harmonics.

To eliminate undesired pulse competitions, a narrow pulse detection method is traditionally adopted for which a narrow pulse detection unit is added. Then all of the narrow pulses from the SPWM generator are deleted and do not appear in the final output. However, the detection unit has an inherent time delay which is approximately of the same magnitude as the time shift of the phase-shifted carriers and will cause interference in the multilevel output. In addition, the selection of the threshold for the detection unit is difficult due to the uncertain width of the narrow pulse. Generally, the larger the threshold is, the less narrow pulses remain. However, a larger inherent time delay is inevitable.

This paper proposes a zero time delay pulse competition elimination method for which the PWM is restricted to change

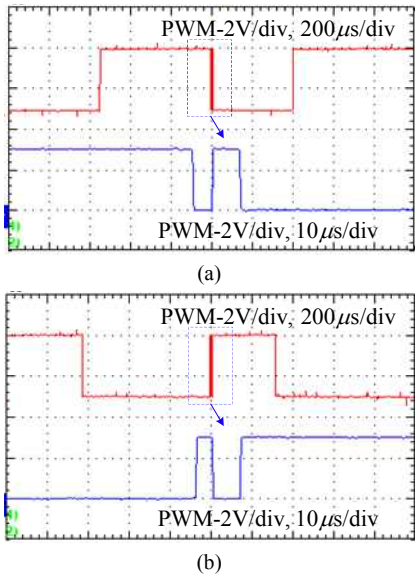


Fig. 8. Experimental results of pulse competitions. (a) Rising half cycle. (b) Falling half cycle.

only once during both the rising half cycle and the falling half cycle of the carrier. Fig. 9 shows the flowchart of the proposed pulse competition eliminate algorithm. The algorithm works at each FPGA clock pulse. *R_flag* and *F_flag* are binary variables (0-1 variables) corresponding to the rising half cycle and falling half cycle, respectively. It is typically defined that 0 means that the PWM has not changed before the current clock pulse, while 1 means the PWM has changed. In a particular half cycle, the PWM changes for the first time when the modulation signal equals the triangular carrier signal. Meanwhile, the corresponding binary variable is set to 1. After that the PWM does not change even if the modulation signal becomes equal to the triangular carrier signal again. The binary variable *R_flag* is cleared to 0 for the next riding half cycle at the end of the current rising half cycle, and *F_flag* is cleared at the end of the falling half cycle.

The proposed method can ensure that the PWM changes only once each half cycle, and it can eliminate pulse competitions without a time delay as shown in Fig.10.

C. Universal Asynchronous Receiver Transmitter

The master controller is connected to the module controllers via high-speed links made of optical cables, and the data exchange is performed using universal asynchronous receiver transmitter (UART) communication. Fig. 11 shows the self-defined data format of the UART for which downstream data rather than upstream data is taken as an example. Each frame data includes one low level start bit, one high level end bit and several data bits. During the idle time the bus level is set to high. The downstream data that contains the control instruction is 4μs per frame and each frame contains 5 valid bits, including two bits of PWM enable signal, two bits of

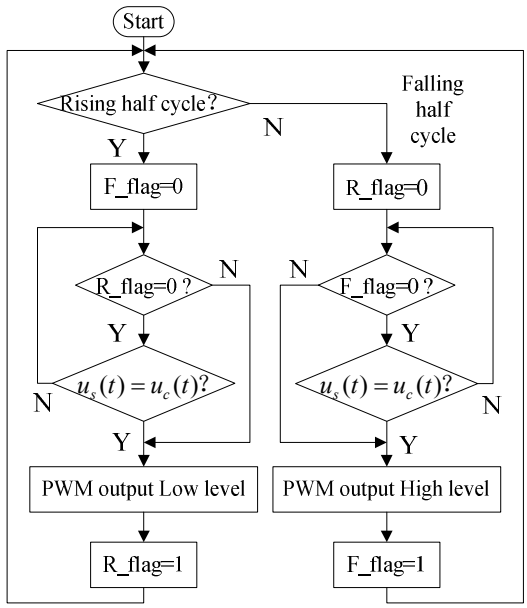


Fig. 9. Flowchart of the proposed pulse competition eliminate algorithm.

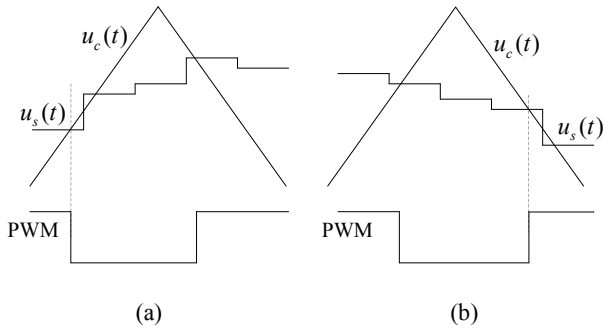


Fig. 10. Demonstration of pulse competitions elimination. (a) Rising half cycle. (b) Falling half cycle.

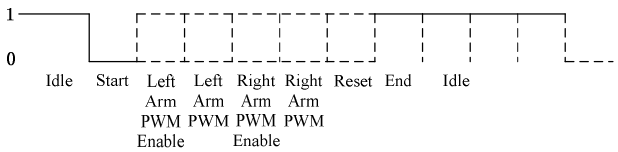


Fig. 11. Self-defined data format of UART.

PWM for each arm and one bit of software reset. Each bit width is 400 ns. Fig. 12 shows the experimental results of the downstream data. The top waveform of the figure is for the overall process of communication, while the bottom one is for the details of a frame data.

The PWM enable signal can be used to perform protection of the inverter modules. The signal is at a high level when the system operates properly and the bridge arms can switch according to the pulses generated by the CPS-PWM generator as shown in Fig. 12(a). Otherwise, the signal is at a low level so that all of the switches of inverter modules are locked as shown in Fig. 12(b).

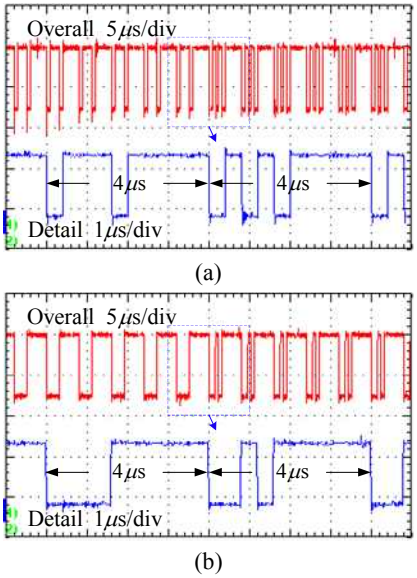


Fig. 12. Experimental results of downstream data (a) PWM unlocked and (b) PWM locked.

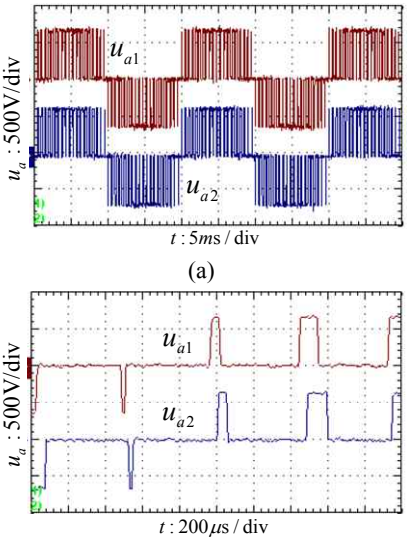


Fig. 13. Output voltages of inverter module 1 and 2 in phase A (a) Overall waveforms and (b) Detailed waveforms.

Then the phase A output voltages of inverter modules 1 and 2 when the DSTACOM is operated using the proposed concentrated controller are shown in Fig. 13. It can be seen that the time delay between the output of the two inverters is about 42μs, which is quite in accordance with the value calculated using (2) for a 12-layer cascaded DSTATCOM with a carrier frequency of 1 kHz.

Fig. 14 shows comparison results between the narrow pulse detection method and the proposed method. u_{ca1} is the phase A output multilevel voltage of a DSTATCOM with the conventional narrow pulse detection method, while u_{ca2} is output voltage with the proposed method. From the detailed waveforms, it is obvious that there are numerous fault voltage

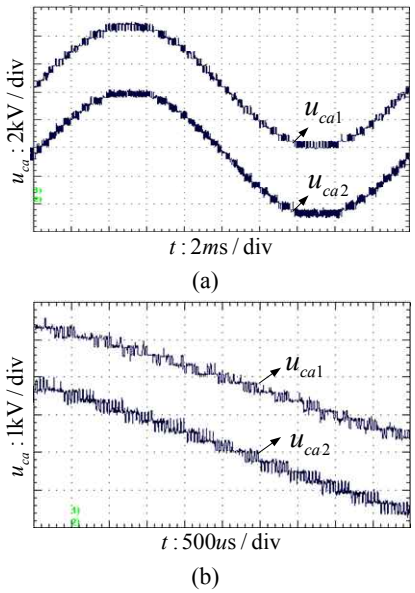


Fig. 14. Comparison results between narrow pulse detection method and the proposed method. (a) Overall waveforms. (b) Detailed waveforms.

TABLE I
MAIN PARAMETERS OF DSTATCOM SYSTEM

Rated power	10 MVar
Line-to-line voltage	10 kV
Grid frequency	50 Hz
AC inductor	2 mH
DC-link capacitor	5.4 mF
DC-link voltage reference	800 V
Cascade number per phase	12
Switching frequency	1.0 kHz
Sampling frequency	5.0 kHz

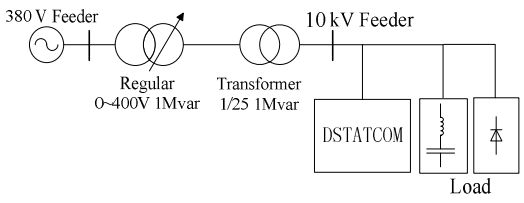
levels on u_{ca1}, while u_{ca2} has better sinusoidal performance.

IV. EXPERIMENTAL STUDY

A 10kV/10Mvar rated three-phase three-wire cascaded DSTATCOM prototype has been manufactured for testing purposes. Fig. 15 shows the configuration and photos of the DSTATCOM prototype as well as the concentrated controller. The main parameters of the DSTATCOM system in this study are listed in Table I. The 10kV feeder is produced by a regular together with a transformer. Limited by the capacity of the feeder, the capacitive load is used to support the feeder. Besides, the maximum dynamic experiment cannot exceed the feeder capacity for safety reasons.

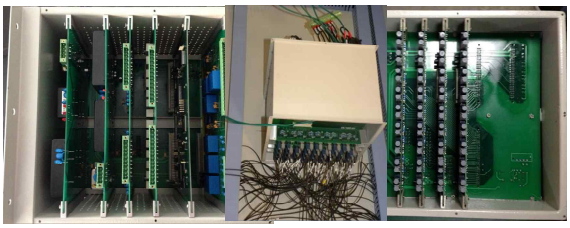
Due to the limitations of the experiment, only the capacitive load consists of a total 2Mvar reactive capacity MSC and harmonic load are available.

First make the prototype work in the current tracking mode. Fig. 16(a) and Fig. 16(b) show the static and dynamic



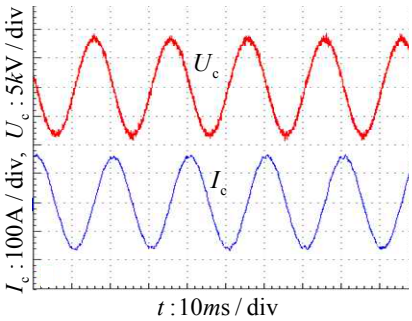
(a)

(b)

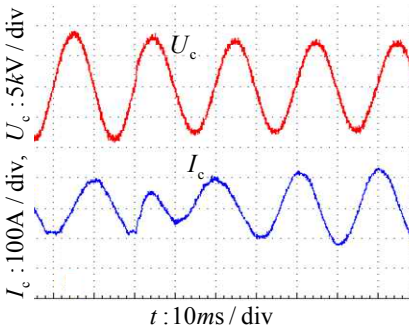


(c)

Fig. 15. Configuration and photos of cascaded DSTATCOM. (a) DSTATCOM configuration. (b) Photo of cascaded DSTATCOM. (c) Photos of concentrated controller.



(a)



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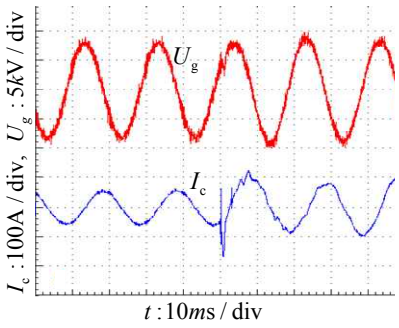
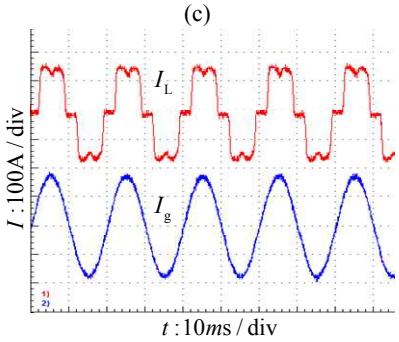


(c)



(d)

Fig. 16. Experimental results of 10kV/10Mvar DSTATCOM prototype (a) 2Mvar capacitive compensation, (b) 1.5Mvar capacitive to inductive compensation, (c) Feeder voltage stabilization and (d) Harmonics compensation.

reactive power compensation results, respectively. Then make the prototype work in the voltage stabilizing mode. Fig. 16(c) gives the dynamic waveforms when the 10kV feeder voltage is mutated. Finally, Fig. 16(d) shows the harmonic compensation results, where the waveforms include the load and grid current. All of the experimental results show that the performance and reliability of the concentrated controller are satisfactory.

V. CONCLUSIONS

A DSP and FPGA based concentrated control is designed for implementing a CPS-SPWM strategy with which PWM synchronization can be simply achieved. A self-defined UART protocol is used for communication between the master controller and the individual module controllers via high speed links. This paper analyzes the generation mechanism of pulse competition and proposes a method for eliminating competition pulses with no time delay. Finally, the proposed concentrated controller is applied to a 10kV/10MVar rated DSTATCOM industrial prototype. The experimental results show the accuracy and reliability of the concentrated controller.

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