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Power Tracking Control of Domestic Induction Heating System using Pulse Density Modulation Scheme with the Fuzzy Logic Controller

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Abstract – Power requirement to the induction heating system varies during the heating process. A closed loop control is required to have a smooth control over the power. In this work, a constant frequency pulse density modulation based power tracking control scheme for domestic induction heating system is developed using the Fuzzy Logic Controller. In the conventional power modulation schemes, the switching losses increase with the change in the load. The proposed pulse density modulation scheme maintains minimum switching losses for the entire load range. This scheme is implemented for the class-D series resonant inverter system. Fuzzy logic controller based power tracking control scheme is developed for domestic induction heating power supply for various power settings. The open loop and closed loop simulation studies are done using the MATLAB/Simulink simulation tool. The control logic is implemented in hardware using the PIC16F877A microcontroller. Fuzzy controller tracks the set power by changing the pulse density of the gate pulses applied to the inverter. The results obtained are used to know the effectiveness of the fuzzy logic controller to achieve the set power.

Keywords: Closed loop control, Fuzzy logic controller, Induction heating, Pulse density modulation

1. Introduction

Induction heating (IH) load requires high frequency power supply to induce high frequency eddy currents in the work-piece which result in heating effect. IH technique is used to produce high temperature for domestic cooking and many industrial applications like steel melting, brazing and surface hardening. For these applications, the operating frequency must be selected based on the work-piece geometry and skin depth requirements [1]. Advanced technology in development of the high frequency semiconductor switches has made it possible to introduce new switching devices with sophisticated functions in a smaller size at a lower price. Recent developments in power electronic devices and switching schemes have made the voltage source fed series resonant inverter (SRI) suitable for IH applications [2-4]. Different modulation schemes for the resonant inverters are developed to vary the output power. The output power can be controlled by varying the switching frequency using pulse frequency modulation (PFM) technique [5-8]. The phase shift (PS) control technique varies the output power by phase shifting the pulses applied to the power switches of the inverter [9-11]. The asymmetrical duty cycle (ADC) control technique employs an unequal duty operation of the switches in the inverter. Accuracy in the output power control is very important in IH applications. For example, domestic cooking appliances require accurate power control over a wide range of load with high efficiency. To improve the efficiency of SRI, zero voltage switching (ZVS) operating condition must be maintained over the entire load range. In the conventional fixed frequency modulation techniques, the ZVS condition is ensured only for limited range of duty cycle [12]. In the above mentioned methods, the output power control is difficult due to the variation of IH load parameters during the heating process [13-15]. With the variation in load parameters, non-ZVS operating condition results during the switching operation which causes more power losses [16, 17]. The above literature does not deal with the power tracking control of domestic induction cooking system using pulse density modulation (PDM). The PDM technique regulates the output power by varying the period in which the inverter injects high frequency current to the induction coil. For the load range of (0-100) %, the ZVS condition is maintained in the PDM based control scheme. This power control scheme satisfies the variable power requirement of the load with the minimum switching losses. Since the switching frequency is not varied, the switching loss is minimum and constant throughout the entire load range. This paper discusses the power control of class-D SRI using PDM technique in open loop and closed loop operation. In the closed loop operation, fuzzy logic controller (FLC) based power tracking of the various power settings is proposed. The PID controller based conventional scheme is replaced with the

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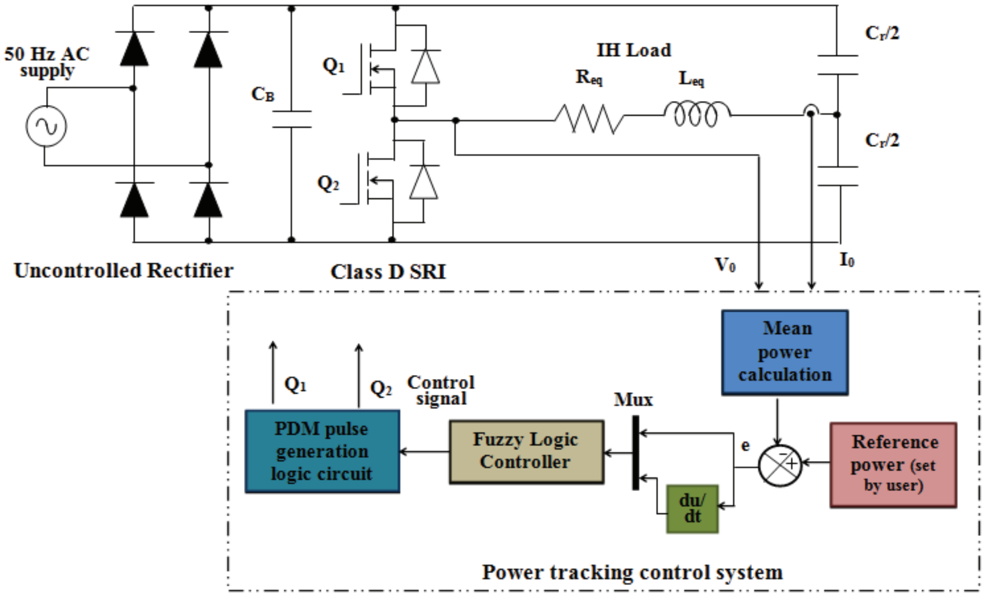


Fig. 1. Schematic diagram of the IH power supply system with the FLC based control scheme

FLC. The closed loop operation ensures the tracking of reference power set by the user in their induction cooking system.

2. Description of the Power Converter

The Fig. 1 shows the main circuit diagram of the class-D SRI fed IH load. Uncontrolled rectifier is used to convert the single phase AC input voltage (V_i) of 50 Hz frequency into DC. In order to filter the ripple content, a DC link capacitor (C_B) is used. Then the DC input voltage (V_B) is given to the inverter to produce high frequency AC which is essential for IH system. This high frequency AC current (i_o) is applied to the IH coil, and the pan gets heated up. R_{eq} and L_{eq} are the equivalent resistance and inductance of the IH coil and the pan. The resonant operating condition is achieved using a resonant capacitor (C_r) which is considered equally on both sides of the bridge. The switches Q_1 and Q_2 are the MOSFET switches with anti-parallel diodes. These switches are alternatively turned on/off with the high frequency PDM pulses generated by the FLC based control scheme to produce the reference power set by the user.

3. Principle of PDM Technique

In PDM technique, the switching frequency of the inverter is kept constant and it is chosen slightly greater than the load resonant frequency in order to reduce the switching losses. The logic circuit for the generation of the PDM based pulses is shown in Fig. 2. High frequency 25 kHz pulses are logically compared with the low frequency 20 Hz pulses. Pulses for the switches Q_1 and Q_2 are generated when the low frequency signal goes high as given in Fig. 3. When the low frequency pulse goes low, the switches Q_1 and Q_2 do not receive the gate pulses and they remain in, off condition.

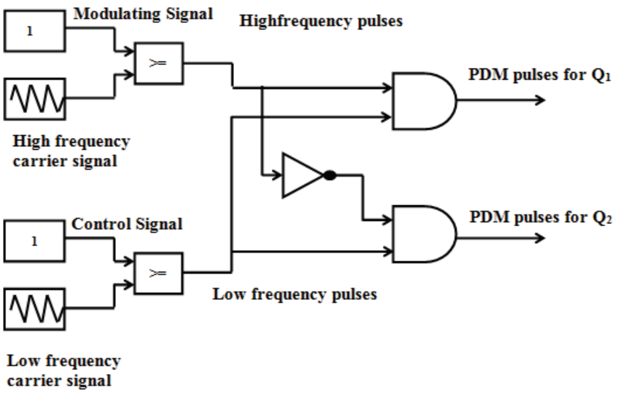


Fig. 2. Gate pulse generation circuit for the switches of the inverter

Waveforms for the output voltage (V_o) and the output current (I_o) of SRI with PDM control are given in Fig. 4.

From the waveforms, it can be observed that the envelope of the current follows a first-order response even though the inverter system is a second order system. For the control of output power, it is important to analyze the output power of the inverter with PDM control. The envelope of the current (i_E) is given by,

$$i_E(t) = I_m\left(1 - e^{\frac{T_{ON}}{\tau}}\right) + I\ e^{-\frac{t}{\tau}}\left(0 \le t \le T_{ON}\right) \tag{1}$$

$$i_E(t) = i_1\left(T_{ON}\right)e^{-\frac{t-T_{ON}}{\tau}}\left(T_{ON} \le t \le T_{PDM}\right) \tag{2}$$

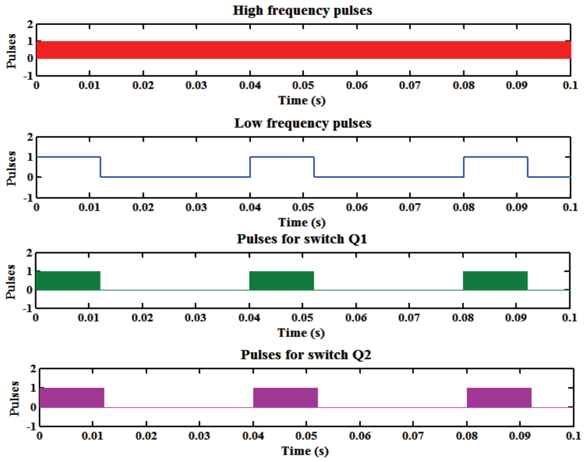


Fig. 3. Generation of the PDM pulses for the switches Q_1 and Q_2

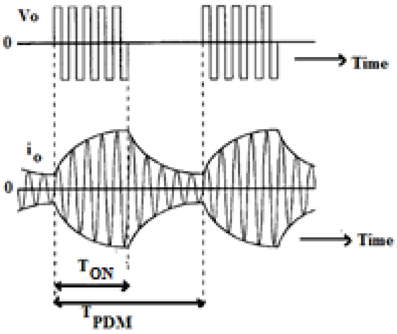


Fig. 4. Key waveforms of the SRI with the PDM control.

$$I = I_m \frac{1 - e^{-\frac{T_{ON}}{\tau}}}{1 - e^{-\frac{T_{PDM}}{\tau}}} \tag{3}$$

Where, T_{PDM} is the total control period for PDM operation and T_{ON} is the total on period of the switch. I is the initial value of the envelope i_E and I_m is the maximum current at the rated power operation of the inverter. The amplitude of the i_E is directly proportional to the pulse density.

$$\lim_{\tau \to \infty} i_E = I_m \left(\frac{T_{ON}}{T_{PDM}} \right) \tag{4}$$

In PDM based SRI, the average output power (P) is obtained by multiplying V_B and i_E as follows,

$$P = \frac{1}{T_{PDM}} \int_0^{T_{ON}} \frac{2}{\pi} V_B i_E(t)\, dt = \frac{2}{\pi} V_B I_M [\frac{T_{ON} + \tau_e^{-\frac{T_{ON}}{\tau}} - \tau}{T_{PDM}}]$$

$$+ \frac{2}{\pi} V_B I_m [\frac{\tau}{T_{PDM}} \frac{e^{\frac{T_{ON}}{\tau}} - 1}{e^{\frac{T_{PDM}}{\tau}} - 1}] \tag{5}$$

$$\left(1 - e^{-\frac{T_{ON}}{\tau}} \right) \tag{6}$$

With $T_{PDM} >> \tau$, the output power is in proportion to the pulse density as given below.

$$\lim_{\tau \to \infty} P = \frac{2}{\pi} V_B I_m \left(\frac{T_{ON}}{T_{PDM}} \right) \tag{7}$$

During every mask period of the pulses, the free-wheeling of resonant current takes place in the load side such that the energy stored in the inductor and capacitor is dissipated in the load. The PDM duty cycle (D_{PDM}) is given by,

$$D_{PDM} = \frac{T_{ON}}{T_{PDM}} \tag{8}$$

The D_{PDM} must be selected such that the low frequency signal must be less than 20 Hz to avoid acoustic noise. The average output power (P_o) can be calculated in terms of D_{PDM} using the following equation.

$$P_o = D_{PDM} P_{rated} \tag{9}$$

Where, P_{rated} is the output power with D_{PDM} equal to one. The output power could be controlled by controlling the D_{PDM}. Since the switching frequency is constant, even with the variation in D_{PDM}, the turn on and turn off instants of the switches are not varied in PDM method. Hence the ZVS condition is maintained throughout the load cycle. This reduces the switching losses in the high frequency SRI.

4. Simulation Results

4.1 Open loop study of IH system with PDM control

The simulink model of the open loop system with class-D resonant inverter is shown in Fig. 5. The parameters used for the simulation are listed below: f_s=25 kHz, R_{eq}=5 Ω, L_{eq}=0.3 mH, C_r/2=0.65µF, P_{rated}=100 W. The PDM pulses for the switches Q_1 and Q_2 are generated as discussed earlier. By varying the D_{PDM} of the low frequency signal, the output power can be controlled. The rated output power is obtained for the D_{PDM} of 100%. To prove the variation in power with the D_{PDM} signal, the simulation is carried out for duty cycles of 70% and 30% respectively. For the rated power of 100W, the high switching frequency (f_s) and the low frequency (f_{PDM}) are chosen as 25 kHz and 20 Hz respectively. Fig. 6(a) illustrates the output voltage waveform with 70% of D_{PDM}.

The output current and the real power for 70% of D_{PDM}

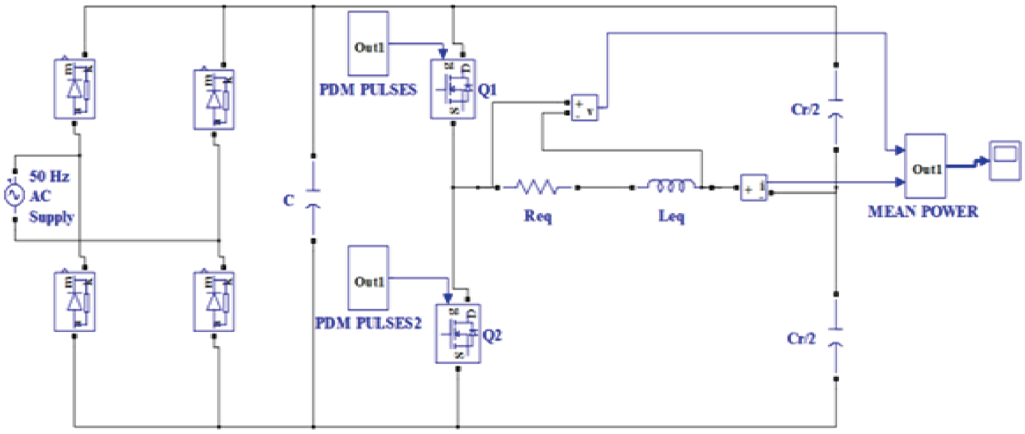
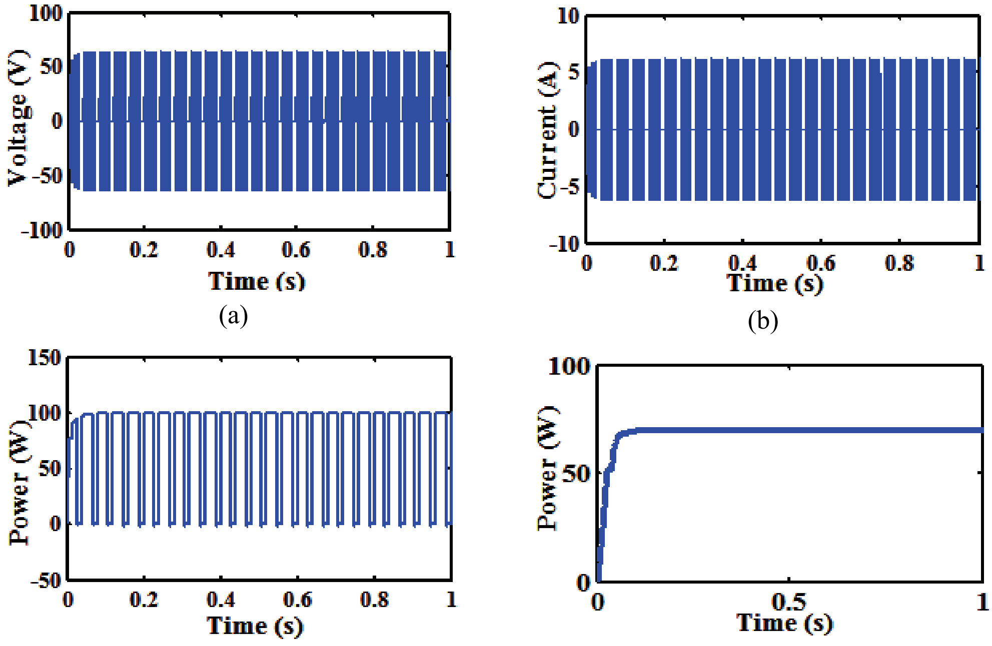


Fig. 5. Simulink model of the open loop system



(a) (b)

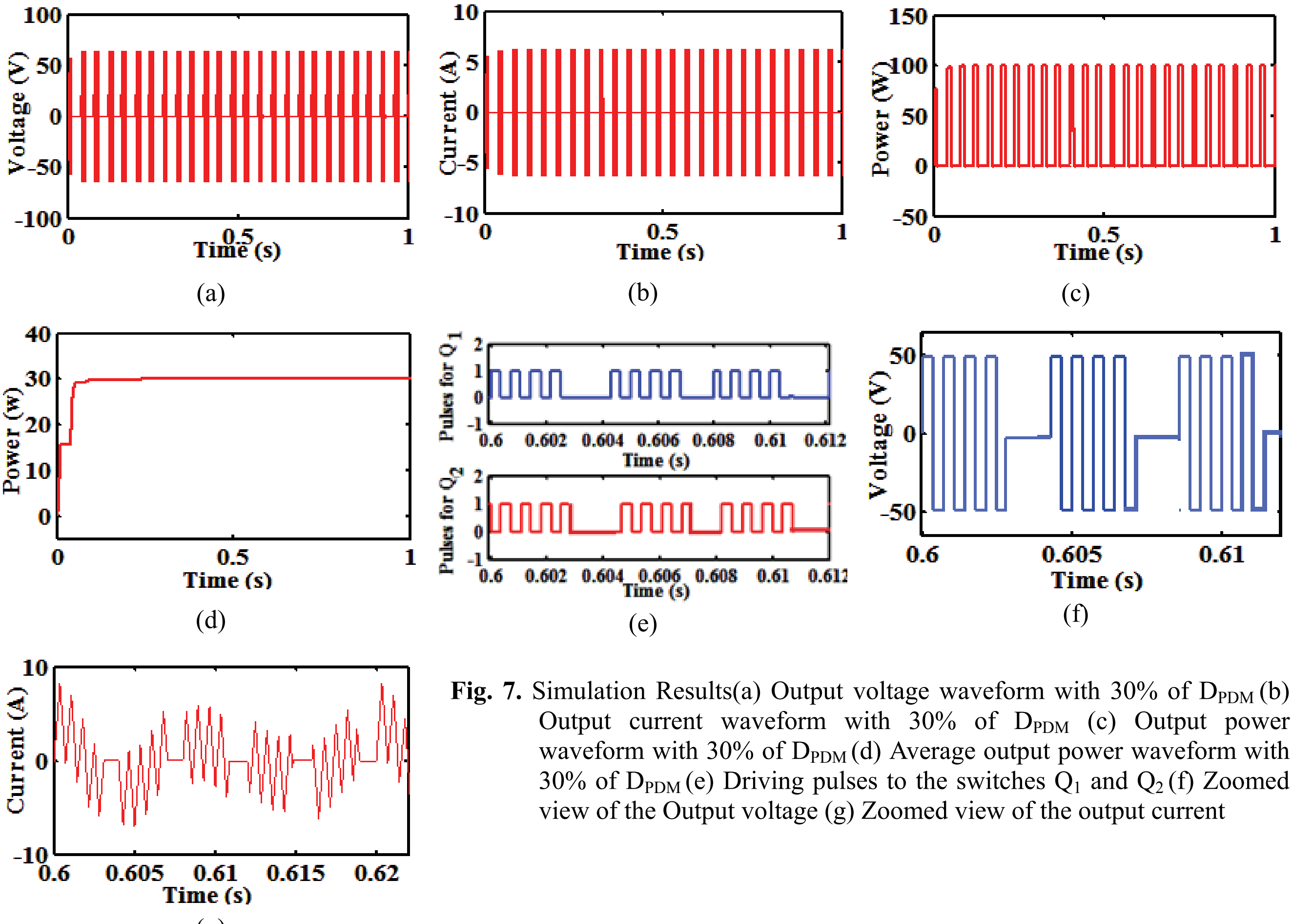
(c) (d)

Fig. 6. Simulation Results (a) Output voltage waveform with 70% of D_{PDM} (b) Output current waveform with 70% of D_{PDM} (c) Output power waveform with 70% of D_{PDM} (d) Average output power with 70% of D_{PDM}

are presented in Figs. 6(b) and Fig. 6(c) respectively. Since the voltage and current are in discontinuous form, the average value of the power is measured and it is shown in Fig. 6(d). When the D_{PDM} is 70%, the average current and the voltage get lowered due to the discontinuous flow of V_o and I_o. This causes the reduction of the average output power from 100 W to 70 W. Similarly the switches are operated with D_{PDM} of 30% and the corresponding waveforms of output voltage, output current , instantaneous power and average output power are shown in Figs. 7(a), 7(b), 7(c) and 7(d) respectively. The average power is about 30W with 30% D_{PDM}. The output voltage is a high frequency waveform and hence the driving pulses to the switches, the zoomed view of the voltage and current are shown in Figs 7(e), 7(f) and 7(g) respectively. The average output power changes linearly with the change in the value of the $D_{PDM,}$ in PDM technique. It has been found from the simulation results that, by controlling the D_{PDM} from 0% to 100%, the average value of the output power can be controlled.

4.2 FLC based power control of IH load

In domestic IH system, according to the heating requirement, the power setting is changed by the user. Different modulation schemes are available to perform power control for IH load. This section discusses the development of FLC for the power control of IH system using PDM technique.



(a)

(b)

(c)

(d)

(e)

(f)

(g)

Fig. 7. Simulation Results(a) Output voltage waveform with 30% of D_{PDM} (b) Output current waveform with 30% of D_{PDM} (c) Output power waveform with 30% of D_{PDM} (d) Average output power waveform with 30% of D_{PDM} (e) Driving pulses to the switches Q_1 and Q_2 (f) Zoomed view of the Output voltage (g) Zoomed view of the output current

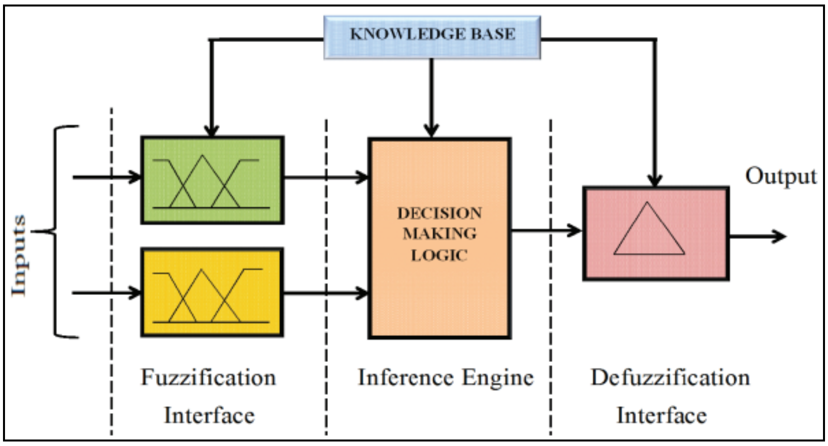


Fig. 8. Block diagram of FLC

Fuzzy logic is a nonlinear control technique, which is applied to the control of converters to improve the performance of the system as suggested in literature [18-20]. Expert knowledge plays a vital role in designing the FLC and it could be used in the system which has large variations of input voltage or load. The performance of the controller is evaluated by the number of linguistic variables, the control range of linguistic variable and the slope of membership function. The fuzzy controller is robust to the variations in input DC voltage and load. FLC does not require the mathematical model of the system / process as like conventional controller but it is necessary to understand the system / process and the control requirements.

The information / data (control input variable) flows must be designed by the fuzzy controller designer, then the information / data is processed (control strategy and decision), and the corresponding control data flows out

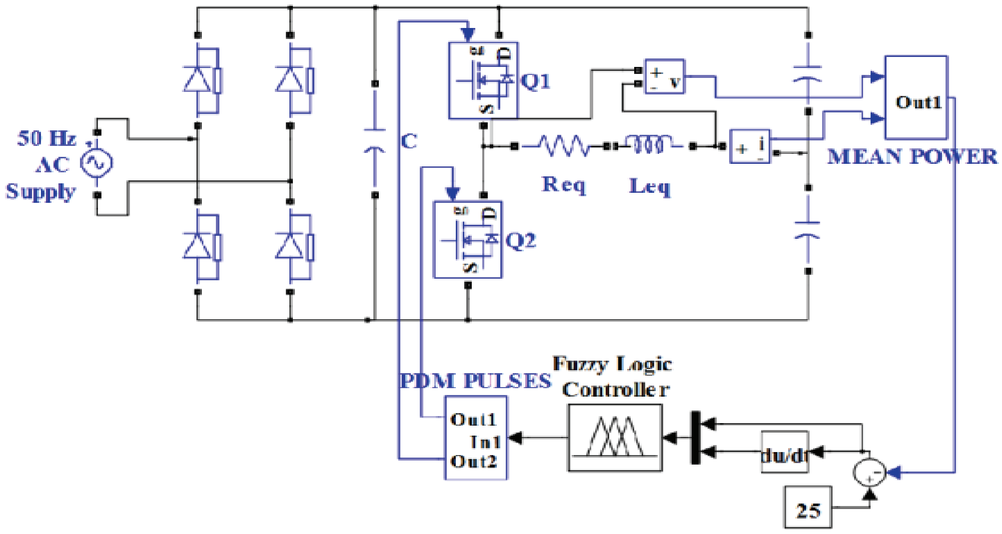


Fig. 9. Simulink model of the FLC based closed loop controlled IH power supply system.

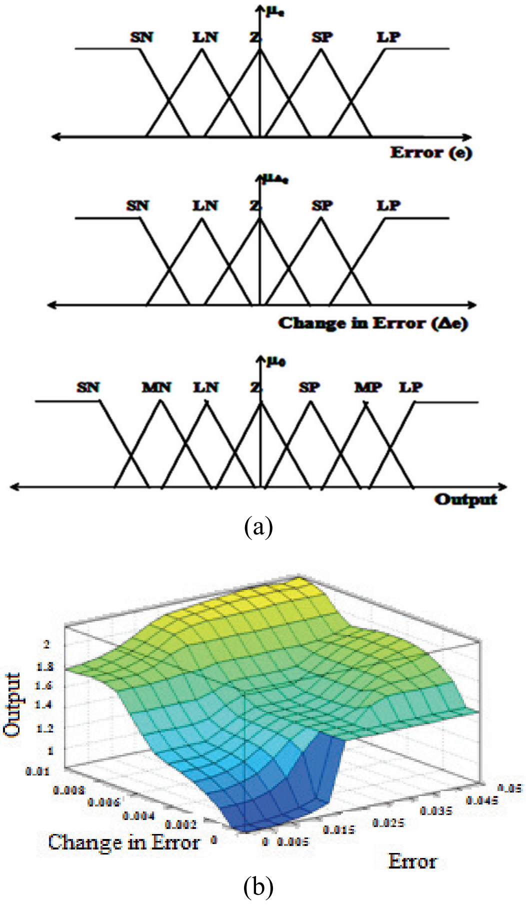
of the system (solution / output variable). The major development of fuzzy logic was primarily designed to represent and reason with some particular form of knowledge. The basic configuration of the fuzzy logic system is shown in Fig. 8.

The operation of the FLC involves three modules. They are fuzzification interface, knowledge based fuzzy reasoning mechanism and defuzzification modules to produce the control signal necessary for the plant. Fuzzy reasoning mechanism is used to convert the measured crisp values into fuzzy linguistic values. This process is called as fuzzification. In order to achieve the control goal, the collections of expert's control rules (knowledge) are needed. They are called as knowledge base. In this process, the fuzzy logic operations and the control actions are taken according to the fuzzy inputs. The process of converting the fuzzified values into the crisp value is called as defuzzification. The centre of area or centroid defuzzification is the most frequently used defuzzification technique which is also used in this work and is characterized by

$$y = \frac{\sum \mu_i y_i}{\sum \mu_i} \tag{10}$$

Where y represents the crisp value of the output of the fuzzy controller and μ is its membership grade. The MATLAB Simulink tool is used to test the performance of the FLC in the output power control of IH load. The output power needs to be varied according to the reference value set by the user. This is an important objective of the FLC based closed loop system considered in this work.

The simulink model of the closed loop control using FLC is shown in Fig. 9. The mean power is measured and compared with the set power to find the error (e). The inputs to the FLC are the error and the derivative of the error (Δe) in power. The output of the controller is the control signal used to vary the D_{PDM}. The two inputs and one output of FLC are divided into five triangular membership functions as shown in Fig. 10(a).



(a)

(b)

Fig. 10. (a) Membership function of the input and output variables of the FLC (b) Surface plot for error, change in error and control variable

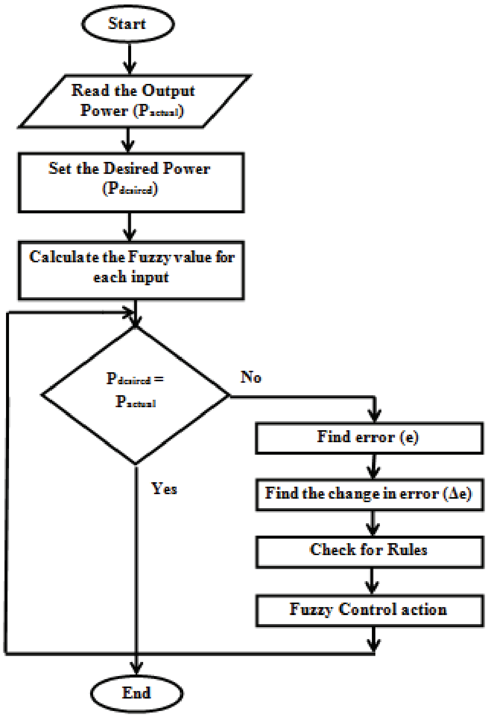


Fig. 11. Flow chart for the FLC based power control

With the basic control knowledge of diverging and converging system, the control action involved is based on the simple linguistic rules which are listed below.

1) If the error is large, change of D_{PDM} must be large to bring the output equal to the reference power.
2) If the error is near zero, small change of D_{PDM} is needed.
3) If the error is near zero and the derivative of error is large, the D_{PDM} should be kept constant.
4) When the set point is reached and the output still changes, a very small change in D_{PDM} is necessary to prevent the output moving away from the required value.

The surface plot which shows the variation of the controller output corresponding to the e and Δe is shown in Fig. 10 (b).

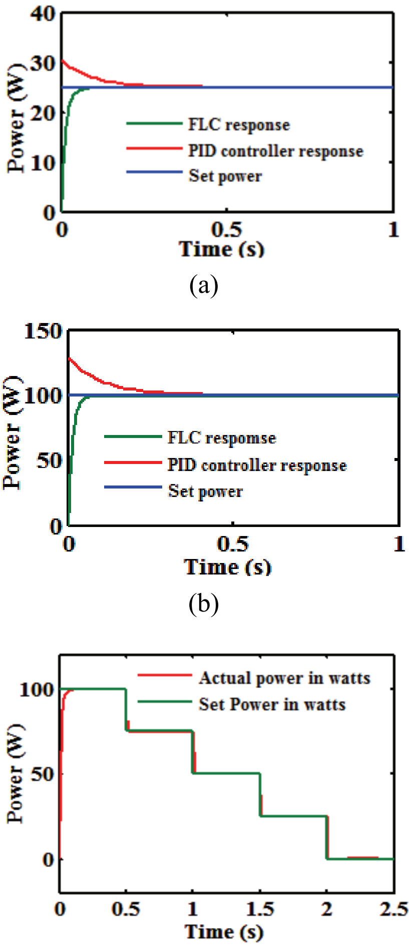
The rule base is developed for FLC scheme with the above points as reference and they are listed in Table 1. The flowchart of the FLC based power control is shown in Fig. 11. The control signal produced by the controller, based on the rule base is used to generate the PDM gate signals to the switches. The FLC is designed such that it tracks the reference power by changing the D_{PDM} of the PDM signals.

The control signal at the output of the PID controller is U(s) and it can be defined as

$$U(s) = (K_p + \frac{K_i}{S} + K_d S)e(s) \qquad (11)$$

Table 1. Fuzzy rule base

e/Δe	SN	LN	Z	SP	LP
SN	LP	MP	MP	LN	SN
LN	SP	MN	LN	MP	LN
Z	SP	MP	Z	LN	SN
SP	LP	LN	MN	LP	Z
LP	MP	MN	SN	LN	LN



(a)

(b)

(c)

Fig.12. (a) Response with PID controller and FLC for set power of 25W (b) Response with PID controller and FLC for set power of 100 W (c) Response of the system with FLC for variation of the power from 100 W to 0 W

Where K_p, K_i and K_d are the proportional, integral and derivative gains of the PID controller for the given operating conditions. For the set power of 25 W, the values of the K_p, K_i and K_d are equal to 0.9, 1.6 and 2.3 respectively. The gains of the PID controller are obtained using Ziegler and Nichols method. The control signal U(s) is used to produce the PDM based gate signals necessary to track the output power.

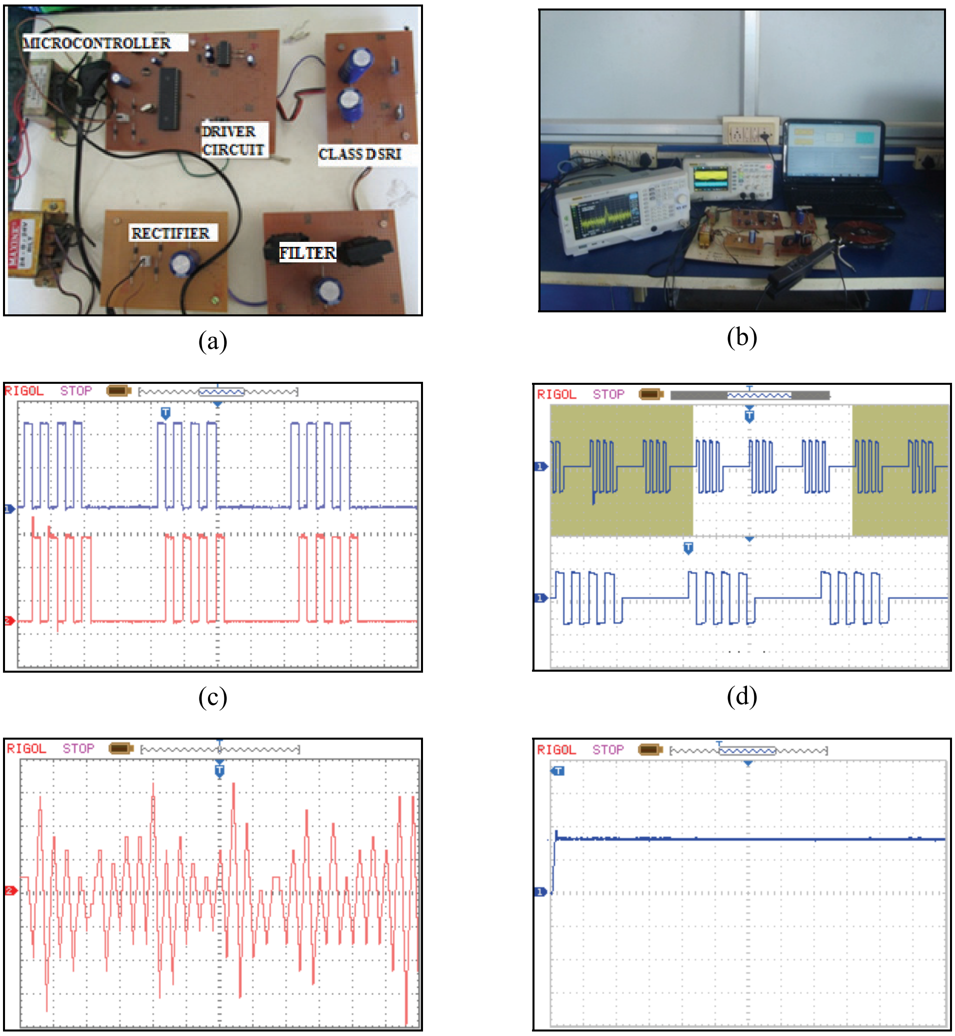
Figs. 12(a) and (b) illustrate the response of the system with the PID controller and FLC for the set power of 25 W and 100 W respectively. For the given values of the gains, the PID controller tracks the output power only for the set power of 25W. It has been found from the simulation study that the the PID controller requires different values of the gains when the set power is varied.

The variation of output power from 100 W to 0 W using the FLC is shown in Fig. 12 (c). The green line indicates the reference power. For every 0.5s, the reference power setting is made to decrease by 25 W from the rated power of 100W. The red line indicates the actual power of the inverter. It can be noted that the output power follows the reference power. Both the controllers track the reference power with zero steady state error. The effectiveness of the FLC can be studied using the settling time (t_s). The comparison of the system using the conventional and the proposed controller for different values of set power are given in Table 2.

The PID controller and FLC system reach the steady state with the settling time of 0.44s and 0.075s respectively for the reference power of 25 W. Thus a fast and smooth transition of power control is possible using the FLC without any oscillation. It is also observed that the proposed FLC tracks the output power for the entire power range whereas the PID controller requires tuning of the controller for every set value due to the nonlinear nature of the load.

Table 2. Comparison of the performance parameters with the PID and fuzzy logic controllers

Parameters	PID controller			
P_s(W)	25	50	75	100
t_s(s)	0.44	0.47	0.59	0.76
Parameters	FLC			
P_s(W)	25	50	75	100
t_s(s)	0.075	0.06	0.052	0.049



(a) (b) (c) (d) (e) (f)

Fig.13. Hardware Results (a) Hardware layout of the IH power supply system (b) Test set up of the Hardware (c) Driving pulses to the switches Q_1 and Q_2 (X axis 1cm = 2V, Y axis 1 cm=100 µs) (d) Output Voltage (X axis 1cm= 30V, Y axis 1 cm=100 µs) (e) Output current (X axis 1cm= 2A, Y axis 1 cm=200 µs) (f) Response of the system with FLC for set power of 25W (X axis 1cm= 15 W, Y axis 1 cm=100 µs).

5. Experimental Results

A prototype of high frequency AC power supply circuit rated for 100 W was fabricated to validate the control scheme in class D inverter circuit. The simulation results of the IH power supply system using the proposed control technique are validated using the experimental results. The hardware layout of the system and the test setup of the system are shown in Figs.13(a) and 13(b) respectively. The full bridge uncontrolled rectifier was constructed using the four IN5408 diodes to supply DC to the class D inverter. The class D inverter was constructed using two IRF840 MOSFET switches for the conversion of DC into high frequency AC.

The control circuit for the PDM control strategy is implemented using a PIC16F877A micro controller. The micro controller produces the PDM pulses required by the switches Q_1 and Q_2. The pulses from the controller are amplified using IR2110 driver. It also provides the isolation between the power circuit and the control circuit. The output pulses from the driver circuit are shown in Fig. 13(c). The output voltage and current of SRI with D_{PDM} of 25% are shown in Figs. 13(d) and 13(e) respectively. The current is measured using SIGLENT CP4060 type current probe. The waveforms are recorded using the RIGOL DS1052E type digital oscilloscope. The response of the system with FLC is shown in Fig. 13 (f). It can be observed that these oscillograms follow the theoretical and simulation results discussed in the previous sections. The obtained results confirm that the FLC track the set power with less settling time.

6. Conclusion

In this paper, the high-frequency IH power supply system is discussed with PDM technique and the power control is done using the FLC. The open and closed loop circuit models with PDM control are developed and they are successfully used for the simulation studies. The detailed study on PDM based SRI confirms the power control through the PDM duty cycle variation without the change in frequency. Experimental verification is also done through the PIC16F877A microcontroller. The PDM operation maintains soft switching condition for the entire load cycle. The closed loop control using PDM based FLC confirms that it tracks the reference power for the whole range of operation with different power settings. The proposed FLC system provides fast response. However, it requires the complete knowledge of the system to develop the rule base. The hardware response of the inverter system can be improved by replacing the PIC controller with DSP controller.

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