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Improvement of Responsivity of Unified Power Flow Controller in Digital Control System

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Abstract – The Unified Power Flow Controller (UPFC) can flexibly manage power flow and maintain line voltage. The UPFC consists of two inverters in parallel side and series side. In parallel side, the reactive power can be compensated to improve the power factor. In series side, the voltage drop can be compensated to maintain proper line voltage. It is necessary for the operation in both sides to output the current and the voltage quickly and accurately. As the method for the UPFC control, the deadbeat control with state observer is applied. The deadbeat control is able to realize a quick response of the current and voltage control for only a sampling period compared with the general PI control. A principle and simulation results are presented in this paper.

Keywords: Unified power flow controller, Reactive power compensation, Voltage drop compensation, Deadbeat control

1. Introduction

In recent years, as distributed generation systems increase in the power line, energy conservation and stable supply of power is getting to be required. In the power transmission, power factor drop caused by the reactive component of the load and the voltage drop due to unexpected accident occur. The reduction of power quality becomes the problem. FACTS components which can flexibly control the power flow and line voltage are investigated and developed. The Unified Power Flow Controller (UPFC)[1]-[7] is one of the FACTS components. The UPFC consists of two inverters with a common DC capacitor and is able to perform the reactive power compensation and the voltage drop compensation. It is possible to improve the power quality by using the UPFC. On the other hand, a digital control system by software is applied to control the UPFC flexibly. In order to obtain good compensation performance of the UPFC in the digital system, it is necessary to control output current and voltage quickly and accurately. In this study, the deadbeat (DB) control[8][9] is applied to improve the responsivity. The deadbeat control is able to realize a quick response of the current and voltage control for only a sampling period compared with the general PI control. Theory of the proposed control method and simulation results are presented in this paper.

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2. Control Method

2.1 Configuration of UPFC

A circuit configuration of the UPFC is shown in Fig.1. The UPFC consists of two inverters with a common capacitor on DC bus and output filters on each AC bus. A block diagram of Parallel side with the deadbeat control is shown in Fig.2. In parallel side, the reactive power is compensated to improve the power factor. At the same time, in order to keep the voltage of the common DC capacitor, the output current for the active power is controlled by the parallel side inverter. The deadbeat control makes the current follow to the calculated current reference quickly and accurately.

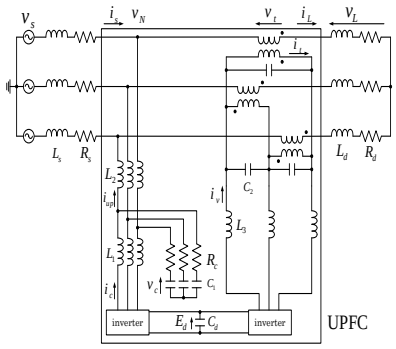

Fig. 1. Circuit configuration of UPFC

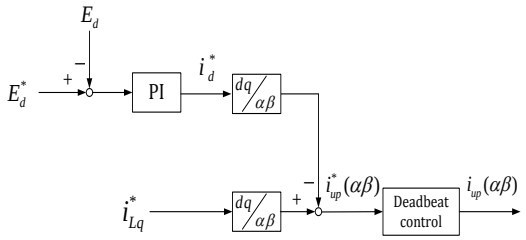

Fig. 2. Block diagram of parallel side of the UPFC

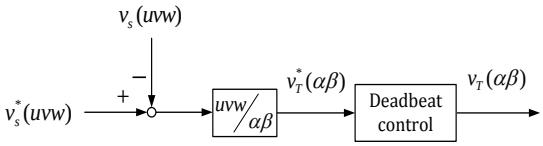

Fig. 3. Block diagram of series side of the UPFC

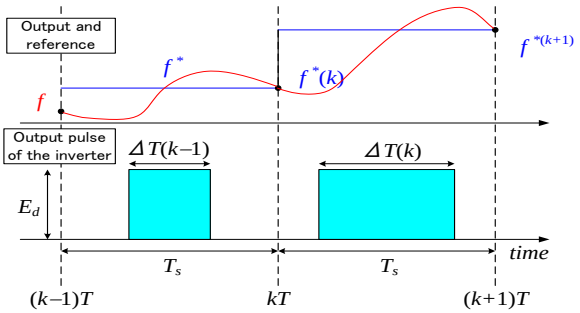

Fig. 4. Principle of the DB control

A block diagram of series side with the deadbeat control is shown in Fig.3. In series side, the voltage drop is compensated to maintain proper line voltage. It is necessary to control with quick and accurate response because the control performance directly affects the compensation performance.

The deadbeat control is independently applied to regulate the output current in parallel side and output voltage in series side. Principle of the DB control is shown in Fig.4. In the proposed scheme, each output can be controlled by changing the output pulse width $\Delta T(k)$ of the inverter. It is determined from detected currents and voltages by a sampling period using the theoretical formula obtained from the state equation of the system.

2.2 DB control of parallel side

Fig.5 shows a single phase equivalent circuit of parallel side for analysis of the deadbeat control. Theory of single phase circuit is applied to three phase using α-β transform. The detail about it will be described in section 2.4.

The output pulse width can be obtained by calculating from the detected i_c, i_{up}, v_c and v_N. v_N, which is voltage of

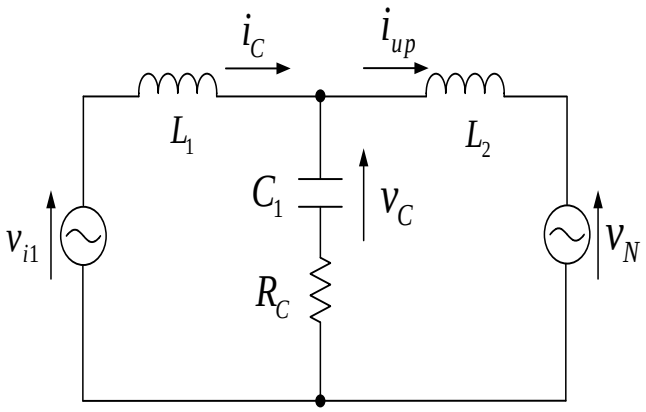

Fig. 5. Analysis model of parallel side (single phase)

connected point, is regarded as a disturbance in the control of parallel side. When four parameters i_c, v_c, i_{up}, and v_N are selected as the states, the state equations are obtained as follows.

$$\frac{d}{dt}\boldsymbol{x_1} = \boldsymbol{A_1}\boldsymbol{x_1} + \boldsymbol{b_1}v_{i1} \tag{1}$$

$$i_{up} = \boldsymbol{c_1}\boldsymbol{x_1}$$

$$\boldsymbol{x_1} = \begin{bmatrix} i_c \\ v_c \\ i_{up} \\ v_N \end{bmatrix} \quad \boldsymbol{A_1} = \begin{bmatrix} -\frac{R_c}{L_1} & -\frac{1}{L_1} & \frac{R_c}{L_1} & 0 \\ \frac{1}{C_1} & 0 & -\frac{1}{C_1} & 0 \\ \frac{R_c}{L_2} & \frac{1}{L_2} & -\frac{R_c}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad \boldsymbol{b_1} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\boldsymbol{c_1} = \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix} \tag{2}$$

(1) and (2) can be converted into (3) and (4), which are expressions of the discrete time system using the o utput pulse width ΔT in Fig.4.

$$\boldsymbol{x}_1(k+1) = \boldsymbol{F}\boldsymbol{x}_1(k) + \boldsymbol{g}\Delta T_1(k) \tag{3}$$

$$i_{up}(k) = \boldsymbol{c}_1\boldsymbol{x}_1(k) \tag{4}$$

The matrixes $\boldsymbol{F}$ and $\boldsymbol{g}$ are calculated by (5), and become constant.

$$\boldsymbol{F} = e^{\boldsymbol{A}_1 T_s}, \quad \boldsymbol{g} = e^{\frac{\boldsymbol{A}_1 T_s}{2}} \boldsymbol{b}_1 E_d \tag{5}$$

$$\boldsymbol{F}=\begin{bmatrix} F_{11} & F_{12} & F_{13} & F_{14} \\ F_{21} & F_{22} & F_{23} & F_{24} \\ F_{31} & F_{32} & F_{33} & F_{34} \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \boldsymbol{g}=\begin{bmatrix} g_1 \\ g_2 \\ g_3 \\ g_4 \end{bmatrix} \tag{6}$$

(6) is obtained from (3)-(5).

$$i_{up}(k+1)=F_{31}i_c(k)+F_{32}v_c(k)+F_{33}i_{up}(k)+F_{34}v_N+g_3\Delta T_1(k) \tag{6}$$

The pulse width $\Delta T_1(k)$ can be calculated as (7) when $i_{up}(k+1)$ is replaced to $i_{up}^*(k+1)$.

$$\Delta T_1(k)=\frac{i_{up}^*(k+1)-F_{31}i_c(k)-F_{32}v_c(k)-F_{33}i_{up}(k)-F_{34}v_N(k)}{g_3} \tag{7}$$

When $\Delta T_1(k)$ is negative, the inverter DC voltage is given as $-E_d$ of width $|\Delta T_1|$. By outputting the calculated $\Delta T_1(k)$, $i_{up}(k+1) = i_{up}^*(k+1)$ can be realized after a sample period.

2.3 DB control of series side

Fig.6 shows a single phase equivalent circuit of series side for analysis of the deadbeat control. The output pulse width is obtained by calculating from the detected i_v, v_t and I_t. I_t, which is current of transformer depends on load current, is regarded as a disturbance in the control of series side. v_t is primary voltage of transformer.

When three parameters i_v, v_t, and I_t are selected as the states, the state equations are obtained as follows.

$$\frac{d}{dt}\boldsymbol{x}_2=\boldsymbol{A}_2\boldsymbol{x}_2+\boldsymbol{b}_2 v_{i2} \tag{8}$$

$$v_t=\boldsymbol{c}_2\boldsymbol{x}_2 \tag{9}$$

$$\boldsymbol{x}_2=\begin{bmatrix} v_t \\ i_v \\ i_t \end{bmatrix} \quad \boldsymbol{A}_2=\begin{bmatrix} 0 & \frac{1}{3C_2} & -\frac{1}{C_2} \\ -\frac{1}{L_3} & 0 & \frac{1}{L_3} \\ 0 & 0 & 0 \end{bmatrix} \quad \boldsymbol{b}_2=\begin{bmatrix} 0 \\ \frac{1}{L_3} \\ 0 \end{bmatrix}$$

$$\boldsymbol{c}_2=\begin{bmatrix} 1 & 0 & 0 \end{bmatrix}$$

(8) and (9) can be converted into (10) and (11) of the discrete time system by giving the output pulse width ΔT_2 as show in Fig.4.

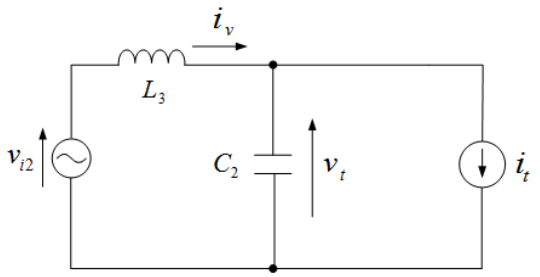

Fig. 6. Analysis model of series side (single phase)

$$\boldsymbol{x}_2(k+1)=\boldsymbol{M}\boldsymbol{x}_2(k)+\boldsymbol{n}\Delta T_2(k) \tag{10}$$

$$v_t(k)=\boldsymbol{c}_2\boldsymbol{x}_2(k) \tag{11}$$

$$\boldsymbol{M}=e^{\boldsymbol{A}_2 T_s},\ \boldsymbol{n}=e^{\frac{\boldsymbol{A}_2 T_s}{2}}\boldsymbol{b}_2 E_d \tag{12}$$

$$\boldsymbol{M}=\begin{bmatrix} M_{11} & M_{12} & M_{13} \\ M_{21} & M_{22} & M_{23} \\ 0 & 0 & 1 \end{bmatrix} \quad \boldsymbol{n}=\begin{bmatrix} n_1 \\ n_2 \\ n_3 \end{bmatrix}$$

The matrixes $\boldsymbol{M}$ and $\boldsymbol{n}$ are calculated by (12) and become constant. (13) is obtained from (10)-(12).

$$v_t(k+1)=M_{11}v_t(k)+M_{12}i_v(k)+M_{13}I_t(k)+n_1\Delta T_2(k) \tag{13}$$

The pulse width $\Delta T(k)$ can be calculated in (14) when $v_t(k+1)$ equals to $v_t^*(k+1)$.

$$\Delta T_2(k)=\frac{v_t^*(k+1)-M_{11}v_t(k)-M_{12}i_v(k)-M_{13}i_t(k)}{n_1} \tag{14}$$

By outputting the calculated $\Delta T_2(k)$, $v_t(k+1) = v_t^*(k+1)$ can be realized after a sampling period.

2.4 Output of three phase pulse

Fig.7 illustrates the timing of the calculation of the observer and the pulse width. Generally the time delay occurs due to the CPU calculation time. To secure the computing time, the state observer is designed. The calculation of the pulse width is accomplished using the states obtained by the observer during the previous sampling period. The estimated states $\hat{i}_c$ and $\hat{v}_c$ in the parallel side are obtained by

(15) when the observer of the state variable $\boldsymbol{x}_{c1}$ is designed. $\hat{\boldsymbol{x}}_{c1}$ is estimated value of $\boldsymbol{x}_{c1}$.

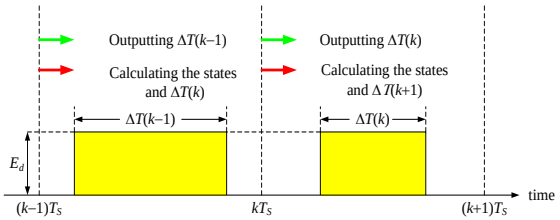

Fig. 7. Timing of DB control calculation and pulse output

$$\hat{\boldsymbol{x}}_{c1}(k)=\boldsymbol{F}_c\hat{\boldsymbol{x}}_{c1}(k-1)+\boldsymbol{F}_a\hat{\boldsymbol{x}}_{a1}(k-1)+\boldsymbol{g}_c\Delta T_1(k-1) -\boldsymbol{L}_{c1}\{i_c(k-1)-\boldsymbol{c}_{c1}\hat{\boldsymbol{x}}_{c1}(k-1)\} \quad (15)$$

$$\boldsymbol{x}_{c1}(k)=\begin{bmatrix} i_c(k) \\ v_c(k)\end{bmatrix} \quad \boldsymbol{x}_{a1}(k)=\begin{bmatrix} i_{up}(k) \\ 0\end{bmatrix}$$

$$\boldsymbol{F}_c=\begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22}\end{bmatrix} \quad \boldsymbol{F}_a=\begin{bmatrix} F_{13} & F_{14} \\ F_{23} & F_{24}\end{bmatrix}$$

$$\boldsymbol{g}_c=\begin{bmatrix} g_1 \\ g_2\end{bmatrix} \quad \boldsymbol{c}_{c1}=\begin{bmatrix}1 & 0\end{bmatrix} \quad \boldsymbol{L}_{c1}=\begin{bmatrix} l_1 \\ l_2\end{bmatrix}$$

l_1 and l_2 are the gain of the observer, which are determined to keep the stability. v_N and i_{up} are calculated by (16) and (17).

$$\hat{v}_N(k)=v_N(k-1)+K_v\{v_N(k)-v_N(k-1)\} \quad (16)$$

$$\hat{i}_{up}(k)=i_{up}(k-1) \quad (17)$$

The inverter output pulse width $\Delta T_1(k)$ in (7) is modified to (18) by using the estimated states $\hat{i}_c(k)$, $\hat{v}_c(k)$, $\hat{v}_N(k)$ and $\hat{i}_{af}(k)$.

$$\Delta T_1(k)=\frac{i_{up}^*(k+1)-F_{31}\hat{i}_c(k)-F_{32}\hat{v}_c(k)-F_{33}\hat{i}_{up}(k)-F_{34}\hat{v}_N(k)}{g_3} \quad (18)$$

The state observer for the series side is designed the same as the parallel side. The estimated states $\hat{v}_t$ and $\hat{i}_t$ in the series side are obtained by (19), when the observer of the state variable $\boldsymbol{x}_{c2}$ is designed.

$$\hat{\boldsymbol{x}}_{c2}(k)=\boldsymbol{M}_c\hat{\boldsymbol{x}}_{c2}(k-1)+\boldsymbol{M}_a\hat{x}_{a2}(k-1)+\boldsymbol{n}_c\Delta T_2(k-1) -\boldsymbol{L}_{c2}\{v_t(k-1)-\boldsymbol{c}_{c2}\hat{\boldsymbol{x}}_{c2}(k-1)\} \quad (19)$$

$$\hat{i}_t(k)=i_t(k-1) \quad (20)$$

$$\boldsymbol{x}_{c2}(k)=\begin{bmatrix} v_t(k) \\ i_v(k)\end{bmatrix} \quad x_{a2}(k)=i_t(k)$$

$$\boldsymbol{M}_c=\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22}\end{bmatrix} \quad \boldsymbol{M}_a=\begin{bmatrix} M_{13} \\ M_{23}\end{bmatrix}$$

$$\boldsymbol{n}_c=\begin{bmatrix} n_1 \\ n_2\end{bmatrix} \quad \boldsymbol{c}_{c2}=\begin{bmatrix}1 & 0\end{bmatrix} \quad \boldsymbol{L}_{c2}=\begin{bmatrix} l_3 \\ l_4\end{bmatrix}$$

The inverter output pulse width $\Delta T_2(k)$ in (14) is modified to (21) by using the estimated states $\hat{v}_t(k)$, $\hat{i}_v(k)$, and $\hat{i}_t(k)$.

$$\Delta T_2(k)=\frac{v_t^*(k+1)-M_{11}\hat{v}_t(k)-M_{12}\hat{i}_v(k)-M_{13}\hat{i}_t(k)}{n_1} \quad (21)$$

2.5 Output of three phase pulse

(18) and (21) derived from Figs.5 and 6 are expressions in a single phase. Those can be extended to three phase. Three phase currents are transformed into α-β components by (22).

$$\begin{bmatrix} i_\alpha \\ i_\beta\end{bmatrix}=\frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix} i_u \\ i_v \\ i_w\end{bmatrix} \quad (22)$$

Three phase voltages are also calculated by the same matrix of (22). And line-to-line voltages are transformed into α-β components by (23).

$$\begin{bmatrix} v_\alpha \\ v_\beta\end{bmatrix}=\frac{2}{3}\begin{bmatrix} \frac{1}{2} & 0 & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & 0\end{bmatrix}\begin{bmatrix} v_{uv} \\ v_{vw} \\ v_{wu}\end{bmatrix} \quad (23)$$

All the detected currents and voltages for the control are transformed by (1) and (2) respectively. The α and β components are independent without interference. Thus, each component can be treated as a single phase component and applied to the proposed DB control in (18) or (21). The pulse widths ΔT_α and ΔT_β are determined from (18) and (21) respectively. The pulse width ΔT_α and ΔT_β are converted into three phase pulse. (24) shows the transformation to the three phase pulse.

$$\begin{bmatrix} \Delta T_{uv} \\ \Delta T_{vw} \\ \Delta T_{wu} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \\ -1 & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \Delta T_{\alpha} \\ \Delta T_{\beta} \end{bmatrix} \quad (24)$$

Figs.8-10 show patterns of pulse output method. Each line voltage pulse is classified by combination of positive and negative pulses. There are three patterns, which are $\Delta T_{uv} > 0$ and $\Delta T_{vw} < 0$, $\Delta T_{vw} > 0$ and $\Delta T_{wu} < 0$, $\Delta T_{wu} > 0$ and $\Delta T_{uv} < 0$. Output of phase voltage is realized by the triangular PWM.

3. Simulation Results

Simulation is performed in Fig.1. Circuit parameters of the simulation and parameters of gain are shown in Table 1 and Table 2. Simulation results in steady state are shown in Figs.11-18.

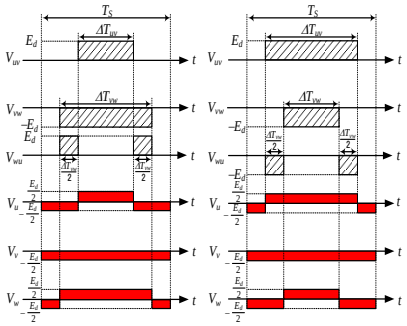

Fig. 8. Principle of pulse conversion ($\Delta T_{uv} > 0$ and $\Delta T_{vw} < 0$)

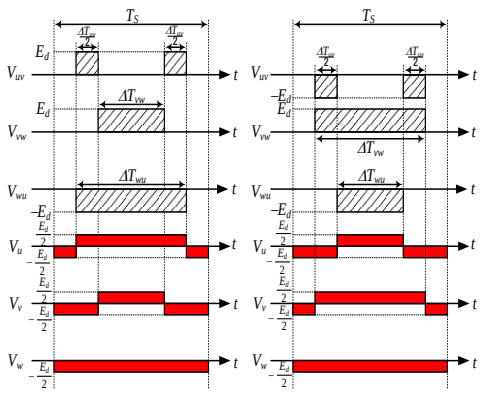

Fig. 9. Principle of pulse conversion ($\Delta T_{vw} > 0$ and $\Delta T_{wu} < 0$)

Figs.11-14 show the results of the general PI control. Figs.15-18 show the results of the proposed method. The proposed control compared with the general PI control, improvement of power factor and compensation of voltage drop can be performed properly by the UPFC operation. Result of the comparison, the DB control has a superior compensation performance than the PI control. In particular, the voltage control of the series side is much improved by the proposed control in Fig.18. In steady state, the DB control is able to follow to the current and the voltage reference quickly and accurately, and it has less time delay than the PI control.

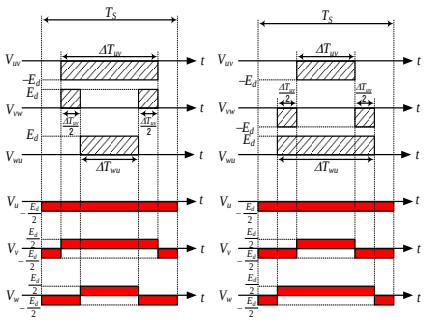

Fig. 10. Principle of pulse conversion ($\Delta T_{wu} > 0$ and $\Delta T_{uv} < 0$)

Figs.19-22 show transient responses of the output current in the parallel side and the output voltage in the series side. In the transient response, the load increases to double at 0.3s. In the transient response, the PI control takes around 3 cycles to converge. However, the DB control is able to follow quickly for variations in load. In comparison of the transient response, the performance of the proposed control has conspicuous advantage.

Table 1. Parameters of circuit

L_S : 0.4 (mH)	R_S : 0.1 (Ω)
L_d : 8.0 (mH)	R_d : 4.0 (Ω)
L_1 : 1.5 (mH)	L_2 : 2.0 (mH)
C_1 : 5.0 (μF)	R_c : 2.0 (Ω)
L_3 : 4.0 (mH)	C_2 : 50.0 (μF)
E_d^* : 200 (V)	V_S : 100 (V)

Table 2. Parameters of control gain

l_1 : –1.0	l_2 : 0.47
l_3 : –1.0	l_2 : –0.50

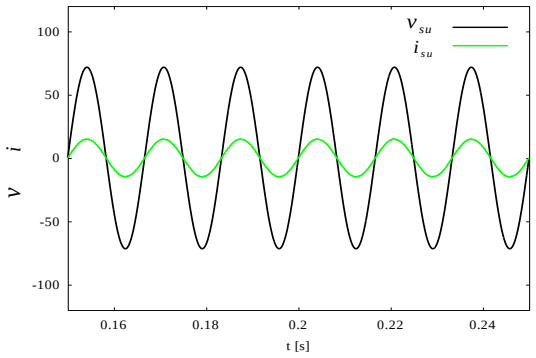

Fig. 11. Line voltage v_{su} and line current i_{su}(by PI control)

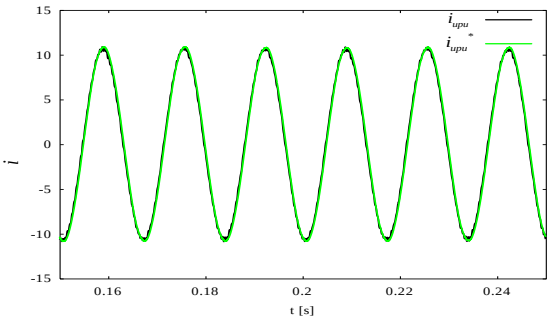

Fig. 12. The output current i_{up} and reference i_{up}^* in the parallel side (by PI control)

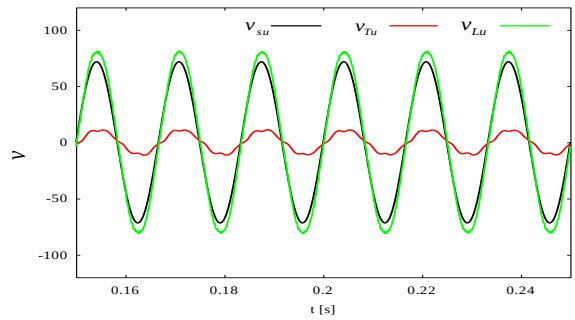

Fig. 13. The voltage drop compensation(by PI control)

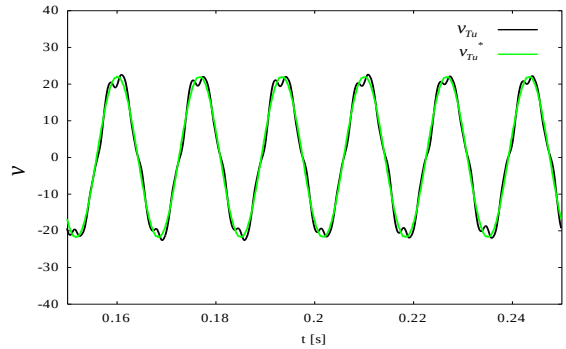

Fig. 14. The primary output voltage v_t and reference v_t^* in the series side (by PI control)

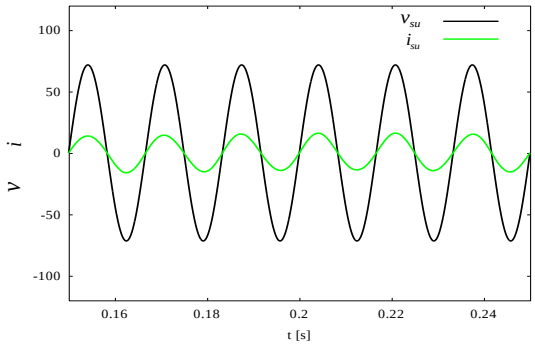

Fig. 15. Line voltage v_{su} and line current i_{su}(by DB control)

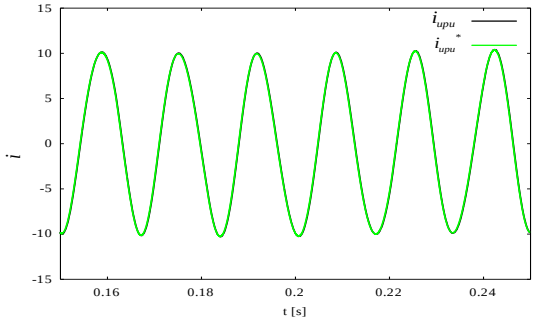

Fig. 16. The output current i_{up} and reference i_{up}^* in the parallel side (by DB control)

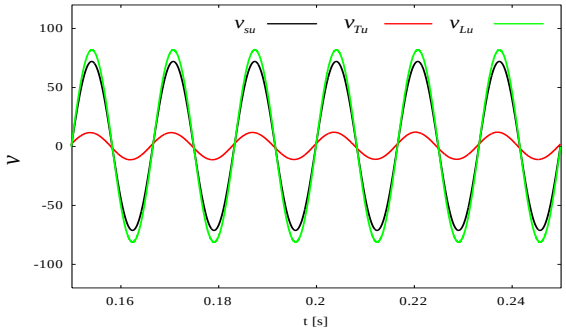

Fig. 17. The voltage drop compensation(by DB control)

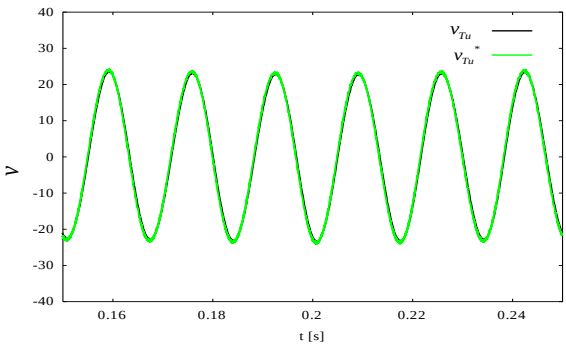

Fig. 18. The primary output voltage v_t and reference v_t^* in the series side (by DB control)

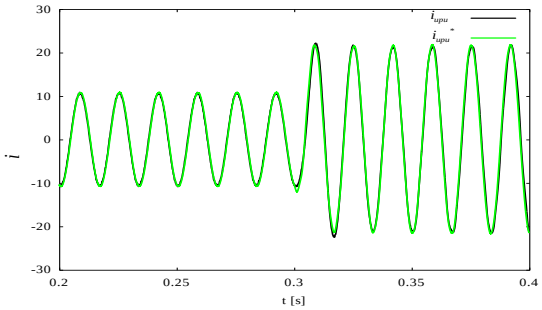

Fig. 19. The transient response of the output current in the parallel side (by PI control)

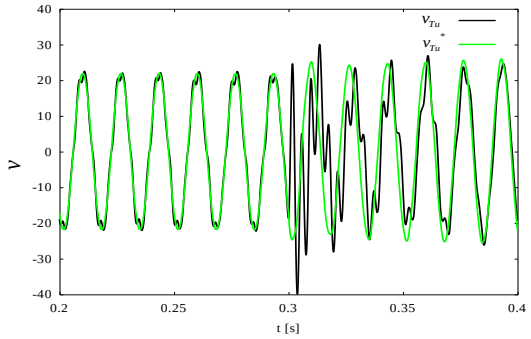

Fig. 20. The transient response of the output voltage in the series side (by PI control)

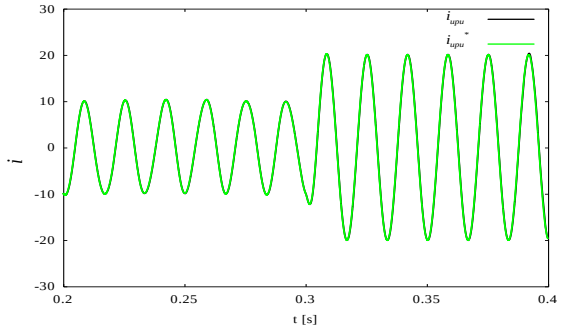

Fig. 21. The transient response of the output current in the parallel side (by DB control)

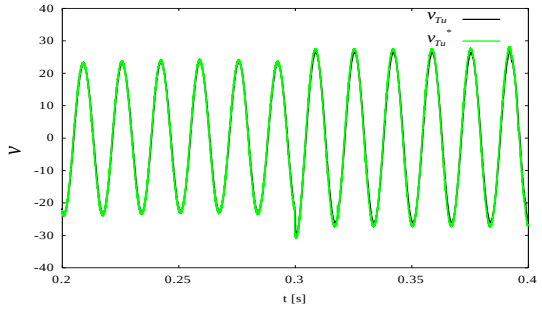

Fig. 22. The transient response of the output voltage in the series side (by DB control)

4. Conclusion

In this study, the DB control is proposed in order to improve performance of the UPFC and the effectiveness of the DB control is verified by comparison with the PI control. The DB control is able to realize a quick and accurate response of the current and voltage control for only a sampling period compared with the general PI control.

The simulation shows that the power quality is improved by performing the reactive power compensation and the voltage drop compensation of the UPFC. It is clarified that excellent results are obtained by the proposed DB control, which is able to operate quickly and accurately in steady state and transient response.

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