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A New Switching Pattern for Multilevel Inverter Based on Selective Harmonic Elimination Using Genetic Algorithm

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Abstract – In this paper, a new switching pattern is presented for multilevel inverters. With changing off-angel of each switch, the on time interval of all switches will approximately be equal and then the lifetime of inverter will increase, also using this method can reduce electrical stress on switches in higher levels of inverter. Switching angels as for desired modulation index are calculated using genetic algorithm whereas selective harmonics are controlled within the allowable range. The computed angels are simulated in Matlab/Simulink for respective circuits to validate the results.

Keywords: **Multilevel Inverter, Harmonic Elimination, THD, Genetic Algorithm**

1. Introduction

The main concepts of multilevel inverters, introduced about 3 decades ago [1-2], entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, higher voltage capability, eliminating the harmonics from the output voltage, and minimizing the THD [3]. Several topologies for multilevel inverter have been proposed over these years, the most popular ones are the diode-clamped [4-5], flying capacitor [6-7] and the cascaded H-bridge [8-11] structures. Theoretically, multilevel inverters can synthesize an infinite output-voltage level. By increasing the number of levels in the inverter, the output voltage has more step generation, a staircase waveform, which has a reduced harmonic distortion [12]. However, a large number of levels increase the number of switching devices, diodes, and other passive elements. Cascade H-Bridge multilevel inverter is common structure used in construction of multilevel inverter. In this structure several H-bridge single phase inverter is connected series and provide the desired voltage level. One of the essential problems in these inverters is failing of switches during inverter's operation time which leads to a failure in a whole inverter. This failure is due to two reasons: One or more switches in bridges providing lower levels of voltage are defective due to longer operation time rather than other switches, these switches are in bridges providing lower levels of voltage,. Also some switches are defective because of working on higher switching frequency rather than other switches, these switches are in bridges providing higher levels of voltage,. Also switching loss at the second group switches is higher than other switches, it reduces the efficiency of the circuit.

In this work to overcome these problems a new switching method is proposed. In this method on time of all switches in all bridges of Multilevel inverter is approximately equal. This method is quite similar to common multilevel inverter however there is the difference in each switch's off-angle.

There have been many attempts at finding an optimal switching sequence for both voltage, and current. The most common method is either pulse width modulation (PWM) or space vector modulation (SVM). While attempts at PWM and SVM have success, it is hard to claim that any have found the absolute best switching sequence solution [13-15].

This problem leads to non-linear equations and direct solution of non-linear equations can lead to discontinuity at certain modulation indices. The prevalent methods to solve this problem utilize intelligent methods. In this paper GA is used to solve this problem. The optimal switching angles are generated, selective harmonic are eliminated and consequently THD of output voltage is minimized. To validate the results, the computed switching angles are used in simulated circuit [12].

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2. Structure of the Cascade Multilevel Inverter

Generally, conventional multilevel inverters include an array of switching devices and voltage sources generating voltages with stepped waveform in the output. A cascade multilevel inverter consists of several single-phase full bridge inverters connected in series (Figure 1). In this structure the switch which turns on at first firing angle (α_1) turns off at π-α_1, and its on time is π-$2\alpha_1$ and this inverter provides the first level of multilevel inverter. Whereas the switch which turns on at last firing angle (α_n) turns off at π-α_n, and it's on time is π-$2\alpha_n$ and this inverter provides the last level of multilevel inverter (Figure 2). As shown in Figure 2 inverter's switches of the first level provider are on a time longer than others, also inverter's switches of the last level provider have higher switching frequency than others. These cases lead to the following problems: due to usage time longer than other switches, inverter's switches of the first level provider become ruined earlier. Also due to working on frequency higher than other switches, inverter's switches of high level provider become ruined earlier. This matter is evident at the higher level multilevel inverters.

To overcome this problem a new switching pattern is suggested. At the angles smaller than $\pi/2$, turn on angles, the switches turn on like conventional multilevel inverter, but at the turn off angles, the switches that turn on at α_1 angle, turn off at π-α_n and this sequence continues until the switches turning on at α_n angle, turn off at π-α_1 (Figure 3). As shown in Figure 3 all switches of inverter have approximately equal on time and this case causes the lifetime of inverter to increase. Also this matter reduces the electrical stress on switches providing high level voltage. Due to reduction in the switching frequency on these switches, the switching loss decreases. This matter leads to increase in the efficiency of the inverter.

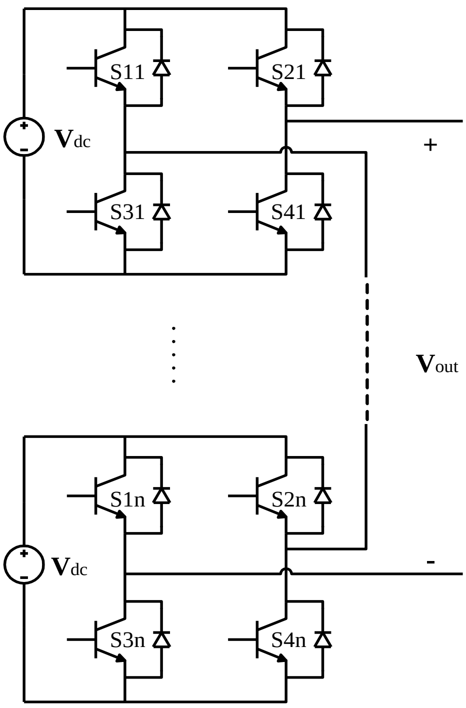

Fig. 1. Single phase structure of cascaded multilevel inverter

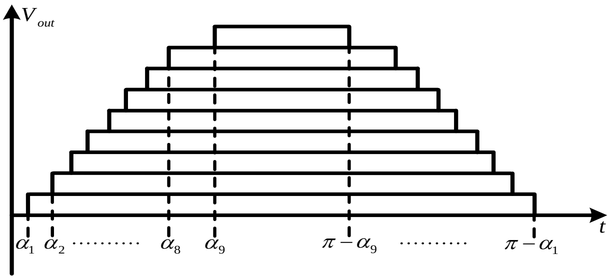

Fig. 2. Output voltage of each cell in conventional SHE switching pattern multilevel inverter

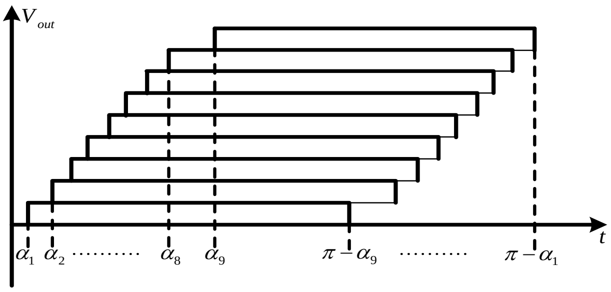

Fig. 3. Output voltage of each cell in proposed SHE switching pattern in cascaded multilevel inverter

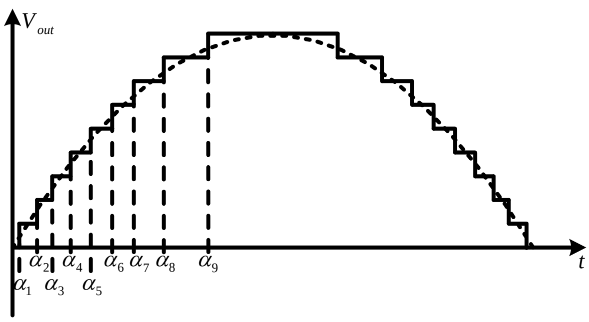

Fig. 4. Output voltage waveform of a 19-level multilevel inverter in SHE

level shown in Fig. 3. This waveform is similar to output voltage waveform of conventional switched inverter (Figure 2). But to prove this matter, the calculation of the Fourier series for proposed switching pattern output voltage is presented in the next section.

Fig. 4 shows the output voltage waveform of proposed switching pattern that is achieved by sum of each voltage.

3. Problem Formulation

Fig. 3shows output voltage waveform of proposed switching pattern multilevel inverter (*V*(*t*)) that can be expressed in Fourier series as:

$$V(t)=\sum_{n=1}^{\infty} a_n \sin(n\alpha_n) + b_n \cos(n\alpha_n) \tag{1}$$

Considering to Figure 2 and (1), the Fourier series of the first level of output voltage is:

$$\begin{aligned} a_{01} &= 0 \\ a_{n1} &= \begin{cases} 0 & n \ is\ even \\ \dfrac{2V_{dc}}{n\pi}\left(\cos n\alpha_m + \cos n\alpha_1\right) & n \ is\ odd \end{cases} \\ b_{n1} &= \begin{cases} 0 & n \ is\ even \\ \dfrac{2V_{dc}}{n\pi}\left(\sin n\alpha_m - \sin n\alpha_1\right) & n \ is\ odd \end{cases} \end{aligned} \tag{2}$$

for second level is:

$$\begin{aligned} a_{02} &= 0 \\ a_{n2} &= \begin{cases} 0 & n \ is\ even \\ \dfrac{2V_{dc}}{n\pi}\left(\cos n\alpha_{m-1} + \cos n\alpha_2\right) & n \ is\ odd \end{cases} \\ b_{n2} &= \begin{cases} 0 & n \ is\ even \\ \dfrac{2V_{dc}}{n\pi}\left(\sin n\alpha_{m-1} - \sin n\alpha_2\right) & n \ is\ odd \end{cases} \end{aligned} \tag{3}$$

and for m[th] level is:

$$\begin{aligned} a_{0m} &= 0 \\ a_{nm} &= \begin{cases} 0 & n \ is\ even \\ \dfrac{2V_{dc}}{n\pi}\left(\cos n\alpha_1 + \cos n\alpha_m\right) & n \ is\ odd \end{cases} \\ b_{nm} &= \begin{cases} 0 & n \ is\ even \\ \dfrac{2V_{dc}}{n\pi}\left(\sin n\alpha_1 - \sin n\alpha_m\right) & n \ is\ odd \end{cases} \end{aligned} \tag{4}$$

The sum of Fourier coefficients obtained for each level resulted to the Fourier coefficient of the output voltage.

$$\begin{aligned} a_0 &= 0 \\ a_n &= a_{n1} + a_{n2} + \cdots + a_{nm} \\ &= \frac{4V_{dc}}{n\pi}\sum_{k=1}^{m}\cos(n\alpha_k) \quad n\, is\, odd \\ b_n &= b_{n1} + b_{n2} + \cdots + b_{nm} = 0 \end{aligned} \tag{5}$$

and

$$0 < \alpha_1 < \alpha_2 < ..\alpha_m < \pi/2 \tag{6}$$

that (5) is same with the furrier series for conventional switching pattern used multilevel inverter[12].

Also the methods used to conventional switched inverter can also be used for proposed switched inverter.

For any harmonics, (5) can be expressed up to the k[th] term, where *m* is the number of variables corresponding to switching angles α_1 through α_m of the first quadrant. In selective harmonic elimination, a_n is assigned as the desired value for fundamental component and equals to zero for the harmonics to be eliminated [16].

$$\begin{aligned} a_1 &= (4V_{dc}/\pi)\sum_{k=1}^{m}\cos\alpha_k = M \\ a_5 &= (4V_{dc}/5\pi)\sum_{k=1}^{m}\cos 5\alpha_k = 0 \\ a_n &= (4V_{dc}/n\pi)\sum_{k=1}^{m}\cos(n\alpha_k) = 0 \end{aligned} \tag{7}$$

where *M* is the amplitude of the fundamental component[12].

Solving these equations is tending to compute the $\alpha_1, \ldots, \alpha_k$. Whereas triples harmonics are eliminated in a three phase balanced system, computing these harmonics are neglected in the computing of switching angle. It is evident that with computed *m* switching angles, (*m*-1) harmonics can be eliminated. These lead to non-linear equations and direct solution of non-linear equations can lead to discontinuity at certain modulation indices. These non-linear equations show multiple solutions and the main difficulty is solution's convergence at certain points, while no analytical solution is available [16-18].

In this work the complexity of solving the non-linear equations is prevented by converting the selective harmonic elimination problem to an optimization problem as follow:

The %THD of the output voltage can be expressed by:

Voltage THD is considered as the fitness function $F(\alpha)$, that must be minimized with the constraints of the selective

$$\%THD = \left[\frac{1}{a_1^2} \sum_{n=5}^{\infty} (a_n)^2 \right]^{1/2} \times 100 \qquad (8)$$

where $n=6i \pm 1$ ($i=1, 2, 3, \ldots$).

harmonic elimination to reduce the overall THD in the output voltage waveform. Mathematically, the problem can be formulated as follows:

$$\begin{aligned} &Minimize\, F(\alpha) = F(\alpha_1, \alpha_2, \ldots, \alpha_m) \\ &Subject\ to: 0 < \alpha_1 < \alpha_2 < ..\alpha_m < (\pi/2); \\ &a_1 = M; \\ &a_5 < \varepsilon_1; \\ &a_7 < \varepsilon_2; \\ &. \\ &. \\ &a_n < \varepsilon_m; \end{aligned} \qquad (9)$$

where ε_1, ε_2,…, ε_m are the allowable limits of individual harmonics.

The values of ε_1, ε_2,…, ε_m are chosen very close to zero for the selected low-order harmonics to be eliminated completely. In the proposed method based on GA, at the modulation indices of discontinuity for the computation of switching angles α_1 through α_n, the angles are computed based on minimum possible voltage THD and optimizing individual harmonics. With this formulation the selected harmonics are not completely removed but they remain within allowable limits, instead the above mentioned problems can be solved.

4. Genetic Algorithm Method

GA is a search mechanism imitates the natural selection and the genetics of living organisms. A typical GA consists of three operators, i.e., reproduction, crossover, and mutation [19-20]. A flowchart of the GA algorithm is shown in Fig. 5.

The process of a GA usually begins with a randomly selected population of chromosomes. These chromosomes are representations of the problem to be solved, in this case switching angles of inverters. Then to start the search procedure, the switching angles are randomly generated. These values must be satisfied the conditions of (9) for the chosen number of population. According to the attributes of the problem, different positions of each chromosome are encoded as bits, characters, or numbers. These positions are sometimes referred to as genes and are changed randomly within a range during evolution. An evaluation function ($F(\alpha)$) is used to calculate the "goodness" of each chromosome.

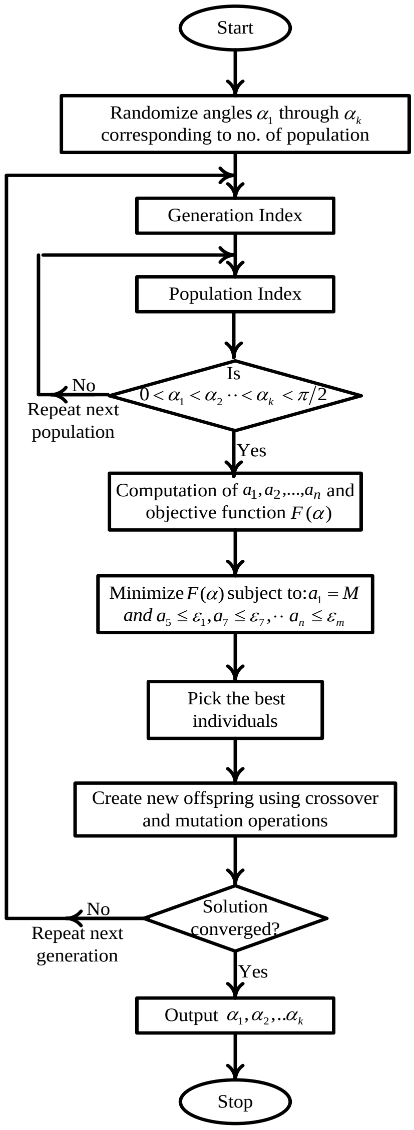

Fig. 3. Flowchart of the genetic algorithm

In the optimization problem considered, the $F(\alpha)$ is defined as voltage THD which presented in (8). During evaluation, two basic operators, crossover and mutation, are used to simulate the natural reproduction and mutation of species. In crossover, randomly selected subsections of two individual chromosomes are swapped to produce the offspring. In mutation, randomly selected genes in chromosomes are altered by a probability equal to the specified mutation rate. These operators are applied to offspring to generate next generations during optimization process. When the convergence is achieved, the repeat of this process is stopped. With a considerable number of generations and large number of population in each generation, the algorithm searches for all probable set of solutions and finally compute the angles α_1 through α_n, to contribute the minimum THD, keeping the individual harmonics within the limits as specified by (9)[12].

The program is run for different values of modulation index and the switching angles corresponding to minimum voltage THD are stored as a look-up table.

5. Simulation Results

The calculated switching angles are simulated through simulation of cascaded multilevel inverter using the software package Matlab/Simulink. The results are presented in this section. The simulation results of the

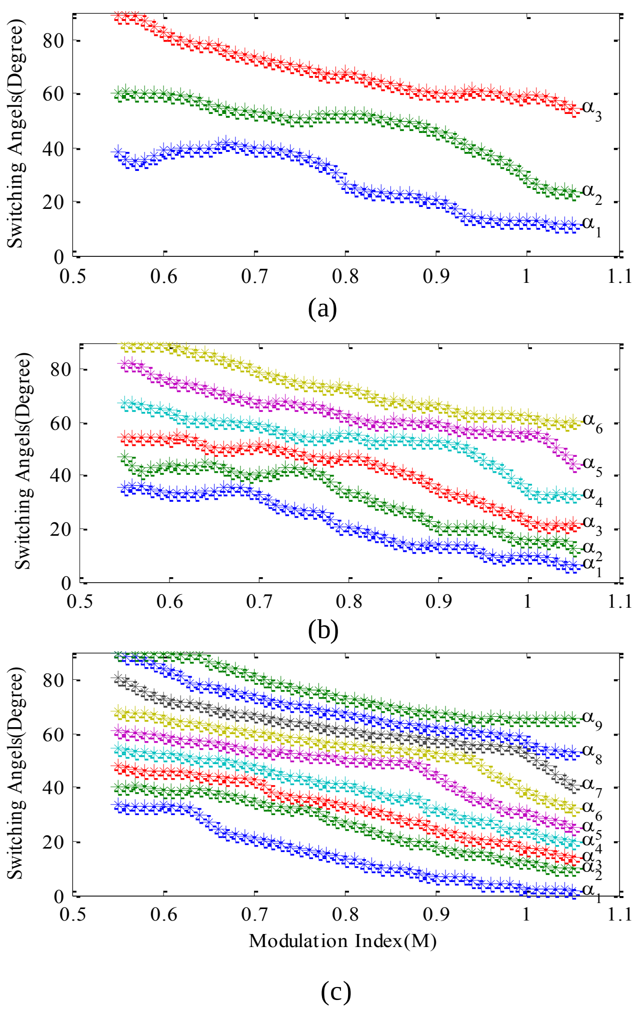

Fig. 4. Switching angles against modulation index for (a) 7, (b) 13 and(c) 19 level multilevel inverter

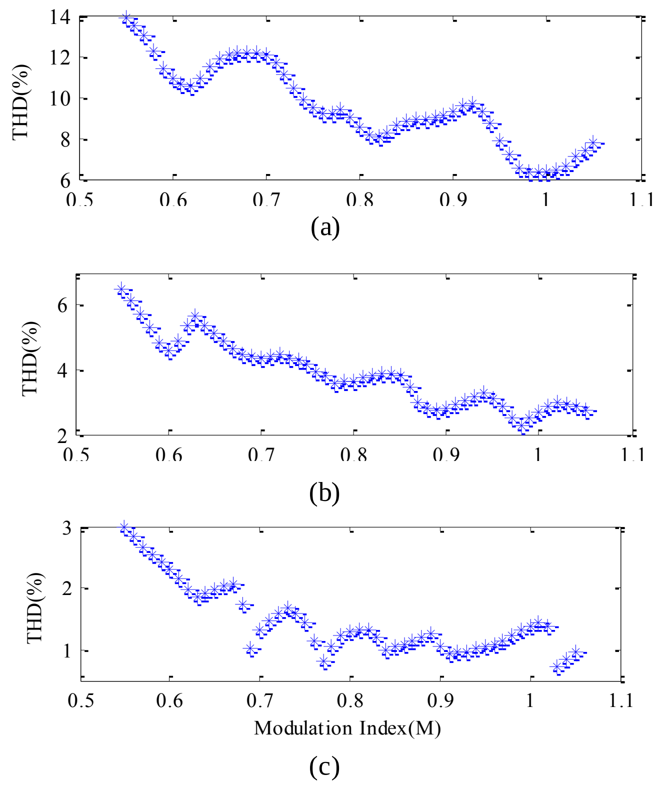

Fig. 5. Minimum THD against Modulation Index for a) 7, b) 13 and c) 19 level multilevel inverter

switching pattern with varying modulation index (*M*) considering 3 multilevel inverters (7, 13 and 19 level) is shown in Fig. 6. As can be seen from this Figure the algorithm has found solution for all modulation indices include discontinuity points.

Voltage THD (%) against modulation index related to the optimal switching angles which come from GA is shown in Fig. 7. As shown in Fig. 7, with increase the level of inverter, voltage THD is reducing. This improved quality of voltage and power of multilevel inverter.

The output phase voltage waveform of the inverter's at *M*=0.9 is shown in Fig. 8. In each inverter the dc sources (V_{dc}) are same and are selected so that the effective value of the output voltage is equal to 100v. The load is connected to inverter is inductive and R=1Ω and L=5mH.

Fig. 9 shows the output voltage waveform of each cell of multilevel inverter, which is similar to Figure 3. In other words, first level switches turn on at α_1 and turn off at π-α_n angle. Other switches also act likewise.

Figure 10 shows the current waveform of a three phase delta connected load. The waveform of the current is found to be almost sinusoidal.

As shown in Fig. 8 and 10, the output voltage and current of this type inverter is same with the output voltage and current of conventional inverters [12].

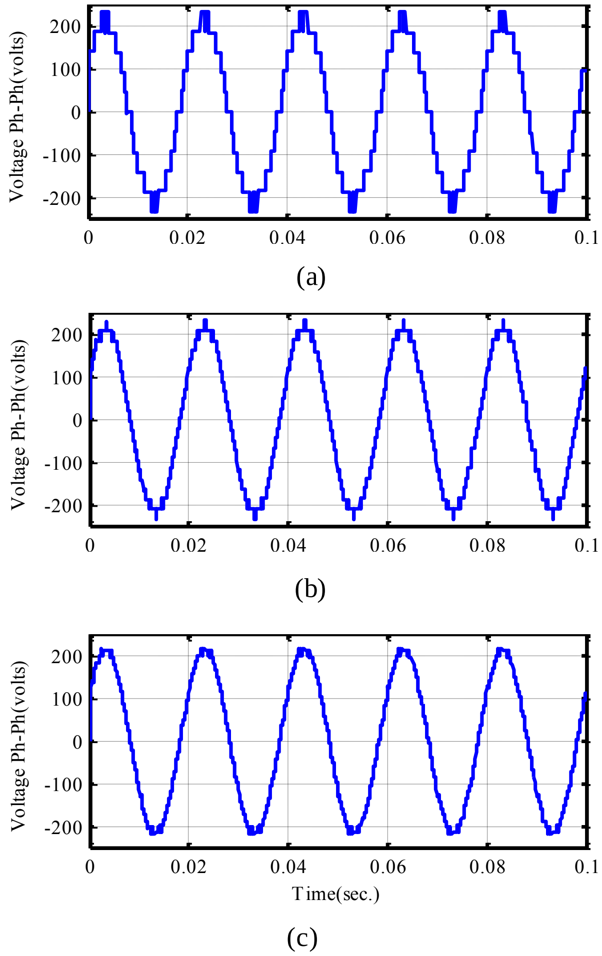

Fig. 6. Output voltage waveform for(a) 7, (b) 13 and (c) 19 level multilevel inverter at M=0.9

5. Conclusion

In this paper a new switching method is presented for multilevel inverters. With using this method switching the on time interval of all switches in the multilevel inverters will approximately be equal and therefore the lifetime of inverter will increase. Also a GA algorithm was applied to eliminate selected order of harmonics and to reduce output voltage THD. Besides controlling individual selected harmonics within the allowable limits, the method also optimizes the other order of harmonics to minimize the overall voltage THD. Moreover, at the points of discontinuity of solutions, the algorithm computes the lowest possible voltage THD through optimization of the objective function and finds solutions for all desired modulation indices. The effectiveness of applied method has been verified through simulation and the results were presented. The results show that the proposed method effectively minimizes a large number of specific harmonics, and the output voltage results in very low THD. Also the waveform of the current is found to be almost sinusoidal.

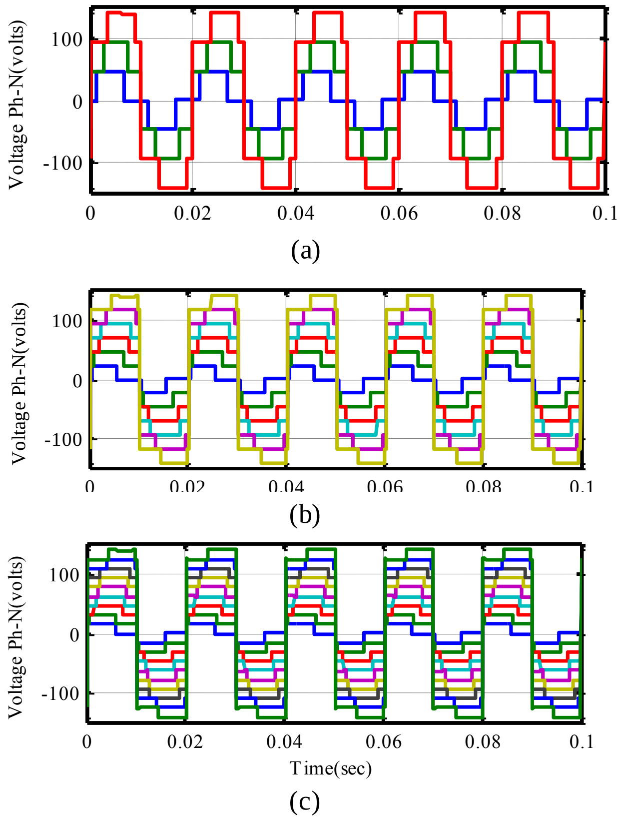

Fig. 7. Output voltage of each cell of multilevel inverter

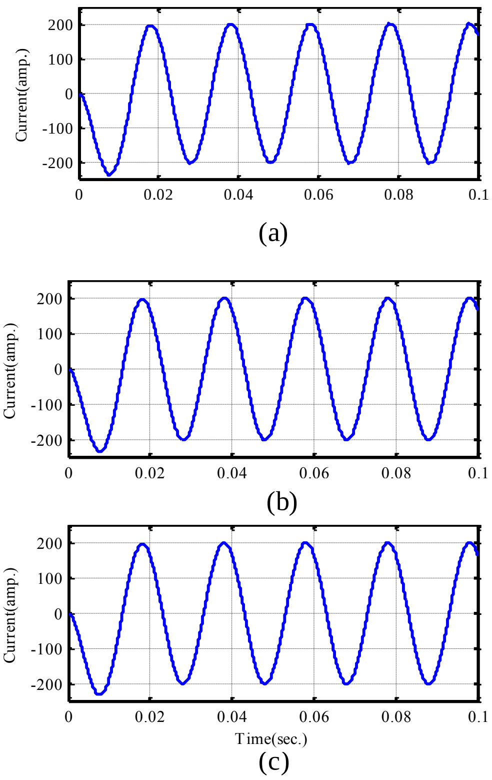

Fig. 8. Current waveform for(a) 7, (b) 13 and(c) 19 level multilevel inverter at M=0.9

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