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A Novel Extended Topology for Cascade Multilevel Voltage Source Converter for High-Power Applications with Interesting Advantages

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Abstract – In this paper, a novel topology for cascade multilevel converter is introduced, which has many levels with fewer number of power electronic components. Less number of the switches leads to the reduction of size, losses, simple control strategy and high efficiency. For proposed multilevel converter, a new algorithm for determination of dc voltage source values has been recommended. The performance and operation of the proposed multilevel converter has been evaluated with the simulation results of a cascade 25-level converter.

Keywords: **Multilevel Converter, Bidirectional Switch, High-Power Applications, Full-Bridge Converter.**

1.Introduction

Multilevel converter has been widely introduced for high-power applications in recent years [1]. A multilevel converter is a power electronic device built to synthesize a desired ac output voltage from several levels of dc voltage sources [2]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3], utility interface for renewable energy systems [4], flexible AC transmission system (FACTS) and traction drive systems [5], [6]. Many types of structures of multilevel converters have been introduced. Multilevel converters can be classified into three kind's structures:

- Diode clamped [7].
- Flying capacitor [8].
- Cascade converter with separated dc sources [9].

Conventional H-bridge cascade converter is one of the most important structures in the family of multilevel converters, because this structure needs the least number of power electronic components when compared to flying capacitor and diode clamped converter [10]. A cascaded multilevel converter has a number of H-bridge converter cells with separate dc sources for each cell and it is connected in series. In symmetrical cascaded multilevel converter, the values of DC sources of similar cells are the same. For the same number of components, asymmetrical cascade multilevel structures significantly increase the number of output voltage levels. In these topologies, DC voltage sources of different cells are non-equal [11]. However, this structure needs to a large number of unidirectional switches and dc sources. The most important Part in multilevel converters is switches which increase the cost and control complexity and tend to reduce the overall reliability and efficiency.

Recently, several multilevel converter structures have been improved to reduce the number of switches in [12-15]. But, this multilevel converter needs a large number of power electronic components for producing all levels at the output.

In this Paper, a new topology for cascade multilevel converter has been investigated to increase the number of output voltage levels with minimum number of power electronic components.

1. Proposed Cascade Topology

Fig. 1 shows the proposed topology for a sub-multilevel converter which consists of the basic unit and a full bridge converter. The basic unit consists of n bidirectional switches and (n+1) capacitors. There are several structures

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for bidirectional switches. In this paper, the proper structure of bidirectional switches (S1, S2,…, Sn) which is shown in Fig. 1, arranged by a common emitter combination of two switches which each switch has one IGBT and an anti-parallel diode. This arrangement needs only one gate driver

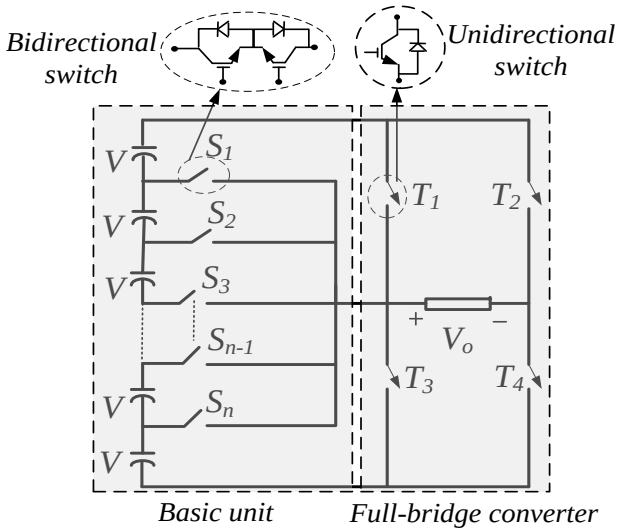

Fig. 1. Proposed sub-multilevel converter.

circuit. The full-bridge converter has four unidirectional switches.

Table 1 gives the values of voltages V_O for different states of the switches S_1, S_2,..., S_n, T_1 … and T_4 in proposed sub-multilevel converter. It is noticeable that there are several switching states for generating the zero voltage level and in the table 1; only one of them is introduced.

Table 1. Values of V_O for Different States of the Switches.

state	*Switches states*									*Output voltage*
	S_1	S_2	……	S_{n-1}	S_n	T_1	T_2	T_3	T_4	
1	0	0	……	0	0	1	1	0	0	0
2	0	0	……	0	1	0	0	0	1	*V*
3	1	0	……	0	0	0	1	0	0	*-V*
4	0	0	……	1	0	0	0	0	1	*2V*
5	0	1	……	0	0	0	1	0	0	*-2V*
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(2n+2)	0	0	……	0	0	1	0	0	1	*(n+1)V*
(2n+3)	0	0	……	0	0	0	1	1	0	*-(n+1)V*

In the proposed sub-multilevel converter, the values of capacitor voltages are equal. Therefore, this converter is called symmetrical sub-multilevel converter. In this structure, the number of levels can be calculated as follows:

$$N_{level} = 2n + 3 \tag{1}$$

In addition, the total numbers of IGBTs (N_{IGBTs}) and gate drivers (N_{driver}) are given by (2) and (3), respectively:

$$N_{IGBTs} = 2n + 4 \tag{2}$$

$$N_{driver} = n + 4 \tag{3}$$

Where n represents the number of bidirectional switches in the basic unit. In the recommended sub-multilevel converter, the maximum output voltage $(V_{o\max})$ is:

$$V_{o\max} = (n+1) \times V \tag{4}$$

To generate a large number of output voltage levels with minimum number of IGBTs, cascade multilevel converters can be utilized. Fig. 2 shows the new proposed configuration for cascade multilevel converter. The overall output voltage of the proposed cascaded multilevel converter is the sum of output voltages of the sub-multilevel converters as follows:

$$V_o = V_{o1} + V_{o2} + ... + V_{ok} \tag{5}$$

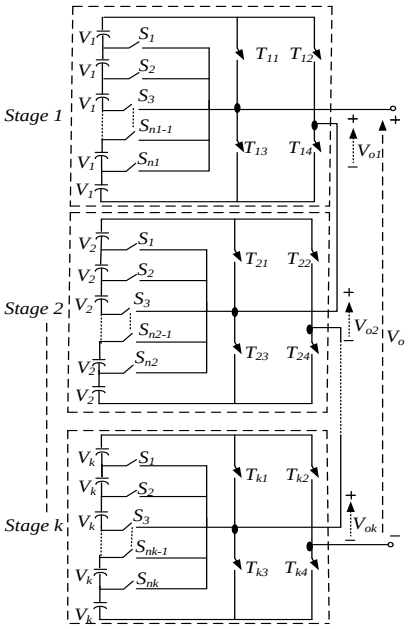

Fig. 2. Proposed topology for cascaded multilevel converter.

The magnitude of dc sources must be selected based on the following algorithm:

Stage 1:

$$V_1 = V \tag{6}$$

In this stage, the maximum value of output voltage $\left(Vo_{1,\max}\right)$ is obtained as follows:

$$Vo_{1,\max} = (n_1 + 1) \times V \tag{7}$$

Stage 2:

$$V_2 = V + (2 \times Vo_{1,\max}) = \left[(2n_1 + 3)\right] \times V \tag{8}$$

Therefore, the maximum magnitude of output voltage for this stage can be obtained by (9):

$$Vo_{2,\max} = (n_2 + 1) \times V_2 \tag{9}$$

Stage 3:

$$\begin{aligned} V_2 &= V + (2 \times Vo_{1,\max}) + (2 \times Vo_{2,\max}) \\ &= \left[(2n_1 + 3) \times (2n_2 + 3)\right] \times V \end{aligned} \tag{10}$$

For the kth stage:

$$\begin{aligned} V_k &= \left[(2n_1 + 3) \times (2n_2 + 3) \times \ldots \times (2n_{k-1} + 3)\right] \times V \\ &= \prod_{i=1}^{k-1} \left(2n_i + 3\right) \end{aligned} \tag{11}$$

Hence, considering equations (6-11), the total numbers of levels can be obtained by using equation (12):

$$\begin{aligned} V_k &= (2n_1 + 3) \times (2n_2 + 3) \times \ldots \times (2n_k + 3) \\ &= \prod_{i=1}^{k} \left(2n_i + 3\right) \end{aligned} \tag{12}$$

In this algorithm, the values of dc sources in different stages are non-equal. Consequently, this structure is called asymmetric cascade converter. In the recommended structure, the number of IGBTs is given by (13):

$$N_{IGBT} = 2(n_1 + n_2 + \ldots + n_k) + 4k \tag{13}$$

In addition, the peak value of output voltage is calculated using the following equation:

$$Vo_{\max} = \sum_{i=1}^{k} (n_i + 1) \times V_i \tag{14}$$

3. Design of Multilevel Converter Based on the Prop osed Topology

In this section, the problem is to design a typical 800-V multilevel converter with a minimum of 340 output voltage levels based on the suggested topology and those presented in [12-15]. It is evident that more output voltage levels with minimum number of component will provide a better design. Fig. 3 shows a sample of the proposed topology. In this design, the magnitudes of dc sources are determined by the suggested method. As shown in this figure, the number of IGBTs, capacitors and gate driver circuits are 24, 8 and 20, respectively. In this figure, the number of output voltage levels is 625.

The topology of optimal multilevel converter with minimum used IGBTs based on the suggested topology of [12-13] is presented in Fig. 4(a). The number of IGBTs, capacitors, gate driver circuits are 36, 6 and 18, respectively, and the number of levels is 343.

The optimal multilevel structure with minimum used IGBTs based on the recommended in [14] is shown in Fig. 4(b). The number of IGBTs, capacitors and gate driver circuits are 34, 10 and 19 respectively. Also, the number of output voltage levels is 485.

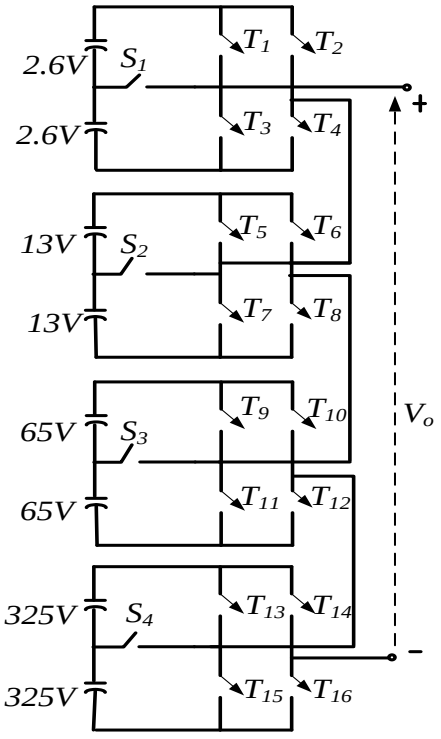

Fig. 3. A sample for proposed cascade structure.

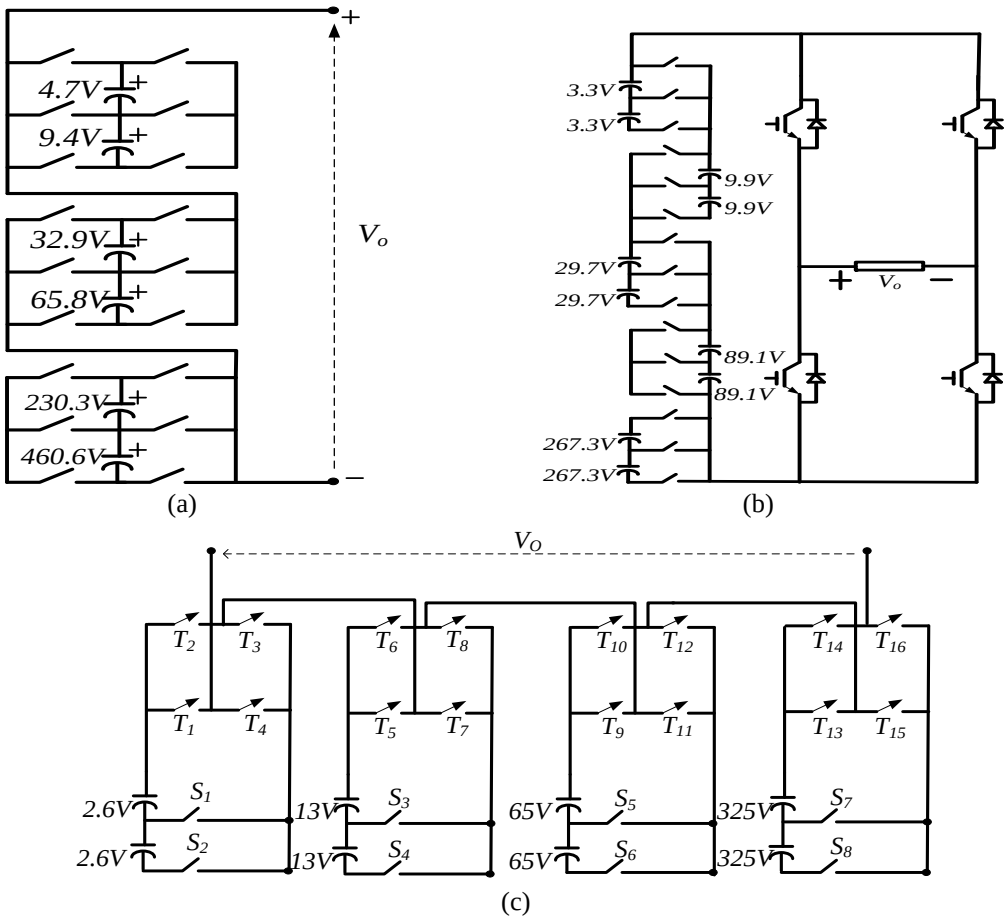

Fig. 4. Optimal multilevel structure considering the minimum used Switches presented topologies in. (a) (b) (c) [12-15]

The optimal structure with minimum number of IGBTs based on recommended topology in [15] is shown in Fig. 4(c). This topology needs 32 IGBTs, 24 gate driver circuits and 8 capacitors. In this converter, the number of voltage levels is 625.

The comparison of power electronic components in the proposed topology and other topologies shows that the presented topology requires minimum number of power electronic components.

4. Simulation results

To study the operation of the proposed multilevel converter in the generation of different voltage waveforms, a single-phase 25-level cascade multilevel converter is implemented based on the proposed topology shown in Fig. 5. The cascade 25-level converter needs 4 dc voltage sources which have values V1= 25V and V2= 125V. So that, maximum 300V output voltage is obtainable. A test has been made on the R-L load (R = 250Ω and L = 80mH). In order to validate the proposed multilevel converter, computer simulation using MATLAB Software has been used. This topology studied to examine the characteristics of the output voltage and current. The total harmonic distortion (THD) evaluates the quantity of harmonic contents in the output waveform and is a popular performance index for power converters. Several modulation techniques and control strategies have been developed for multilevel converters such as fundamental frequency-switching, sinusoidal PWM, space vector PWM (SV-PWM), selective harmonic elimination (SHE-PWM),

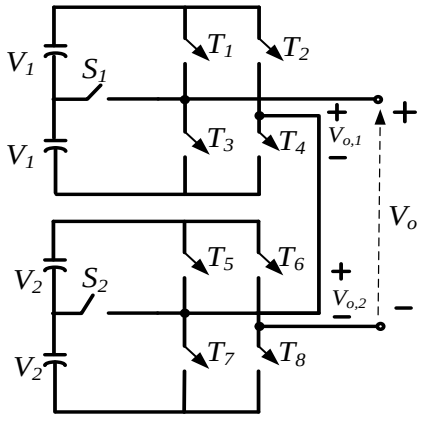

Fig. 5. 25-level cascade converter.

and others [17]-[22]. In this paper, the fundamental frequency-switching method has been utilized. The advantage of the fundamental frequency-switching technique is its low switching frequency compared to other control strategies [23]. It is important to note that the calculation of the optimal switching angles for different objective such as the elimination of selected harmonics and minimizing the total harmonic distortion (THD) is not the objective of this paper. Table 2 shows the magnitude of V_O for different states of switches in proposed 25-level cascade converter. It is important that there are different switching patterns for generating the zero level, and in table 2, only one of them is shown.

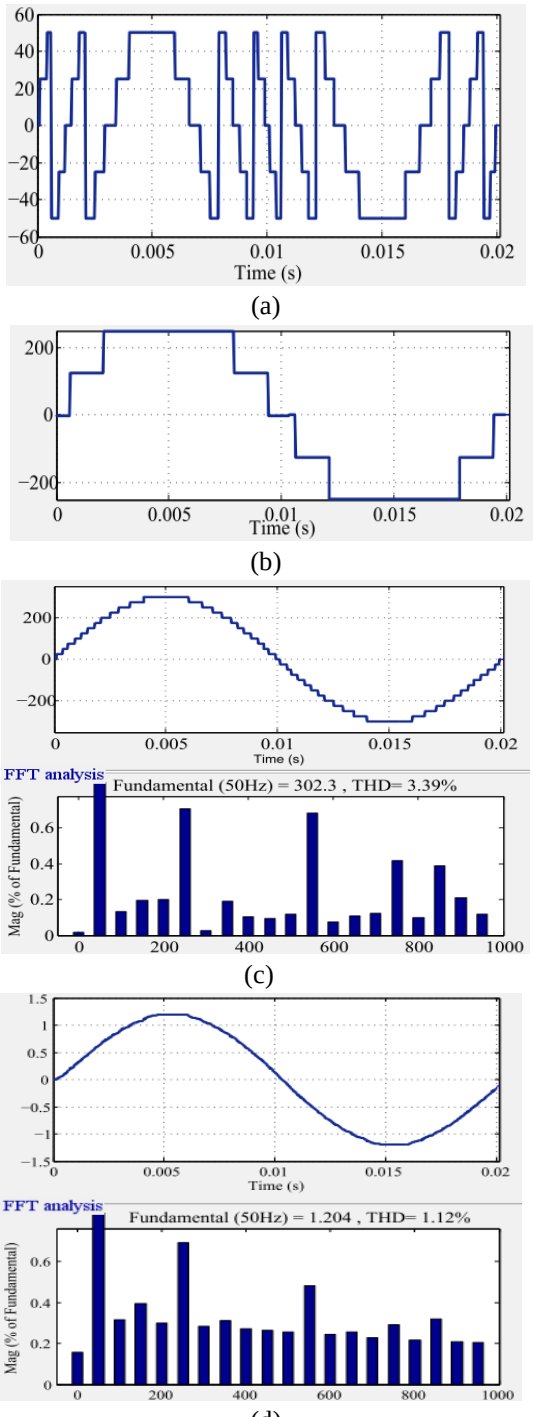

Fig. 6. Simulation results (a) $V_{O,1}$; (b) $V_{O,2}$; (c) Output voltage and harmonic spectrum (THD=3.39%) (d) Output current and harmonic spectrum (THD= 1.12%).

Table. 2. Switches States for 25- level Cascade Topology

State	Switches states										Output voltage (v)
	S_1	S_2	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	
1	0	0	1	0	0	1	1	0	0	1	300
2	1	0	0	0	0	1	1	0	0	1	275
3	0	0	1	1	0	0	1	0	0	1	250
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
12	1	0	0	0	0	1	1	1	0	0	25
13	0	0	1	1	0	0	1	1	0	0	0
14	1	0	0	1	0	0	1	1	0	0	-25
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
23	0	0	1	1	0	0	0	1	1	0	-250
24	1	0	0	1	0	0	0	1	1	0	-275
25	0	0	0	1	1	0	0	1	1	0	-300

Fig. 6 shows simulation and measurement results. For this case, THDs of the output voltage and current based on simulations are 3.39% and 1.12%, respectively. To generate a desired output with high power quality, the number of voltage levels should be increased or other switching technique should be applied to the converter.

5. Conclusion

This paper proposes a new topology for cascade multilevel converter with fewer numbers of components. An algorithm for determination of dc sources values for proposed cascade topology has been suggested. This method generates a large voltage levels without increasing number of power electronic components. Less number of the switches leads to the reduction of size, simple control strategy, and high efficiency. Comparison among the proposed converter with other similar topologies has been provided. It is shown that the proposed topologies, has many levels with fewer components. The performance of the proposed topology has been verified on a single-phase 25-level cascade multilevel converter prototype.

References

[1] M. D. Manjrekar, P. K. Steimer and T. A. Lipo, "Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power

Applications,"*IEEE Trans. Ind. Appl.*, vol.36, pp. 834-841, 2000.

[2] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "Control of Multilevel converter Using Resultant Theory " , *IEEE Trans. On Cont. Sys. Tech.*, vol. 11, no. 3, pp. 345-354, 2003.

[3] M. F. Aiello, P. W. Hammond, and M. Rastogi, "Modular Multi-Level Adjustable Supply with Parallel Connected Active Inputs," *U.S. Patent*, 2001.

[4] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Design of new power electronic converter (PEC) for photovoltaic systems and investigation of switches control technique", *In Proc. 28th Power System Conf. (PSC)*, 2013, pp. 1-8.

[5] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel Inverters for Electric Vehicle Applications," *IEEE Workshop on Power Electronics in Transportation*, pp. 1424-1431, 1998.

[6] M.N.Abdul Kadir, S.Mekhilef and H.W.Ping "Dual vector control strategy for a three –stage hybrid cascaded multilevel inverter," *Journal of power Electronic* ,vol.10, no.2,pp.155-164,2010.

[7] Y. Xiaoming, I. Barbi, "Fundamentals of a new diode clamping multilevel Inverter,"*IEEE Trans. Power Electron*, vol. 15, No. 4 ,pp. 711-8, 2000.

[8] J. Hunag, K. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans Power Electron*, vol. 21, no.1 , pp.140-7, 2006.

[9] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Design of New Single-phase Multilevel Voltage Source Inverter", International Journal of Power Electronics and Drive Systems (IJPEDS), vol. 4, no. 1B, pp. 45-55, 2014.

[10] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, M. Sabahi: 'New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," IET Power Electron., vol. 7, no. 1, pp. 96–104, 2014.

[11] Y.-S. Lai and F. S. Shyu, "Topology for hybrid multilevel inverter", *IEE Proc-Electro. Power Appl.*, vol. 149, no. 6, pp. 449-458, 2002.

[12] M. T. Haque, "Series sub-multilevel voltage source inverters (MLVSIs) as a high quality MLVSI," *in Proc. SPEEDAM*, pp. F1B-1–F1B-4., 2004

[13] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of DC voltage sources and switches in asymmetrical multilevel converters using a novel topology," *J. Elect. Power Syst. Res*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[14] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron*., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[15] J. Ebrahimi, E. Babaei, G. B. Gharehpetian , "A New Multilevel Converter Topology With Reduced Number of Power Electronic Components," *IEEE trans. power electron.*, vol. 59, no. 2,pp.655-667, 2012.

[16] C. Klumpner and F. Blaabjerg, "Using reverse blocking IGBTs in power converters for adjustable speed drives," *IEEE Trans. Ind. Appl*., Vol. 42, No. 3, pp. 807-816, 2006.

[17] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, M. Sabahi, "Novel Topologies for Symmetric, Asymmetric and Cascade Switched-Diode Multilevel Converter with Minimum Number of Power Electronic Components," IEEE Trans. Ind. Electron, vol. 61, no.10, pp. 5300 - 5310, 2014.

[18] R. Shalchi Alishah, D. Nazarpour and S. H. Hosseini, "Design of new multilevel voltage source inverter structure using fundamental frequency-switching strategy", Transaction on electrical and electronic circuits and systems, vol. 1, no. 1, pp. 1-7, Jan. 2013.

[19] M. G. Hosseini Aghdam, S. H. Fathi, G. B. Gharehpetian, "Analysis of Multi-Carrier PWM Methods for Asymmetric Multi-Level Inverter" IEEE Conf. on Ind. Elect. and Appl., pp.2057 - 2062, 2008.

[20] P.T.Josh, J. Jerome, A. Wilson, "The Comparative Analysis of Multi-Carrier Control Techniques for SPWM Controlled Cascaded H-Bridge Multilevel Inverter", *proc. of icetect*, pp. 459-464, 2011.

[21] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, 2006.

[22] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, M. Sabahi: 'Switched-diode structure for multilevel converter with reduced number of power electronic devices," IET Power Electron., vol. 7, no. 3, pp. 648 – 656, 2014.

[23] D. C. Ludois, J. K. Reed, and G. Venkataramanan, "Hierarchical control of bridge-of-bridge multilevel power converters," *IEEE Trans. Ind. Elec.*, vol. 57, no. 8, pp. 2679–2690, 2010.

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