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Reducing Test Power and Improving Test Effectiveness for Logic BIST

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***Abstract*—Excessive power dissipation is one of the major issues in the testing of VLSI systems. Many techniques are proposed for scan test, but there are not so many for logic BIST because of its unmanageable randomness. This paper presents a novel low switching activity BIST scheme that reduces toggle frequency in the majority of scan chain inputs while allowing a small portion of scan chains to receive pseudorandom test data. Reducing toggle frequency in the scan chain inputs can reduce test power but may result in fault coverage loss. Allowing a small portion of scan chains to receive pseudorandom test data can make better uniform distribution of 0 and 1 and improve test effectiveness significantly. When compared with existing methods, experimental results on larger benchmark circuits of ISCAS'89 show that the proposed strategy can not only reduce significantly switching activity in circuits under test but also achieve high fault coverage.**

***Index Terms*—IC testing, BIST, test power, pseudorandom test data, fault coverage**

I. INTRODUCTION

At the present day, the low power design has become an urgent and challengeable issue in the design for high-performance very large scale integration (VLSI). Therefore, many techniques have been developed to decrease the power consumption of new VLSI design. However, most of these approaches are proposed to reduce power consumption during functional operation, while test mode operation has not been a major emphasis of research. However, recent survey shows that the switching activity during test mode operation is often much higher than that during functional operation [1]. Higher peak power dissipation may cause a voltage droop due to inductance. This, in turn, can lead to some good die to fail the test, and thus introduce unnecessary loss of yield. Higher average power dissipation may elevate temperature and current density which could influence the reliability of circuit under test (CUT) and even damage CUT [2]. As VLSI devices grow in size and complexity, it becomes increasingly expensive to test them at high level.

There has been a lot of interest in developing solutions to reduce power consumption during scan based test. These approaches to reduce switching activity in CUT include adding additional logic [3], scan architecture segmentation with gated clocking [4], scan cell redesigning [5], ordering of tests [6], modified test generation methods [7, 8], and post-generation filling of unspecified values in test cubes [9, 10].

Build-In Self-Test (BIST) [11] has been commonly used in VLSI testing since the design-for-test methodology avoids storing pre-computed test data in automatic test equipment and requires little area overhead. In logic BIST, pseudorandom test dada are generated by pseudorandom test generator (PRTG) such as linear feedback shift register (LFSR), ring generator and cellular automata (CA). Test responses are compacted for fault analysis by multiple input shift register (MISR). Due to the low correlation between consecutive test patterns generated by a PRTG, this

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power problem in scan-based BIST seems to be particularly serious. The low switching activity test application for logic BIST has become an important issue.

In recent years, some sophisticated methods are proposed to decrease test power of scan-based BIST, especially for shift power. Technique proposed in [12] uses token scan chain to reduce power consumption during scan testing. However, token scan cells comprised of two flip-flops and other additional logic gates increase hardware overhead extremely. The method presented in [13] uses a modified clock scheme for PRTG and generates pseudorandom test patterns with two LFSRs resulting in shift power reduction, especially in the clock tree feeding the PRTG. The approaches insert extra logic gates to freeze the scan cell outputs during scan shift are proposed in [14, 15]. These extra logics may cause circuit performance degradation. The technique in [16] focuses on the ratio of care bits in a scan chain and reduces shift power by enabling scan chains that are ineffective for detecting new faults during scan shift. To improve this technique, the approach in [17] clusters the scan chains into several groups and achieves more significant shift power reduction by limiting scan shift to a portion of groups with mask logics during scan shift. The researchers in [18, 23, 24] develop low power test pattern generation technique for test-per-scan BIST that generates test patterns with low toggle characteristic. M. Filipek et al. propose a method that feeds scan chains with test patterns having low transition count [19]. However, these methods may cause test coverage loss for a given test length. In [20], the authors propose an adaptive low shift power PRTG. The technique monitors the transitions occurred during shifting out test responses and applies observed information to adjust dynamically the correlation among adjacent test stimulus bits from PRTG. Thus, it reduces shift power and avoids significant fault coverage loss as well. The method proposed in [21] reduces shift-power by eliminating the specified high-frequency parts of vectors and also reduces capture power. The paper [25] describes a low power programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage by automatically selecting several controls of the generator. The technology decreases test coverage loss, but requires complicated control logics.

In this paper, we propose a low switching activity test scheme for scan-based BIST. The scheme inserts a multiplexer at each scan input. These multiplexers select one of two data sources: previous scan value into the scan chain and pseudorandom test data generated by PRTG. In this manner, the scheme applies low toggle test stimulus bits among adjacent scan cells with a specified probability resulting in shift power reduction. In order to improve the tradeoff between test effectiveness decrease and test power reduction, we consider allowing a fraction of scan chains to receive fully pseudorandom test data. As a result, our technique reduces shift power significantly while suppressing fault coverage loss.

We will introduce our scheme step by step. Firstly, we propose a method described in section II. We analyze the advantage and disadvantage of the method. Then, in order to overcome the disadvantage of the proposed method we make a modification and present a modified form described in section III. This modified form of proposed scheme inherits the main properties from the previous scheme, but suppresses the fault coverage loss effectively.

II. THE LOW SWITCHING ACTIVITY BIST SCHEME

1. The Architecture of the Proposed Low Switching Activity BIST Scheme

It is conceivable that delivering the same value to the scan chains with a specified probability can reduces the number of transitions at scan inputs during scan shift, and thus reduces switching activity in whole CUTs during overall scan tests.

To implement this idea, we propose a low switching activity BIST (LSA-BIST) scheme for scan-based testing, as shown in Fig. 1. In this scheme, the outputs of the PRTG are connected with a phase shifter (PS). A well designed phase shifter (implemented with an XOR network) can be used to break the signal interdependence effectively when the number of its outputs is very large. In this scheme, we choose LFSR as PRTG. A detailed description for PRTG and PS is illustrated in Fig. 2. We cluster the scan cells into *N* scan chains. We insert 2-to-1 multiplexers between PS outputs and scan chain inputs. The outputs of the multiplexers are connected with scan

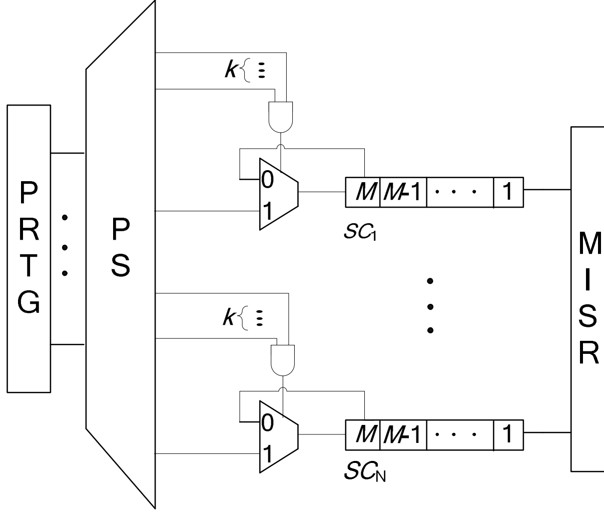

Fig. 1. The architecture of low switching activity BIST scheme.

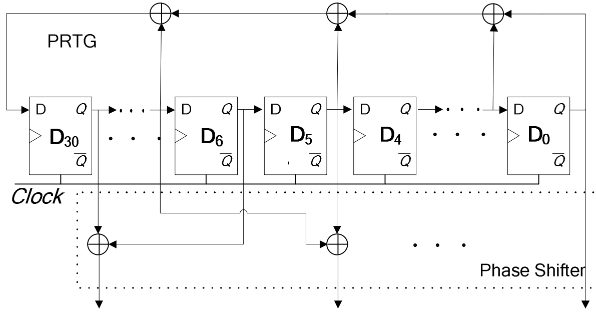

Fig. 2. The PRTG and Phase Shifter in the proposed scheme.

chain inputs. At a scan clock cycle, either pseudorandom test stimulus directly from PRTG or previous shift value from the first scan cell of each scan chain are selected to shift into scan chain via these multiplexers. A k-input AND gate is placed at the control input end of each multiplexer for the behavioral control. AND gate inputs are connected with PS outputs. When the AND gate output is 0, i.e. the control input of the corresponding multiplexer is 0, the previous shift value is selected and shifted into the scan chain input repetitively. Otherwise, if the AND gate output is 1, i.e. the control input of the multiplexer is 1, pseudorandom test stimulus provided by PRTG is shifted into the scan chain. The input count of AND gate determines the toggle rate at each scan chain input. The outputs of scan chains are connected with the multiple input signature register (MISR). The test responses compacted by MISR are compared with theoretical results for fault analysis.

2. Transition Probability Analysis in Scan Chain Inputs

When a scan chain is driven by a traditional LFSR, the transition probability of its input is nearly 0.5. In contrast, applying low transition test stimulus decreases transition probability of scan inputs. Assigning the same values to adjacent scan cells can break the uniformity of 0 and 1 distribution and may decrease fault detection efficiency. Now, we analyze transition probability at a scan chain input in the power-aware scheme. We define the transition probability of a scan input SC_i as the probability that value val(val={0,1}) is assigned to SC_i at a clock cycle while the opposite value $\overline{val}$ is assigned to SC_i at next clock cycle. In order to make every possible test pattern appear, the toggle probability of any scan input should be 0.5.

Without losing reasonableness, we suppose the probability that the value of PS output is 0(or 1) is equal to 0.5. Therefore, the probability that AND gate input is assigned 0(or 1) is equal to 0.5. The probability that 1-input of the multiplexer is assigned 0(or 1) is also equal to 0.5. Let the input number of the AND gate is k. The probability that the output of the AND gate is assigned a 1 during a scan cycles is given by $P_{and}(1)=0.5^k$. Since transition appears in the input of a scan chain only when control input of the multiplexer is 1 and the previous value in 1-input of the multiplexer is 0(or 1) and the current one is 1(or 0). The transition probability in a scan chain input is given by

$$P(\text{toggle})=P_{and}(1)*[P_{pre}(1)*P_{cur}(0)+P_{pre}(0)*P_{cur}(1)] = 0.5^k *(0.5*0.5+0.5*0.5)= 0.5^{k+1}, \quad (1)$$

where $P_{pre}(0/1)$ and $P_{cur}(0/1)$ is the probability that the previous and current value in 1-input of the multiplexer is 0/1 respectively. In order to suppress possible fault coverage loss caused by applying low transition test patterns, only k =1, 2 or 3 are recommended. It's should be noted that the control input of the multiplexer is connected with PS output directly when k=1.

3. Shift Power and Test Coverage Simulation for the LSA-BIST Scheme

To evaluate the power consumption and test coverage

Table 1. Simulation results for the LSA-BIST scheme

Circuit	#scan	Test Length	LFSR		*k*=1		*k*=2		*k*=3	
			FC%	WSA	FC% (chg%)	WSA red. %	FC% (chg%)	WSA red.%	FC% (chg%)	WSA red.%
S5378	10	65536	99.13	1565	98.50 (-0.63)	25.8	96.20 (-2.93)	39.2	92.48 (-6.65)	47.9
S9234	10	524288	91.58	2843	93.22 (1.64)	33.7	92.67 (1.09)	48.1	91.86 (0.28)	62.8
S13207	15	132072	98.28	4671	97.20 (-1.08)	32.2	92.99 (-5.29)	51.4	87.56 (-10.72)	53.5
S15850	15	132072	94.34	4541	96.19 (1.85)	35.6	94.42 (0.08)	52.1	93.74 (-0.6)	58.9
S35932	20	128	89.76	10478	88.39 (-1.37)	31.8	86.08 (-3.68)	54.9	85.05 (-4.71)	58.4
S38417	20	132072	97.41	12890	95.68 (-1.73)	35.8	94.84 (-2.57)	55.7	94.20 (-3.21)	60.7
S38584	20	132072	95.65	10247	95.54 (-0.11)	37.8	94.20 (-1.45)	54.6	92.85 (-2.8)	61.3
Average	-	-	95.16	-	94.96 (-0.2)	33.2	93.06 (-2.1)	50.9	91.11 (-4.05)	57.6

for the LSA-BIST scheme, experiments are performed on large ISCAS'89 benchmark circuits. The weighted switching activity (WSA) is used to evaluate test power. The WSA of a gate g is the number of state switches (N_{swi}(g)) at the gate multiplied by the number of gate fan-out (N_{fan}(g)) added 1. The WSA of CUT in a period is calculated by summing the WSA of all the gates whose state changed, i.e.

$$WSA_{\text{total}} = \sum_{\forall g \in \text{CUT}} (N_{\text{fan}}(g) + 1) \times N_{\text{swi}}(g) \qquad (2)$$

The fault simulation results for stuck-at faults and WSA evaluation results are shown in Table 1. Four simulation runs are carried out for each circuit. In the experiments, LFSR whose size is set as 30 or 40 is used as PRPG. In Table 1, Column 2-3 designate the number of scan chains and the number of applied test patterns. Under the column LFSR, the sub-columns labeled *FC %* and *WSA* show the achieved fault coverage and WSA per test pattern on average for conventional LFSR test scheme. The fault coverage and the shift power reduction compared with conventional LFSR test scheme are listed under the sub-columns *FC %*(*Chg %*) and *WSA Red. %* for the LSA-BIST schemes with *k*=1, *k*=2 and *k*=3, respectively. The fault coverage change related to conventional LFSR is also listed under the sub-columns *FC%*(*Chg %*) for *k*=1, *k*=2 and *k*=3, respectively. The negative numbers in fault coverage change indicates fault coverage loss when comparing with conventional LFSR test scheme. Otherwise, it indicates fault coverage gain. The variable *k* denotes the input number of AND gate.

It can be seen that significant test power reduction is achieved by the proposed scheme especially for test case with large *k*. However, fault coverage is also reduced for the benchmark circuits except for S9234 and S15850. The fault coverage loss becomes more significant as *k* increases. The low transition test patterns have the 1s and 0s with equal probability, but it increases the identical probability in neighboring scan cells. That is, the bit string 00 and 11 will appear often, while bit string 01 and 10 will become sparse. This degrades the uniformity of 0-1 distribution and makes the test patterns for some detectable faults unable to appear. This is why fault coverage is reduced for a given test length.

Since test coverage loss may make defective chips escape from test, it motivates us to find a new approach that can suppress the test coverage loss while not deteriorating the shift power reduction ratio significantly. In the following section, we will describe the modified form of the proposed LSA-BIST scheme to achieve this goal.

III. THE MODIFIED FORM OF THE LSA-BIST SCHEME

1. The Architecture of the Modified Form of LSA-BIST Scheme

It's been found that in logic BIST effective test

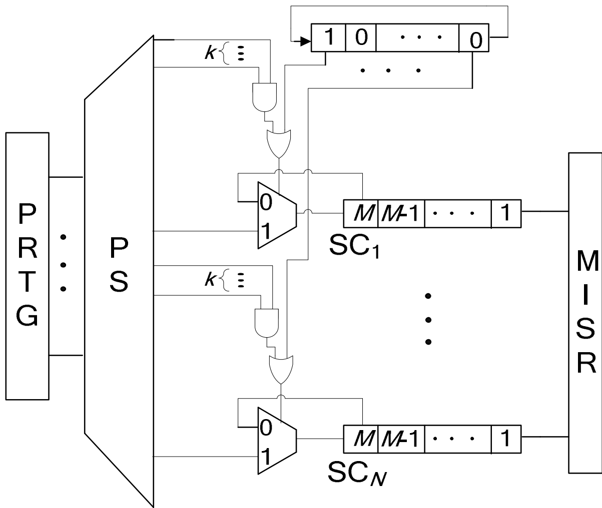

Fig. 3. The architecture of modified low switching activity BIST scheme.

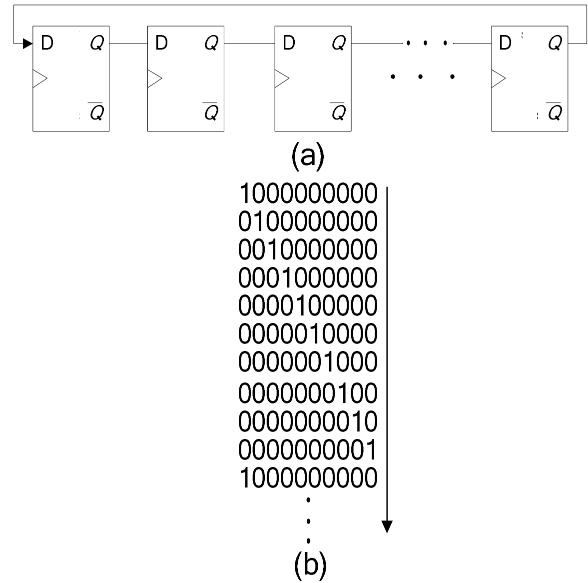

Fig. 4. The architecture of CSR and its state transition in the example.

patterns able to detect additional faults are quite sparse after a few dozens of test cycles and often less than one test pattern in a hundred detects new faults [22]. In most cases, such an effective test pattern contains only a few care bits. Hence, shifting pseudorandom test data to a fraction of scan cells can hit the effective test patterns with very high probability. That is, it is usually enough for keeping detection effectiveness of a BIST pattern.

Inspired by the fact above, we consider allowing a small fraction of scan chain to receive pseudorandom test data and other scan chains to receive low transition test stimulus bits just as in the low power scheme described in section II. This modified form of the LSA-BIST scheme will not deteriorate the test power reduction ratio significantly. On the other hand, it improves the randomness of test data by a small margin, nevertheless, enhances the test effectiveness significantly.

Fig. 3 depicts the modified form of the low switching activity BIST (MLSA-BIST) scheme. This scheme inherits the main properties from the LSA-BIST scheme described in section II. Somewhat differently, the MLSA-BIST scheme embeds an N-bits cyclic shift register (CSR) in the chip. The CSR consists of D flip-flops as shown in Fig. 4(a). Each bit of CSR controls the input of a multiplexer through a 2-input OR gate. The other input of the OR gate is connected to a AND gate output. If set properly, the CSR can control the multiplexer whether to select pseudorandom test data from PRTG persistently when shifting into a test pattern. During scan shift operation, the corresponding OR gate output is 1 if a bit in CSR is 1. As a result, the corresponding control input of the multiplexer is also assigned 1. This means that the corresponding scan chain can receive pseudorandom test data from PRTG persistently during the period that a test pattern is shifted into scan chains. If a bit in CSR is 0, then the OR gate output is determined by the AND gate output. In this case, either pseudorandom test stimulus directly from PRTG or previous shift value from the first scan cell of each scan chain are selected with a specified probability to shift into a scan chain.

2. The Test Flow of the MLSA-BIST Scheme

The test flow is depicted briefly as below. For convenience's sake, a scan chain that receives pseudorandom test data at a test cycle is referred to as "pseudorandom scan chain" hereinafter. Supposed that, in the scheme a scan chain is selected as pseudorandom scan chain at a time. At the beginning of test, we initialize the CSR so that only one bit is 1 and the other bits are 0's as shown in Fig. 4(b). The state of CSR is changed only before shifting into a new test pattern. For example, if the current values in the CSR are 10…00, that is only the first scan chain (SC_1) receives

Table 2. Simulation results for MLSA-BIST scheme and low power scheme in [18]

Circuit	#scan	Test Length	*k*=1		*k*=2		*k*=3		Low power [18]	
			FC%	WSA red. %	FC%	WSA red. %	FC%	WSA red. %	FC%	WSA red. %
S5378	10	65536	98.68 (-0.45)	24.2	97.85 (-1.28)	36.9	**97.11** (-2.02)	43.8	96.54	43
S9234	10	524288	93.34 (1.76)	30.1	93.11 (1.53)	46.7	**92.54** (0.96)	59.8	90.89	62
S13207	15	132072	97.95 (-0.33)	30.2	**94.22** (-4.06)	**48.8**	93.47 (-4.81)	50.2	93.66	45
S15850	15	132072	96.14 (1.8)	32.8	96.17 (1.83)	50.5	**95.95** (1.61)	57.6	94.40	58
S35932	20	128	89.59 (-0.17)	29.5	89.10 (-0.66)	49.2	**88.74** (-1.02)	58.7	87.84	56
S38417	20	132072	96.32 (-1.09)	33.9	96.08 (-1.33)	50.7	**95.62** (-1.79)	61.5	94.99	56
S38584	20	132072	95.63 (-0.02)	32.9	95.17 (-0.48)	50.6	**94.83** (-0.82)	60.3	93.35	59
Average	-	-	95.38 (0.22)	30.5	94.53 (-0.63)	47.6	**94.04** (-1.12)	56.0	93.10	54.1

pseudorandom test data during shifting in a test pattern. For other scan chains except for SC_1, the control input of the corresponding multiplexer is set to 1 when all the inputs of the corresponding AND gate is assigned 1 at a clock cycle. At the cycle, pseudorandom test stimulus provided by PRTG is shifted into the scan chain. If at least one input of the AND gate is assigned 0 at a clock cycle, the control input of the corresponding multiplexer is certainly set to 0. At this cycle, the previous shift value is selected and shifted into the scan chain repetitively. Test data are shifted in scan chains from scan inputs (multiplexer outputs) while the test responses captured in them are shifted out. The CSR is shifted one bit cyclically to the right just before shifting into next test pattern. The state transition of CSR is also illustrated in Fig. 4(b). There is always pseudorandom scan chain for every test pattern. Furthermore, the pseudorandom scan chain would change cyclically. After shifting in a test pattern, CUT goes into normal mode for capturing test responses. Then, CUT returns to test mode for shifting into test pattern. The test flow is repeated until all the test patterns are applied.

3. Determination of the Parameter *k*

In specific applications one can select the smaller *k* if the high test coverage requirement is top-priority. Otherwise, the larger *k* can be considered. In order to reduce possible loss in fault coverage, only the schemes with *k*=1, 2 or 3 are recommended.

IV. EXPERIMENTAL RESULTS

To verify the efficiency of the MLSA-BIST scheme, experiments are performed on the same ISCAS'89 benchmark circuits as those in simulation of the previous scheme. The weighted switching activity is also used to evaluate test power.

Table 2 shows the simulation results for MLSA-BIST scheme. The scheme also uses LFSR as PRPG whose size is set as 30 or 40. Three fault simulation runs are also carried out for each circuit. In Table 2, column 2-3 designate the number of scan chains and the number of applied test patterns which are same as those in Table 1. In the experiments, only one scan chain is selected as pseudorandom scan chain for every design. The fault coverage and the test power reduction are listed under the sub-columns *FC%*(*Chg%*) and *WSA Red.%* for the MLSA-BIST scheme with *k*=1, *k*=2 and *k*=3, respectively. The fault coverage change related to conventional LFSR is also listed under the columns *FC%*(*Chg%*) for *k*=1, *k*=2 and *k*=3, respectively. The negative and positive numbers in fault coverage change indicates the same meanings as those in Table 1.

Table 2 also gives comparison of the MLSA-BIST scheme with the effective low power test scheme proposed in [18]. In the both schemes, the same number of test patterns for each benchmark circuit is applied as

shown in third column of Table 2. Under the column low power [18], the sub-columns labeled FC % and WSA Red.% show the achieved fault coverage and the test power reduction for the low power scheme [18]. All the test power reduction results in the table are calculated by comparing with conventional LFSR test scheme.

As shown in the Table 2, the amount of WSA reduction increases as the input number of AND gate increases. Comparing with the results in Table 1 for LSA-BIST scheme, the test power reduction percentage for the MLSA-BIST scheme is changed slightly. However, the MLSA-BIST scheme suppresses the fault coverage loss effectively. The larger the variable k is selected in the MLSA-BIST scheme, the more the fault coverage gain (or less the fault loss) can be achieved. For example, the fault coverage gain for k=3 is 2.93% (from 91.11% to 94.04%) on average while it is 0.42% (from 94.96% to 95.38%) for k=1.

It can be seen that, when compared with the technique in [18] the proposed MLSA-BIST scheme with k=3 achieves the sub-equal WSA reduction, but it can attain higher fault coverage for all benchmark circuits except for S13207.

In order to further explain the efficiency of the MLSA-BIST method, Table 3 provides a comparison with another effective low power BIST scheme [24]. In the table, all of the fault coverage changes and the power reduction percentages are calculated by taking the power results of the random X-fill as a comparison baseline. When comparing the MLSA-BIST scheme with k=1 and the scheme in [24], there is little difference in the fault coverage changes, but the proposed technique delivers the higher power reductions for all benchmark circuits.

The area overhead of the proposed MLSA-BIST scheme consists of an N-bit CSR, N AND gates, N OR gates and N 2-to-1 multiplexers. The additional logic depends on the number of scan chains. Table 4 presents area overhead details for the MLSA-BIST scheme in the experiments. The area overhead means the percentage of extra hardware overhead compared with original circuit size. Area overhead is estimated based on the cell library class.lib of the Synopsys system [26]. The extra AND gate in MLSA-BIST brings more area overhead as its input number increases. However, the difference is tiny. The table presents only the area overhead for the MLSA-BIST scheme with k=3. The additional logics are very trivial in relation to the circuit size. (The area overhead results are not given in these compared schemes, so no such comparisons are given.)

Table 3. Comparison between the MLSA-BIST scheme and the scheme in [24]

Circuit	The scheme [24]		k=1	
	FC Chg%	FC Chg%	FC% Chg%	WSA red. %
S13207	-0.38	22.4	-0.33	30.2
S15850	-1.75	29.8	1.8	32.8
S35932	0	9.9	-0.17	29.5
S38417	0	16.5	-1.09	33.9
S38584	-0.35	11.8	-0.02	32.9
Average	-0.50	**18.1**	0.04	**31.9**

Table 4. Area overhead for the MLSA-BIST scheme

Circuit	Area Overhead% (k=3)
S5378	4.2
S9234	2.4
S13207	2.6
S15850	2.4
S35932	1.0
S38417	1.0
S38584	0.9
Average	2.1

V. Conclusions

Currently, logic BIST becomes vital for digital system debug and field test. This paper firstly proposes a power-aware BIST technology that applies low transition test data. This scheme reduces switching activity in CUT significantly, but causes significant fault coverage loss. For improving the tradeoff between power consumption reduction and fault coverage loss, a modified form of the low power BIST scheme is also presented in the paper. The modified form applies low transition test stimulus into most of scan chains. Meanwhile, it allows a small fraction of scan chain to receive pseudorandom test data from PRTG. The proposed technique reduces the switching activity significantly and suppresses fault coverage loss effectively as well with little area overhead. Experimental results on several larger ISCAS’89 benchmark circuits demonstrate the efficiency of the proposed technique.

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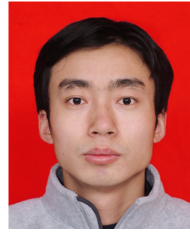

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