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A Capacitor Mismatch Error Cancelation Technique for High-Speed High-Resolution Pipeline ADC

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** Short Paper*

***Abstract*:** An accurate gain-of-two amplifier, which successfully reduces the capacitor mismatch error is proposed. This amplifier has similar circuit complexity and linearity improvement to the capacitor error-averaging technique, but operates with two clock phases just like the conventional pipeline stage. This makes it suitable for high-speed, high-resolution analog-to-digital converters (ADCs). Two ADC architectures employing the proposed accurate gain-of-two amplifier are also presented. The simulation results show that the proposed ADCs can achieve 15-bit linearity with 8-bit capacitor matching.

***Keywords*:** Pipeline ADC, Calibration, Capacitor error-averaging, Spurious free dynamic range(SFDR), Signal to noise and distortion ratio(SNDR), Effective number of bit(ENOB).

1. Introduction

Recently, an increasing number of applications, such as wireless communication systems, imaging and instrumentation, require high-speed, high-resolution ADCs. The pipeline ADC architecture is the best for these applications among the various ADC architectures available. On the other hand, pipeline ADCs suffer from a variety of errors in the analog domain, such as finite operational amplifier (opamp) gain, charge-injection, comparator offset, and capacitor mismatch, etc. Fortunately, most of them can be fixed using a range of design techniques. For example, a finite opamp gain error can be suppressed by a high gain opamp using gain-boosting techniques [1]; even a 130dB DC gain was reported [2]. Charge-injection can be converted to common-mode noise and be removed by a differential architecture using a careful switching scheme, such as bottom-plate sampling. The comparator offset is greatly relaxed by the digital error correction technique [3]. On the other hand, capacitor mismatch depends heavily on IC processes and it is difficult to fix. Several calibration techniques have been developed. Digital calibration techniques [4-8] move the errors in the analog domain to the digital domain in various ways, but they often increase the circuit complexity and power consumption. Multi-bit per stage is also used widely to relax the capacitor matching requirements of the stage analog output.

On the other hand, complicate layout can also increase the mismatch errors, making it difficult to achieve high linearity. The ratio-independent algorithmic technique [9], the feedback-capacitor commutating technique [10], and the capacitor error-averaging techniques [2, 11, 12] are analog calibration techniques. These techniques are simpler than digital ones. On the other hand, they often limit the ADC speed, because they require additional clock phases to cancel any mismatch errors. The capacitor error-averaging technique is one of the most powerful calibration techniques. This method is relatively simple compared to other techniques, but it requires an additional phase to average out any mismatch errors. The procedure operates with three clock phases [11, 12] or four clock phases [2] and only slow ADCs have been reported (less than 20Msample/s) using this technique.

The aim of this study was to develop an analog calibration technique that suppresses capacitor mismatch errors without compromising the speed.

2. Proposed Techniques

A fundamental speed limitation of the capacitor error-averaging technique originates from the fact that the capacitor mismatch error is averaged out after the

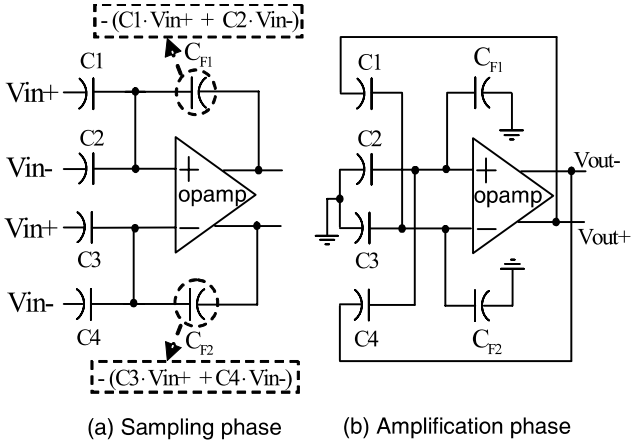


Fig. 2. Proposed Accurate gain-of-two Amplifier.

amplification phase, which requires an additional phase (averaging phase). To overcome this limitation, capacitor mismatch error must be sampled during the sampling phase and canceled out during the amplification phase. This is the underlying principle of the proposed accurate gain-of-two amplifier.

2.1 Proposed Accurate gain-of-two Amplifier

Fig. 1 presents the proposed accurate gain-of-two amplifier. The basic concept is that capacitor mismatch errors are sampled on feedback capacitors, C_{F1} and C_{F2}, during the sampling phase and added to the amplifier output with opposite polarity in the amplification phase, thus reducing the capacitor mismatch errors to the second order. The model assumes that all capacitors are of the same size with small mismatches, and are fully discharged before the sampling phase. In the sampling phase, the positive input V_{in+} is sampled on capacitors C_1 and C_3 and the negative input V_{in-} is sampled on C_2 and C_4. Because the charge on C_1 and C_2 is from C_{F1} and the charge on C_3 and C_4 is from C_{F2}, the charge on C_{F1} is $-(C_1 \cdot V_{in+}+C_2 \cdot V_{in-})$ and C_{F2} is $-(C_3 \cdot V_{in+}+C_4 \cdot V_{in-})$. In the amplification phase, C_1 is connected to C_3 and C_{F2}, C_4 is connected to C_2 and C_{F1}. From the charge conservation law,

$$C_1 \cdot V_{out+} = (C_1 + C_3) \cdot V_{in+} - \underbrace{(C_3 \cdot V_{in+} + C_4 \cdot V_{in-})}_{=Q_{C_{F2}}}$$
$$= C_1 \cdot V_{in+} - C_4 \cdot V_{in-} \quad (1)$$
$$V_{out+} = V_{in+} - \frac{C_4}{C_1} \cdot V_{in-}$$

$$C_4 \cdot V_{out-} = (C_2 + C_4) \cdot V_{in-} - \underbrace{(C_1 \cdot V_{in+} + C_2 \cdot V_{in-})}_{=Q_{C_{F1}}}$$
$$= C_4 \cdot V_{in-} - C_1 \cdot V_{in+} \quad (2)$$
$$V_{out-} = V_{in-} - \frac{C_1}{C_4} \cdot V_{in+}$$

From (1) and (2),

$$V_{out+} - V_{out-} = V_{in+} - V_{in-} + \frac{C_1}{C_4} \cdot V_{in+} - \frac{C_4}{C_1} \cdot V_{in-} \quad (3)$$

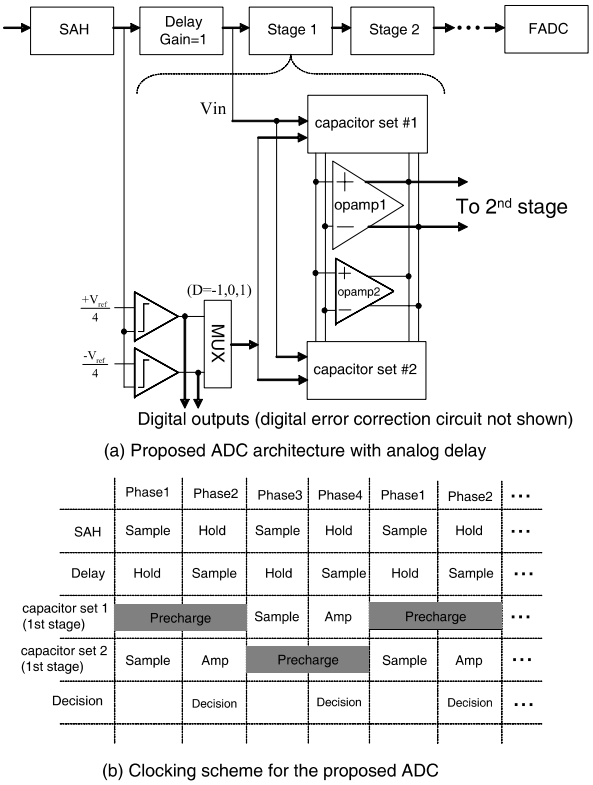


Fig. 1. Proposed ADC architecture and clocking scheme.

Assuming C1 = C and C4 = (1+ε) · C,

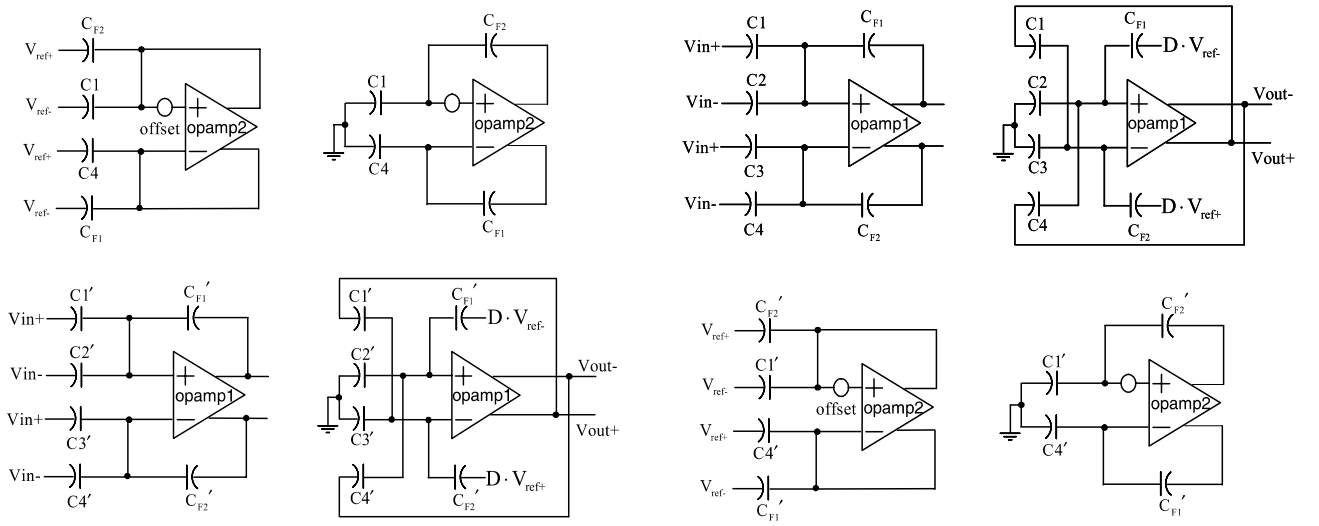
$$\frac{C_4}{C_1} = (1+\varepsilon), \quad \frac{C_1}{C_4} = \frac{1}{(1+\varepsilon)} \simeq (1-\varepsilon) \quad (\varepsilon \ll 1) \quad (4)$$

From (3) and (4),

$$V_{out+} - V_{out-} \simeq V_{in+} - V_{in-} + (1-\varepsilon) \cdot (V_{in+}) - (1+\varepsilon) \cdot V_{in-}$$
$$\simeq 2 \cdot (V_{in+} - V_{in-}) - \underbrace{\varepsilon \cdot (V_{in+} + V_{in-})}_{=0} \quad (5)$$

Because $V_{in+}=^{\Delta Vin}/_2$ and $V_{in-}=-^{\Delta Vin}/_2$, $\varepsilon \cdot (V_{in+}+V_{in-})=0$.

From the above equations, it is clear that the capacitor mismatch error is canceled out during the amplification phase, i.e., no additional phase is required and this amplifier is suitable for high-speed applications. The additional capacitors C_{F1} and C_{F2} reduce the feedback factor from $^1/_3$ to $^1/_4$ (assuming the opamp input capacitance is similar to that of C_{F1}) and increase the settling time during the amplification phase compared to the conventional gain-of-two amplifier, but they relax the opamp significantly during the sampling phase. In the sampling phase, the amount of charge on C_1 and C_2 are similar with opposite polarity, which means most of the charge stored on C_1 and C_2 comes from each other just like passive sampling. Therefore, the opamp does not need to have a large signal swing and high DC gain because it only needs to charge the feedback capacitors with the small



(a) Phase 1(sampling phase 1) (b) Phase 2(amplification phase 1) (c) Phase 3(sampling phase 2) (b) Phase 4(amplification phase 2)

Fig. 3. Proposed 1.5-bit pipeline stage with reference error cancelation.

errors caused by capacitor mismatch between C_1 and C_2 (for example, 0.1% capacitor mismatch and $2V_{pp}$ input signal swing produces 2mV opamp output). This makes it possible to use the partially switched two-stage opamp, which is similar to the one proposed in [13]. The second stage can be turned off during the sampling phase to reduce the power consumption.

2.2 Proposed ADC architectures

Although the proposed amplifier successfully performs accurate gain-of-two function, it requires two important modifications to be used in a pipeline stage. The first is that all capacitors must be discharged before the sampling phase. This can be achieved easily using two capacitor sets. While one set of capacitors is performing the accurate gain-of-two operation, the other set is fully discharged. In the next cycle, two capacitor sets exchange their roles. Small errors introduced by mismatch of the two capacitor sets are also suppressed by an accurate gain-of-two action. Thus, the channel offset and gain mismatches that introduce tones at $^{Fs}/_{2}$ and $^{Fs}/_{2}$-F_{in} like two-channel time-interleaved ADC [14] are almost negligible, which was verified by simulation with approximately 8-bit capacitor matching between channels. Second, the reference signals $\pm$Vref (V_{ref+}-V_{ref-}) or 0 should be added to the amplifier output accurately depending on the stage input amplitude. An explicit way of solve the problem is precharging capacitors C_1 and C_4 with V_{ref+} or V_{ref-} depending on the input amplitude. This, however, is possible only when the input amplitude is determined at least one clock period earlier than the sampling phase, which is quite expensive because two analog delay circuits are needed between the front-end sample and hold circuit (SAH) and the first stage (each accounts for half a period of delay) to give the first stage sufficient time to precharge capacitors C_1 and C_4 before the sampling input. Fig. 2 presents an alternative way with only one analog delay circuit and Fig. 3 describes a detailed 1.5-bit stage. The four clock phases are defined as follows: phases one and two are the precharging phases of capacitor set one, and the sampling and amplification phase of capacitor set two, respectively, and phases three and four are precharging phases of capacitor set two and the sampling and amplification phase of capacitor set one, respectively. During the precharging phases, capacitors C_{F1} and C_{F2} or C_{F1}' and C_{F2}' are precharged with the reference errors caused by the capacitor mismatches. In phase one, capacitors C_1, C_4, C_{F1}, and C_{F2} of capacitor set one sample the reference (V_{ref+} or V_{ref-}), as shown in Fig. 2, while the other set is used to sample the input signal. In phase two, the charge on C_1 and C_4 is transferred to C_{F2} and C_{F1}, respectively, so the charge on C_{F1} is $C_4 \cdot V_{ref+} + C_{F1} \cdot V_{ref-}$ and C_{F2} is $C_1 \cdot V_{ref+} + C_{F2} \cdot V_{ref-}$, and they are used to cancel out the reference errors caused by the capacitor mismatch between C_1 and C_{F1} (or C_{F2}), C_4 and C_{F2} (or C_{F1}) during the amplification phase (phase four). At the same time, capacitor set two is used to amplify the input signal. A decision is also made after a small delay (immediately after the SAH opamp enters the linear settling region) according to the SAH output during this phase. This is the early comparison technique described elsewhere [16]. In phase three, the input signal is sampled on capacitor set one and the capacitors C_1', C_4', C_{F1}' and C_{F2}' of capacitor set two are used to sample the references. In phase four, C_{F1}' and C_{F2}' are charged with reference errors and capacitor set one goes to amplification mode connecting C_{F1} and C_{F2} to V_{ref+}, V_{ref-} or 0 according to the decision signal.

When $V_{in} > {}^{Vref}/_{4}$, Eq. (1) should be modified as follows:

$$C_1 \cdot V_{out+} + C_{F2} \cdot V_{ref+} = (C_1 + C_3) \cdot V_{in+} - (C_3 \cdot V_{in+} + C_4 \cdot V_{in-}) + C_1 \cdot V_{ref-} + C_{F2} \cdot V_{ref+}$$

$$V_{out+} = V_{in+} - \frac{C_4}{C_1} \cdot V_{in-} + V_{ref-} \quad (6)$$

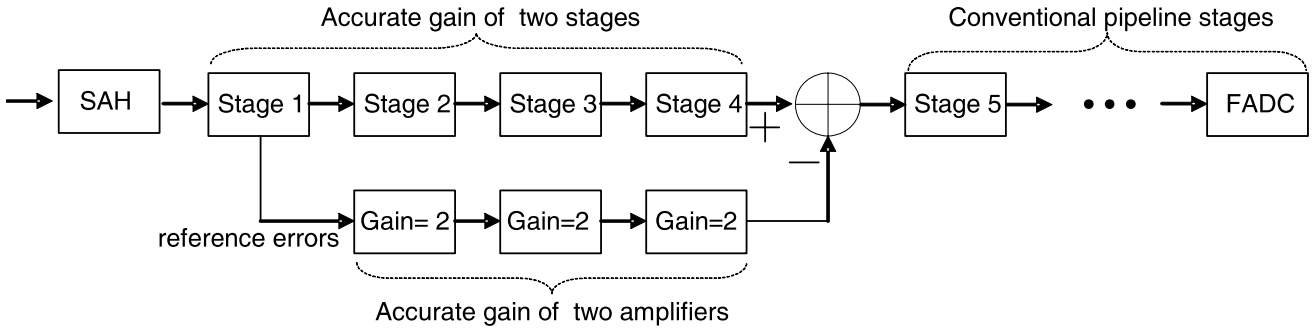


Fig. 4. Proposed ADC architecture without analog delay.

$$C_4 \cdot V_{out-} + C_{F1} \cdot V_{ref-} = (C_2 + C_4) \cdot V_{in-} - (C_1 \cdot V_{in+} + C_2 \cdot V_{in-}) + C_4 \cdot V_{ref+} + C_{F1} \cdot V_{ref-}$$
$$V_{out-} = V_{in-} - \frac{C_1}{C_4} \cdot V_{in+} + V_{ref+} \quad (7)$$

From (6) and (7),

$$V_{out+} - V_{out-} \simeq 2 \cdot (V_{in+} - V_{in-}) - (V_{ref+} - V_{ref-}) \quad (8)$$

When $V_{in} < -^{Vref}/_4$, the stage output can be obtained by switching C_{F1} and C_{F2} during the sampling phase. The equations described above can be modified as follows:

$$C_1 \cdot V_{out+} + C_{F1} \cdot V_{ref-} = (C_1 + C_3) \cdot V_{in+} - (C_3 \cdot V_{in+} + C_4 \cdot V_{in-}) + C_4 \cdot V_{ref+} + C_{F1} \cdot V_{ref-}$$
$$V_{out+} = V_{in+} - \frac{C_4}{C_1} \cdot V_{in-} + \frac{C_4}{C_1} \cdot V_{ref+} \quad (9)$$

$$C_4 \cdot V_{out-} + C_{F2} \cdot V_{ref+} = (C_2 + C_4) \cdot V_{in-} - (C_1 \cdot V_{in+} + C_2 \cdot V_{in-}) + C_1 \cdot V_{ref-} + C_{F2} \cdot V_{ref+}$$
$$V_{out-} = V_{in-} - \frac{C_1}{C_4} \cdot V_{in+} + \frac{C_1}{C_4} \cdot V_{ref-} \quad (10)$$

From (4),

$$\frac{C_4}{C_1} \cdot V_{ref+} - \frac{C_1}{C_4} \cdot V_{ref-} \simeq V_{ref+} - V_{ref-}$$
$$V_{out+} - V_{out-} \simeq 2 \cdot (V_{in+} - V_{in-}) + (V_{ref+} - V_{ref-}) \quad (11)$$

In the case of $-^{Vref}/_4 < V_{in} < {}^{Vref}/_4$, capacitors C_{F1} and C_{F2} or C_{F1}' and C_{F2}' will be quickly discharged during phase two after the decision is made before the sampling phase. The discharging time can be very short because the error signals on C_{F1} and C_{F2} are always small (less than several mV).

Three important facts should be mentioned.

(1) The second opamp (opamp2) can be small compared to the main opamp (opamp1) because it only processes small mismatch errors (less than several mV) and any errors introduced by incomplete settling and finite opamp gain appear as second-order effects.

(2) The second opamp offset should be removed by an auto-zero technique because the opamp offset combined with capacitor mismatch between channels can introduce offset error at $^{Fs}/_2$ like a two-channel time-interleaved ADC [14].

(3) Analog delay in front of the first stage is expensive. This increases thermal noise ($^{kT}/_C$) and power consumption considerably.

Fig. 4 also shows the second approach without analog delay employed in the 15-bit ADC. This approach consists of 4 MSB accurate gain-of-two stages and 10 conventional stages with the assumption that 10-bit matching is allowed with careful layout, but a more accurate gain of two stages can be used depending on matching if necessary. Without analog delay, the reference error cancelation technique described above can only be used from the second stage because it is possible from the second stage to predict the input amplitude half clock earlier using a similar scheme described elsewhere [15]. On the other hand, the feedback capacitors C_{F1}, C_{F2}, C_{F1}', and C_{F2}' of the first stage cannot be precharged with reference errors because it is impossible for the first stage to predict the input amplitude without analog delay. Instead of removing the errors at the first stage, it can be canceled out at a later stage. The first stage, the reference error is sampled and multiplied by 8 through 3 additional accurate gain-of-two amplifiers just like the reference error in the first stage residue, and then subtracted from 4th stage residue. Although the error is multiplied by 2 every stage, it is still small enough to be cured by a digital error correction with comparator offsets. The additional accurate gain-of-two amplifiers can be very small because they amplify only small error signals, and the capacitors used in the amplifiers are small (equal to the 4th stage capacitor). They consume less power than the analog delay circuit does.

3. Simulation Results

A transistor-level simulation was performed on the proposed accurate gain-of-two amplifier. The circuit was designed using 0.18μm CMOS technology with 95dB DC gain opamp and CMOS switches. Approximately 15-bit linearity was achieved with capacitor mismatches of 1%. Behavioral models of a 15-bit pipeline ADCs were built and simulated to verify the effectiveness of the proposed

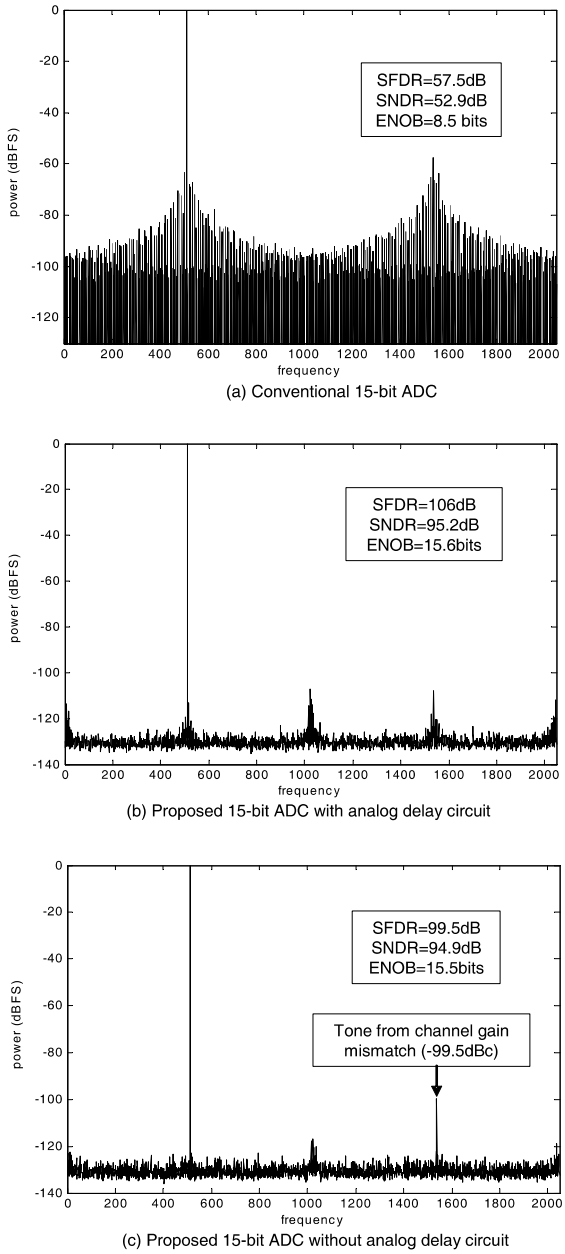


Fig. 5. Averaged FFT plots with same capacitor mismatch distribution.

architectures. Only the capacitor mismatch errors were included in the simulation with the assumption that the other errors would be suppressed to the second order using the range of techniques discussed before. The capacitor mismatch was also assumed to have a Gaussian distribution with zero mean and 0.005 standard deviation and was uncorrelated. For example, $C_1 = C \cdot (1+\varepsilon)$, where $\varepsilon \sim N(0,0.0005^2)$. To observe the difference clearly, the averaged FFTs were performed and depicted in Fig. 3 for the 15-bit ADCs (a) conventional architecture, (b) proposed architecture with an analog delay circuit, and (c) proposed architecture without analog delay circuit. The averaged FFT was based on the rms values of the magnitudes of frequency bins from 1000 runs. For both architectures, the SNDR is increased from 53dB to 95dB, resulting in 7-bit improvement in the ENOB. The SFDRs were improved by 48.5dB and 42dB for the first and second architectures, respectively. The additional accurate gain-of-two amplifier in the second approach increases the gain mismatch between the channels; hence reduces the SFDR, but the reduction is still tolerable.

4. Conclusion

A new accurate gain-of-two amplifier, which is particularly useful in high-speed high-resolution applications, has been described and modified to be used in pipeline ADCs. Two ADC architectures employing the proposed accurate gain-of-two amplifier are also presented and their performances were verified by simulations. The first architecture is more straightforward and has higher SFDR, but the second architecture is more power efficient. Both ADC architectures showed high linearity improvement from poor capacitor matching.

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