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Dependence of Electrons Loss Behavior on the Nitride Thickness and Temperature for Charge Trap Flash Memory Applications

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$Pt/Al_2O_3/Si_3N_4/SiO_2/Si$ charge trap flash memory structures with various thicknesses of the Si_3N_4 charge trapping layer were fabricated. According to the calculated and measured results, we depicted electron loss in a schematic diagram that illustrates how the trap to band tunneling and thermal excitation affects electrons loss behavior with the change of Si_3N_4 thickness, temperature and trap energy levels. As a result, we deduce that Si_3N_4 thicknesses of more than 6 or less than 4.3 nm give no contribution to improving memory performance.

Keywords: Charge trapping, Electrons loss behavior, Memory device

1. INTRODUCTION

Charge Trap Flash (CTF) memory devices, otherwise known as metal-oxide-nitride-oxide-silicon structures, have been the subject of attention in the semiconductor industry due to their advantages over conventional floating gate type memory. These advantages include lower programming voltage, superior programming/erasing speeds, and a simple fabrication process compatible with standard complementary metal-oxide-semiconductor technology [1-3]. Recently, CTF memory devices have gained increasing interest in the three dimensional (3D) integration for next generation nonvolatile memory technology [4,5]. The tunnel oxide thickness plays a crucial role in regulating the erasing speed, data retention characteristics and charge loss mechanisms for CTF memory devices [6], while the thickness of the nitride charge trapping layer is less critical. Nevertheless, in 3D architectures, the nitride thickness has a direct effect on charge storage performance and array density [7]. Moreover, temperatures [8] and trap energy levels [9,10] also are considerable factors for understanding the electron loss mechanisms. Hence, in this letter, $Pt/Al_2O_3/Si_3N_4/SiO_2/Si$ (MANOS) charge trapping memory capacitors with various thicknesses of nitride layer were fabricated. We investigated and analyzed the effect of nitride thickness, trap energy levels and temperatures on electrons loss behavior in the retention state for MANOS capacitors. Also, a reasonable nitride thickness range was obtained through electrical characteristic measurements. Four charge loss mechanisms [11,12] are involved in the data retention state for scaled CTF memory devices: trapped electrons tunnel from traps to the silicon conduction band (T-B), trapped electrons

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tunnel from traps to the Si/SiO_2 interface traps state (T-T), holes tunnel from the silicon valence band to nitride traps (B-T) and thermal excited trapped electrons from the traps to the nitride conduction band followed by tunneling through the tunnel oxide (T-E), as shown in Fig. 1. However, the T-B and T-E mechanisms are regarded as the two main electron loss mechanisms [11]. Therefore, in our case we only consider the T-B tunneling and T-E mechanisms.

2. EXPERIMENTS

The MANOS capacitors were fabricated on p-type (100) Si substrates with a resistivity of 8-12 Ω·cm. Prior to deposition, the p-Si were cleaned by the standard radio corporation of America (RCA) process. Then, these substrates were dipped in HF solution for one minute to remove the native oxide. After a growth of thermal SiO_2 tunnel oxide (TO) with a thickness of 3 nm in dry O_2 ambience, the nitride (Si_3N_4) as charge trapping layers (CTL) ranging from 1 to 6 nm were deposited by low pressure chemical vapor deposition at 700℃. Subsequently, a 8 nm Al_2O_3 layer was deposited as the blocking oxide (BO) by atomic layer deposition (ALD) using trimethylaluminium ($Al(CH_3)_3$) precursor at a substrate temperature of 300℃. The thickness of the samples was measured by a spectroscopic ellipsometer and transmission electron microscopy (TEM). Finally, platinum (Pt) top electrodes with an area of 7.85×10^{-5} cm^2 were deposited using magnetron sputtering at room temperature. Figures 2(a) and (b) show a schematic diagram and cross-sectional TEM image, respectively, of the charge trap flash memory device with a 5 nm Si_3N_4 CTL. The electrical characteristics of these memory capacitors were analyzed by a Keithley 4200 semiconductor characterization system.

3. RESULTS AND DISCUSSION

In order to have a quantitative understanding of the electrons loss mechanisms in the data retention state, we have calculated the time constant associated with the T-B and T-E processes to characterize the electrons loss behavior. The time constant of T-B, $\tau_{T\text{-}E}$, and the time constant of $\tau_{T\text{-}E}$ are written as [11]:

$$\tau_{T\text{-}B}=\tau_{T\text{-}B_0}\exp\left(\frac{4\pi}{h}\sqrt{2m^*_{TO}(E_B+E_T)}\,d_{TO}\right)\exp\left(\frac{4\pi}{h}\sqrt{2m^*_N E_T}\,x\right) \quad (1)$$

$$\tau_{T\text{-}E}=\left(AT^2\right)^{-1}\exp\left(\frac{E_T}{k_B T}\right) \quad (2)$$

where $\tau_{T\text{-}E}$ is a time constant [13], m^*_{TO}= 0.42 m_0 [14] and m^*_N = 0.25 m_0 [11] are the electron effective mass in the SiO_2 and Si_3N_4, respectively, here m_0 is the free electron mass. E_T is the trap energy level referenced to the conduction band edge in the Si_3N_4 (eV), q is the absolute electron charge, E_B=1.05 eV [15] is the energy barrier height of electron tunneling (eV), h is Planck's constant, d_{TO} is the thickness of the SiO_2 (nm), T is the absolute temperature (K), A is the temperature independent constant, k_B is Boltzmann's constant, t is the retention time (s) and is the tunneling distance in the Si_3N_4 measured from the SiO_2/Si_3N_4 interface as follows (nm):

$$x=\frac{h}{4\pi\sqrt{2m^*_N E_T}}\ln\left(\frac{t}{\tau_{T\text{-}B_0}\exp\left(\frac{4\pi}{h}\sqrt{2m^*_{TO}(E_B+E_T)}\,d_{TO}\right)}\right) \quad (3)$$

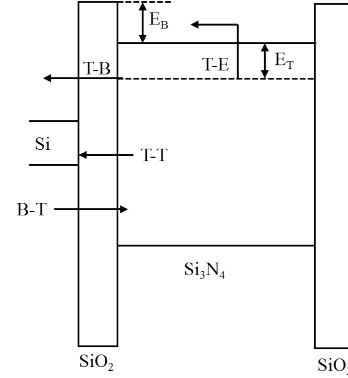

Fig. 1. Energy band diagram of a conventional CTF memory device, showing charge loss mechanisms: T-B, T-T, B-T, and T-E.

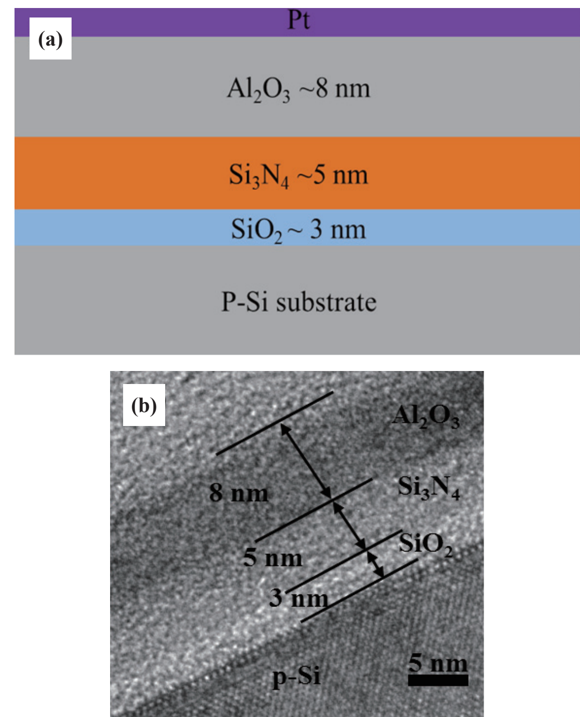

Fig. 2. (a) Schematic diagram and (b) cross-sectional TEM image of memory structure with a 5 nm thick Si_3N_4 layer.

We assumed that the traps are spatially uniform inside the Si_3N_4 with an arbitrary energy level distribution, and all traps are initially filled with electrons in the retention state. The BO absolutely restricts electrons tunneling to and from the gate electrode. Fig. 3(a) shows the results of the calculated time constant based on Eqs. (1) and (2). For the electrons captured by shallow trap energy levels ($E_T\leq$ 0.5 eV), $\tau_{T\text{-}E}$ ($<10^{-3}$ s) is at least 2 orders of magnitude smaller than $\tau_{T\text{-}B}$, suggesting that T-E is a much quicker electrons loss path than T-B tunneling. These trap energy levels cannot effectively capture electrons due to their smalland have no contribution to electron retention. If > 0.5 eV, T-B tunneling starts to influence electrons loss and the the two electron loss mechanisms compete with each other. At 273 K, a relatively small $\tau_{T\text{-}B}$ for electrons trapped near the TO (x<1 nm) suggests that T-B tunneling plays a leading role in the electrons loss process of the region. However, increases to 6 nm, $\tau_{T\text{-}B}$ increases at least 10 orders of magnitude, and the deeper the trap depth,

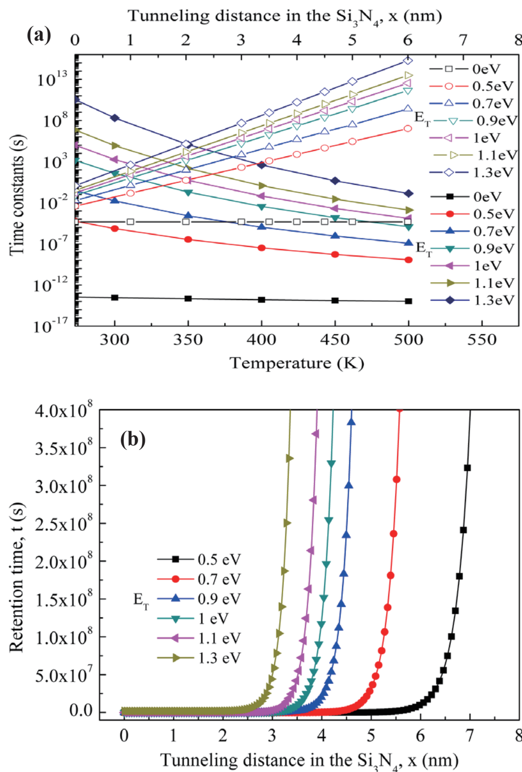

Fig. 3. (a) Calculated time constants of andat different trap energy level (0-1.3 eV). $\tau_{T\text{-}B}$ and $\tau_{T\text{-}E}$ are functions of tunneling distance in Si_3N_4 and temperature, respectively and (b) retention time versus tunneling distance in the Si_3N_4 (t-x) of MANOS capacitors. In the calculation, d_{TO}= 3 nm was used.

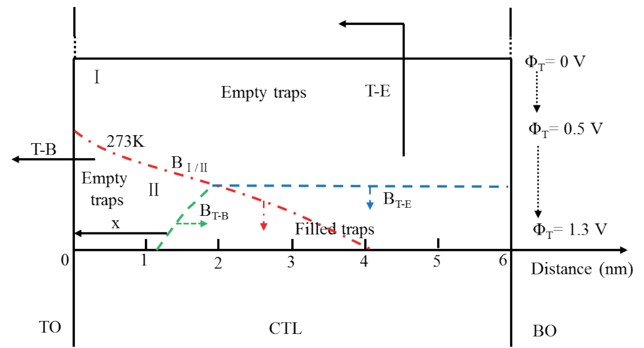

Fig. 4. Contribution of T-B and T-E tunneling to electron loss behavior in the retention state for MANOS capacitors at 273 K.

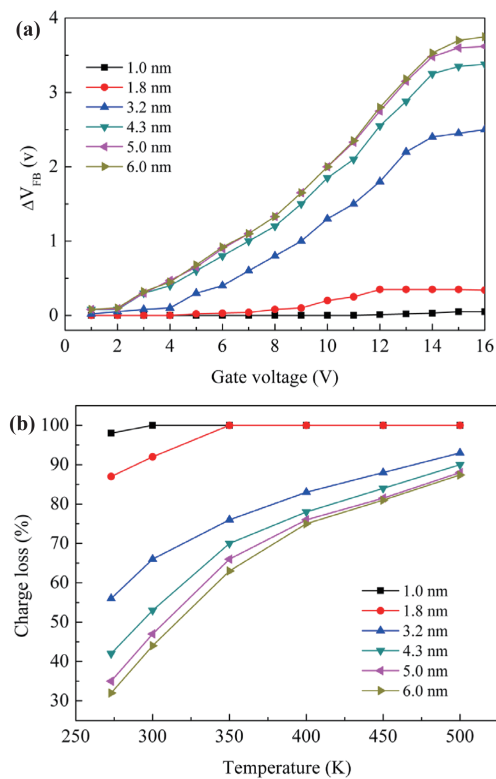

Fig. 5. (a) The VFB shift under different program voltages at 0.1 ms for MANOS capacitors with varying Si_3N_4 thickness and (b) dependence of electron loss on temperature for MANOS capacitors.

the larger the increase, indicating that T-B tunneling becomes more and more difficult, especially for those deep E_T. Moreover, the electron loss path starts to change with increasing, and T-E gradually becomes the important electron loss mechanism from shallow E_T to deep E_T. It is worth noting that there is little effect of T-B tunneling on electron retention when x>4 nm. It was also found that $\tau_{T\text{-}E}$ decrease by several orders of magnitude when increasing the temperature, and more and more trapped electrons tend to be de-trapping through T-E, which is the dominant electron loss mechanism when the temperature exceeds 470 K. This means that the dominant region of T-B will gradually reduce to disappear with an increase of temperature from 273 to 500 K. Fig. 3(b) exhibits the tunneling distance of different E_T in the retention state based on Eq. (3). It was observed that x decreases with E_T increasing from 0.5 to 1.3 eV at the same retention time, indicating that the electrons trapped at deep E_T are less affected by T-B tunneling.

Figure 4 illustrates how the two electron loss processes influences the retention state for MANOS devices. Ⅰ and Ⅱ represent the T-B and T-E dominant region at 273 K, respectively, and the boundary (marked by) is drawn on the basis of the above results. At a retention time t (e.g., 1,000 s), region Ⅰ and Ⅱ should contain empty traps and filled traps. As the electron loss process continues, the empty-filled traps boundary marked by $B_{T\text{-}B}$ and $B_{T\text{-}E}$ moves toward the BO side and the bottom of the Si_3N_4 band gap, correspondingly. The boundary of $B_{I/II}$, which is nonlinear with tunneling distance, moves down at elevated temperatures, suggesting that T-E gradually dominates the electron loss process.

The memory window $\triangle V_{FB}$ (flat-band voltage shift) extracted from the 1 MHz capacitance-voltage (C-V) curve under different program voltages is shown in Fig. 5(a). In the thickness range of our study, much smaller V_{FB} of MANOS devices with an Si_3N_4 layer less than 3.2 nm are observed, indicating that injected electrons are not trapped effectively but are lost quickly. Though the program speed and memory window increase with a thick Si_3N_4 layer, the $\triangle V_{FB}$ appears to be fairly similar when the thickness exceeds 4.3 nm. This result is ascribed to the reduced electric field through Si_3N_4 due to the increasing Si_3N_4 thickness, which gives rise to a decrease of electron trapping efficiency. The retention characteristics of the samples after 10 hours at different temperatures are shown in Fig. 5(b). It shows that high charge loss is observable for thin Si_3N_4 less than 3.2 nm even at 273 K. As illustrated in Fig. 3(a), the T-B tunneling dominates the electron loss process for thinner Si_3N_4 due to the small $\tau_{T\text{-}B}$, and those trapped electrons near the TO/Si_3N_4 interface are lost quickly

through the TO to the substrate. By increasing the thickness of Si_3N_4, the retention characteristics can be improved. However, at and above 4.3 nm, the charge loss is almost independent of Si_3N_4 thickness, especially for temperatures exceeding 470 K. These results can be attributed to the electron loss mechanisms transition between T-B and T-E, as illustrated in Fig.4. When T-E dominates the electron loss process, the retention characteristics are not affected by the gradual increase of Si_3N_4 thickness. Hence, in the thickness range of our study, we deduce that a Si_3N_4 thickness of more than 6 or less than 4.3 nm has no contribution to improving the memory performance.

4. CONCLUSIONS

In summary, we investigated the effect of nitride thickness, temperature and trap energy levels on the electrons loss behavior of a $Pt/Al_2O_3/Si_3N_4/SiO_2/Si$ CTF memory structure. In a data retention state, T-B and T-E tunneling compete with each other to influence the retention characteristics, even at 273 K. Those trapped electrons near TO (<1 nm) and at a shallow E_T (<0.5 eV) inside the Si_3N_4 are lost quickly via T-B and T-E tunneling, respectively. With an increase of Si_3N_4 thickness and temperature, T-B tunneling is gradually reduced, while T-E dominates the electrons loss process. At a certain E_T, electrons may adopt different loss paths, which depend on the Si_3N_4 thickness and temperature. The electrical measurement results demonstrate that a thin Si_3N_4 layer of less than 3.2 nm has no effective trapping ability. Though the storage performance can be improved by increasing Si_3N_4 thickness, the data retention characteristics are almost independent of nitride thickness at elevated temperatures, especially temperatures exceeding 470 K. The above results can pave a way for device design in the future.

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