

# A Canonical Small-Signal Linearized Model and a Performance Evaluation of the SRF-PLL in Three Phase Grid Inverter System

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## Abstract

Phase-locked loops (PLL) based on the synchronous reference frame (SRF-PLL) have recently become the most widely-used for grid synchronization in three phase grid-connected inverters. However, it is difficult to study their performance since they are nonlinear systems. To estimate the performances of a SRF-PLL, a canonical small-signal linearized model has been developed in this paper. Based on the proposed model, several significant specifications of a SRF-PLL, such as the capture time, capture range, bandwidth, the product of capture time and bandwidth, and steady-state error have been investigated. Finally, a noise model of a SRF-PLL has been put forward to analyze the noise rejection ability by computing the SNR (signal-to-noise ratio) of a SRF-PLL. Several simulation and experimental results have been provided to verify and validate the obtained conclusions. Although the proposed model and analysis method are based on a SRF-PLL, they are also suitable for analyzing other types of PLLs.

**Key words:** Noise model, Noise rejection ability, Performance evaluation, Small-signal linearized model, SRF-PLL

## I. INTRODUCTION

A grid-connected inverter perfectly matches the philosophy of a phase-locked loop (PLL), since it should operate in harmony with the utility voltage. It should phase-lock its internal oscillator to the positive sequence voltage at the fundamental frequency in three phase systems to produce an amplitude and phase-coherent utility voltage that is applied to control grid-connected inverters or micro-grid inverters, such as distributed generation and storage systems, flexible ac transmission systems (FACTS), power line conditioners and uninterruptible power supplies (UPS) [1], [2]. Regardless of the detection approach used, it should work as quickly and accurately as possible, even if the utility voltage is distorted and unbalanced.

There are three main detection approaches in the literature. They are the zero-cross phase detection method, the

stationary reference frame phase detection method, and the synchronous reference frame phase detection method [3]. A conventional grid-connected inverter offers a low degree of control and is synchronized to the utility by detecting the zero-crossing of the utility voltage. This assumes that the magnitude of the utility is well known and that the frequency is kept constant. This technique suffers from some drawbacks, such as inaccuracy and the detection of multiple zero-crossings in the case of a distorted grid voltage. To overcome these drawbacks, some modified methods based on comparators circuits with dynamic hysteresis [4], curve-filters [5] or predictive digital filtering algorithms [6] have been proposed. Since these methods employ a comparator as phase detector (PD) for detecting changes in the polarity of the grid voltage, the phase sensitivity should be  $U_g/\pi$  for a single phase system, and  $3U_g/\pi$  for three phase voltages, where  $U_g$  is the phase magnitude of the utility voltage. A PI controller is used as a loop filter. More importantly, it has a small-signal linearized model that is identical to that of the conventional SRF-PLL.

The most popular and essential technique is a three-phase locked loop based on the synchronous reference frame [7].

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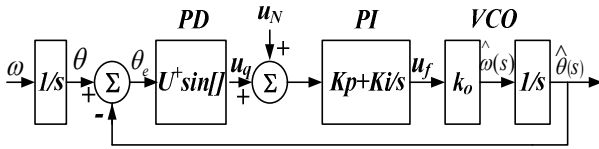


Fig. 2. Simplified model of SRF-PLL.

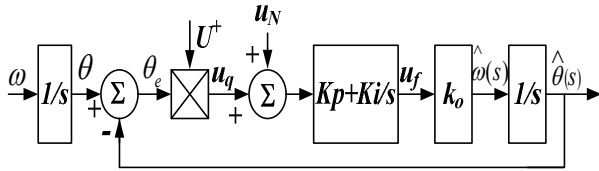


Fig. 3. Small-signal linearized model of SRF-PLL.

$$\sin(\theta - \hat{\theta}) \approx \theta - \hat{\theta} \quad (3)$$

where  $|\theta - \hat{\theta}| \leq \frac{\pi}{6}$ .

Therefore, when the PLL is locked or tends to lock, a small-signal linearized model of the PD can be given by:

$$u_q = U^+ \sin \theta_e \approx U^+ (\theta - \hat{\theta}) \quad (4)$$

Thus, a small-signal linearized model of the SRF-PLL is proposed, as depicted in Fig. 3.

Based on the proposed small-signal linearized model of the SRF-PLL, some typical transfer functions of the SRF-PLL can be derived as follows.

The open-loop transfer function of the SRF-PLL is

$$T(s) = \frac{\hat{\theta}(s)}{\theta_e(s)} = U^+ \frac{(k_p s + k_i)}{s^2} \quad (5)$$

The closed-loop transfer function of the SRF-PLL is

$$H_\theta(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{U^+ k_p s + U^+ k_i}{s^2 + U^+ k_p s + U^+ k_i} \quad (6)$$

The input-to-error transfer function of the SRF-PLL is

$$E_\theta(s) = \frac{\theta_e(s)}{\theta(s)} = \frac{s^2}{s^2 + U^+ k_p s + U^+ k_i} \quad (7)$$

The noise-to-error transfer function the SRF-PLL is

$$E_u(s) = \frac{\theta_e(s)}{u_N(s)} = \frac{k_p s + k_i}{s^2 + U^+ k_p s + U^+ k_i} \quad (8)$$

### B. Stability Consideration

The open-loop transfer function, Eq. (5), can be rewritten as:

$$\frac{\hat{\theta}(s)}{\theta_e(s)} = T(s) = U^+ k_i \frac{(s / \omega_z + 1)}{s^2} \quad (9)$$

where  $\omega_z = \frac{k_i}{k_p}$ .

The substitution of  $s=j\omega$  into Eq. (9) yields the frequency response. Fig. 4 illustrates a Bode plot of the magnitude frequency response of  $T(s)$ .

In Fig. 4, let the crossover frequency  $f_c$  be  $f_z$  so that the phase margin is about 45 degrees. Using the identity  $f_c=f_z$  yields:

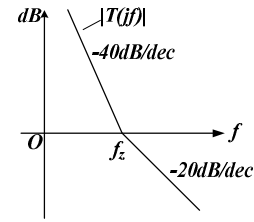


Fig. 4. Magnitude frequency response of  $T(s)$ .

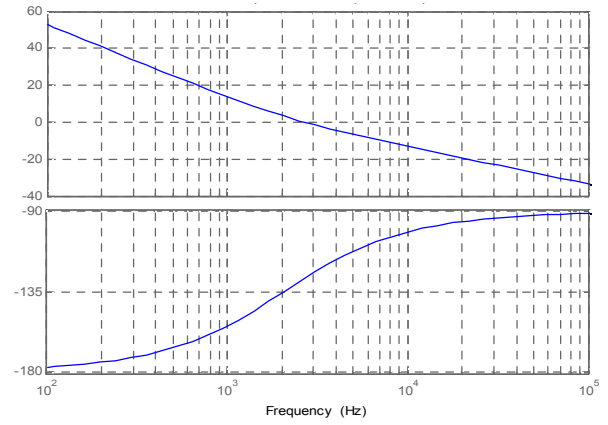


Fig. 5. The simulation results of the frequency response  $T(s)$ , the parameters are:  $U^+=466.62$ ,  $f_c=2.7\text{kHz}$ ,  $k_p=28.277$  and  $k_i=3.73*10^3$ .

$$k_i = \frac{4\pi^2 f_c^2}{U^+} \quad (10)$$

$$k_p = \frac{k_i}{\omega_z}$$

The substitution of  $U^+=466.62$  and  $f_c=2.7\text{kHz}$  yields  $k_p=28.277$  and  $k_i=3.73*10^3$ . The simulation results are demonstrated in Fig. 5. It can be seen that the crossover frequency is about 2.71kHz and that the phase margin is about 53 degree to ensure stability and a fast dynamic response.

### III. PERFORMANCE ANALYSIS OF THE SRF-PLL

The performance of the SRF-PLL is estimated in this section, including the capture time, the capture range, and the steady-state error.

#### A. Capture Time of SRF-PLL

The normalized transfer function of (6) can be rewritten as:

$$H_\theta = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (11)$$

where  $\omega_n^2 = U^+ k_i$ ,  $\zeta = \frac{1}{2} \sqrt{U^+ k_p / \omega_z}$ ,  $\omega_z = \frac{k_i}{k_p}$ .

By ignoring the LHP (left half plane) zero in Eq. (11), it can be approximated by a standard second order transfer

$$\text{function } \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}.$$

The dynamic analysis of a standard second-order system

has been studied in many textbooks. The following approximated formulas are present in reference [9]. The settling time  $t_s$  can be calculated by the formula in [10],

$$t_s = 4.6\tau \quad (12)$$

where  $\tau = 1/\zeta\omega_n$ .

It is noted that the settling time is usually called the capture time in a PLL.

According to the parameters  $k_f=3.73 \times 10^3$  and  $k_p=28.277$  in Section II, the damping factor, natural frequency and capture time can be calculated, yielding  $\omega_n=1.139 \times 10^4$  rad/s,  $\zeta=0.5$  and  $t_s=0.8$ ms, respectively.

The bandwidth of the PLL is:

$$\omega_{-3dB} = \omega_n \sqrt{1-2\zeta^2 + \sqrt{(1-2\zeta^2)^2 + 1}} \quad (13)$$

For  $\zeta = 0.7$ , the  $\omega_{-3dB}$  is:

$$\omega_{-3dB} = 2.06\omega_n \quad (14)$$

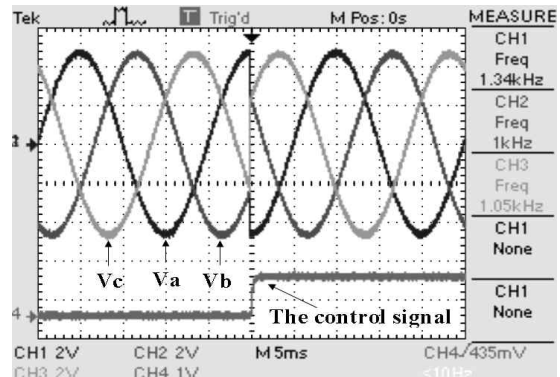
According to Eq. (12), Eq. (13) and Eq. (14), an important formula can be derived that the product of the capture time  $t_s$  and the bandwidth  $\omega_{-3dB}$  is constant, and the value of the product is  $\omega_{-3dB}t_s \approx 2.3$  under the condition of  $\zeta=0.7$  and a 1% steady-state error for the step response. In other words, the capture time  $t_s$  is inversely proportional to the bandwidth  $\omega_{-3dB}$ .

Experimental results are shown in Fig. 6. In Fig. 6(a), CH1, CH2 and CH3 are the three-phase utility voltages, and CH4 is a control signal. The phase of the utility voltage jumps forward 180 degree while the control signal CH4 has a step change at a triggering time point. In Fig. 6(b), CH1 is the estimated output phase  $\hat{\theta}$  of the SRF-PLL, and CH2 is the control signal. The vicinity waveforms of Fig. 6(b) at the triggering time point are enlarged as illustrated in Fig. 6(c) to measure the capture time,  $t_s \approx 1$ ms. The steady-state error  $\theta_e$  is denoted by CH1 shown in Fig. 6(d).

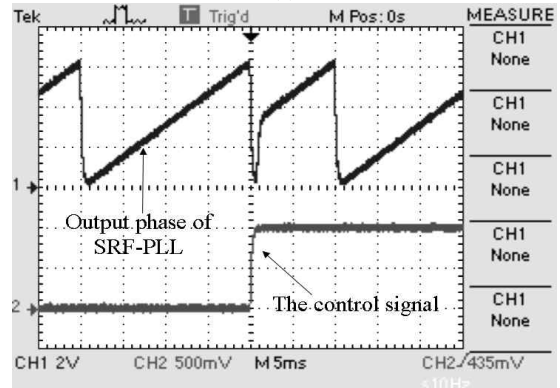
Note that the capture time displays a considerable error between the theoretical result  $t_s=0.8$ ms from Eq. (12) and the experimental result  $t_s=1$ ms. Therefore, the expression result from Eq. (12) should be taken only as a guide rather than precise formula. This formula provides a rough estimate of the time response of the system since the time taken by the coordinate transformation in the SRF-PLL and the influence of the ignored zero  $-\frac{\omega_n}{2\xi}$  of Eq. (11) are not yet considered in this formula [11]. This should be checked, usually by simulation, in order to verify whether the time specification has been properly met or not.

### B. Capture Range of SRF-PLL

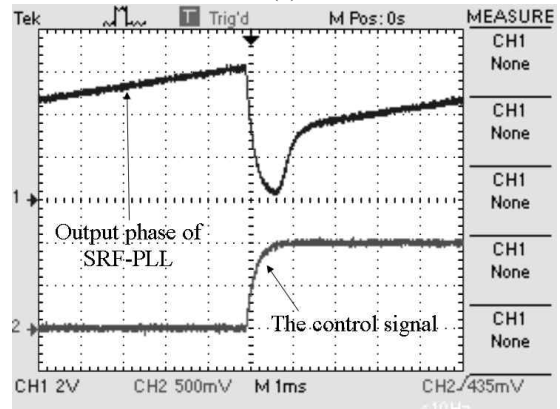
Another significant parameter of the PLL, called the capture range  $\Delta\omega_H$ , is the frequency range at which a PLL is able to keep statically phase-locked. This parameter can be calculated by:



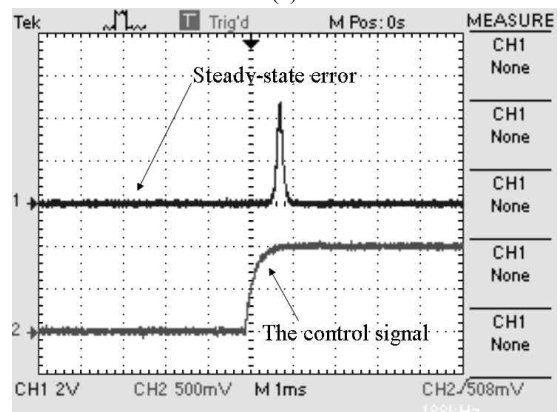
(a)



(b)



(c)



(d)

Fig. 6. Experimental waveforms of SRF-PLL when phase jumps. (a) Three-phase utility voltage. (b) Estimated phase of SRF-PLL. (c) Enlarged waveform of (b), (d) steady-state error.

$$\Delta\omega_H = U^+ F(0) = \infty \text{ for PI controller} \quad (15)$$

where  $F(0)$  is the DC gain of the controller in Fig. 3.

If a PI controller is selected, the capture range  $\Delta\omega_H$  is infinite because PI controller has an infinite DC gain. Therefore, the capture range  $\Delta\omega_H$  is only limited by the maximum value of the integrator output. An infinite capture range implies that the PLL has no ability to reject any noise since it can lock all of the frequency signals. Therefore, a PI controller is not a good choice to suppress the noise present in a PLL.

### C. Steady-state Error of the SRF-PLL

In this section it is investigated how the PLL responds under various conditions: phase step, frequency step, frequency ramp, and magnitude step as well as magnitude ramp.

In practice, when a PLL is used for synchronization with the grid voltage in a grid-connected inverter, and a set of micro-grid inverters working in the island condition by employing the frequency droop control strategy [12]. The phase step, frequency step and ramp of the PCC voltage are always encountered. Moreover, the magnitude step and ramp always occur when the inverter is controlled to ride through the grid fault [13].

1) *Case 1, Steady-state error in the case of variations in the phase and frequency of utility voltage:* By applying Eq. (7), the steady-state error of the SRF-PLL can be expressed as:

$$\begin{aligned} & \lim_{t \rightarrow \infty} e_\theta(t) \\ &= \lim_{s \rightarrow 0} s \theta_e(s) = \lim_{s \rightarrow 0} s E_\theta(s) \theta(s) \quad (16) \\ &= \lim_{s \rightarrow 0} s \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \theta(s) \end{aligned}$$

If a phase step is applied to the utility voltage as a reference signal, then  $\theta(s)=1/s$  and:

$$\lim_{t \rightarrow \infty} e_\theta(t) = 0 \quad (17)$$

This conclusion has already been proved in Fig. 6(d).

Similarly, since  $\theta(s)=\omega(s)/s$ , the steady state error formula of the frequency variation applied to a reference input gives:

$$\begin{aligned} & \lim_{t \rightarrow \infty} e_\omega(t) \\ &= \lim_{s \rightarrow 0} s \theta_e(s) / s = \lim_{s \rightarrow 0} E_\theta(s) \omega(s) \quad (18) \\ &= \lim_{s \rightarrow 0} \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \omega(s) \end{aligned}$$

If a frequency step of the utility voltage is used as an input, then  $\omega(s)=1/s$  and:

$$\lim_{t \rightarrow \infty} e_\omega(t) = 0 \quad (19)$$

If a frequency ramp of the utility voltage acts on the input, then  $\omega(s)=1/s^2$  and:

$$\lim_{t \rightarrow \infty} e_\omega(t) = 1/\omega_n^2 \quad (20)$$

The open-loop transfer function of (5) shows that this PLL

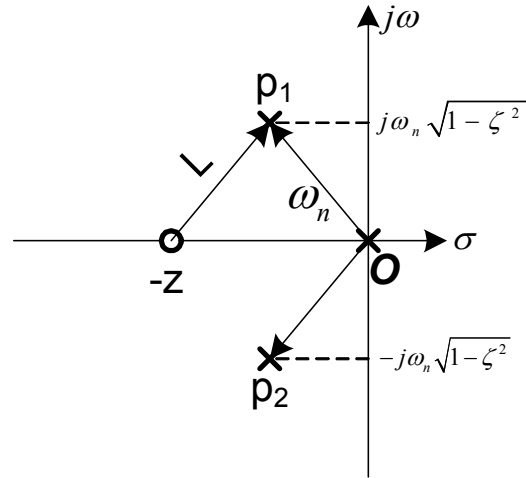


Fig. 7. Diagrams of the poles and zeros location of the closed-loop transfer function  $H_\omega$ .

is a type II system, with two poles at the origin. This means that it is able to track the utility voltage phase step, frequency step and phase ramp (change slowly in a constant slop) without any steady-state errors.

Moreover, the normalized closed-loop transfer function from  $\omega$  to  $\theta$ , shown in Fig. 3, can be written as:

$$H_\omega = \frac{\omega_n^2 (s + z)}{zs(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (21)$$

Compared with the expression of  $H_\theta$ , as shown in Eq. (11), a pole at the origin is added in  $H_\omega$ . A diagram of the poles and zeros location of the closed-loop transfer function  $H_\omega$  is illustrated in Fig. 7.

As show in Fig. 7, the dominant pole is at the origin, rather than the pair of complex poles,  $p_1$  and  $p_2$ . Thus, the system presents first-order system features so that its dynamic performance is not as good as the pervious closed system defined by Eq. (12). Experimental results are shown in Fig. 8. In Fig. 8(a),  $CH1$ ,  $CH2$  and  $CH3$  are three-phase utility voltages, and  $CH4$  is a control signal. A frequency jump of the utility voltage occurs from 50Hz to 60Hz, while the control signal of  $CH4$  has a step change at a triggering time point. In Fig. 8(b),  $CH1$  shows a steady-state error for the SRF-PLL. It can be observed that its steady-state error is zero, but the capture time  $t_s$  is about 25ms.

In addition, a constant steady state error should exist in a conventional SRF-PLL when it is used in a set of micro-grid inverters working in the isolation island condition by adopting the frequency droop control strategy.

2) *Case 2, steady-state error analysis of the magnitude variation of the utility voltage applied to an input signal:* When the magnitude of the utility voltage fluctuates, and the phase is kept constant, the equivalent model is shown in Fig. 9. There are two parts in this model. One is the linear

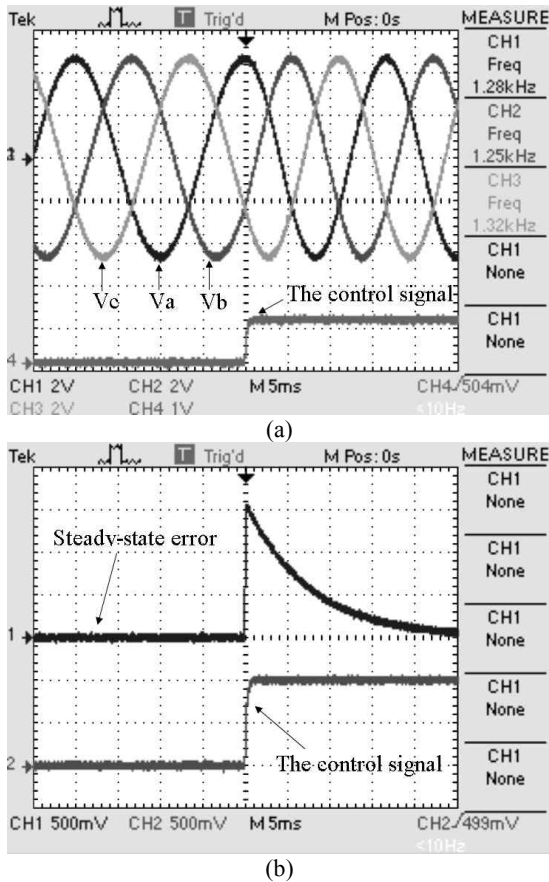


Fig. 8. Experimental waveforms of SRF-PLL when frequency jumps. (a) Utility voltage. (b) Waveform of steady-state error.

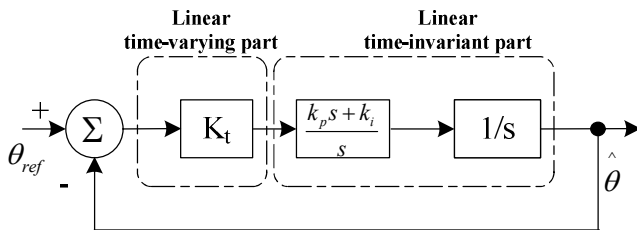


Fig. 9. The equivalent model when the magnitude of the utility voltage fluctuates, and phase is kept constant.

time-varying part, and the other is the linear time-invariant part. The system performance of the magnitude variation is analyzed in the Bode diagram shown in Fig. 10. The nonlinear system is analyzed by using the method of describing function.

When the magnitude of the utility voltage is normal,  $k_t$  is equal to  $k_{t1}$ . When the magnitude of the utility voltage drops at time= $t_2$ , the gain  $k_t$  is equal to  $k_{t2}$ , and the amplitude frequency response curve moves downward. However, the phase frequency response curve remains unchanged.

In summary, as shown in Fig. 10, when the magnitude of the utility voltage drops, the gain-crossover frequency and phase margin decrease, but the system remains stable for the PI controller. Variations in the magnitude have no effect on the steady-state error.

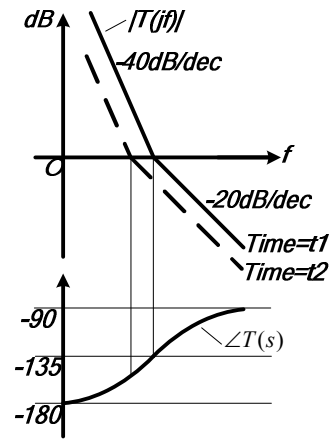


Fig. 10. The Bode diagram when the amplitude of the utility voltage fluctuates.

Experimental results are shown in Fig. 11 and Fig. 12. In Fig. 11(a), *Ch1*, *Ch2* and *CH3*, are three-phase utility voltages, and *CH4* is a control signal. The amplitude of the utility voltage drops from 466V to 233V while the control signal steps. As shown in Fig. 11(b), *CH1* displays the steady-state error for the SRF-PLL, and *CH2* is a control signal. It can be seen that the magnitude step has no effect on the steady-state error.

As shown in Fig. 12(a), the amplitude ramp of the utility voltage is applied, and Fig. 12(b) shows that the amplitude ramp has no effect on the steady-state error.

It can be seen from the above analysis that if the amplitude of the utility voltage fluctuates, the conventional SRF-PLL has no steady-state error. It only decreases the crossover frequency and phase margin of the system.

The performance of the conventional SRF-PLL has been summarized and listed in Table I.

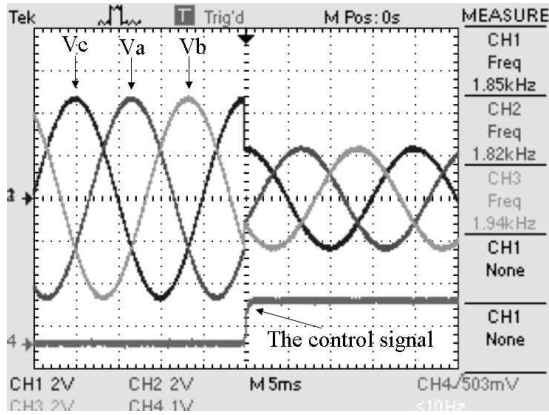
#### IV. PERFORMANCE IN THE PRESENCE OF NOISE

Noise is an extremely important issue when a PLL is employed to detect the fundamental component of the positive-sequence voltage in the control systems of grid-connected inverters or micro-grid inverters.

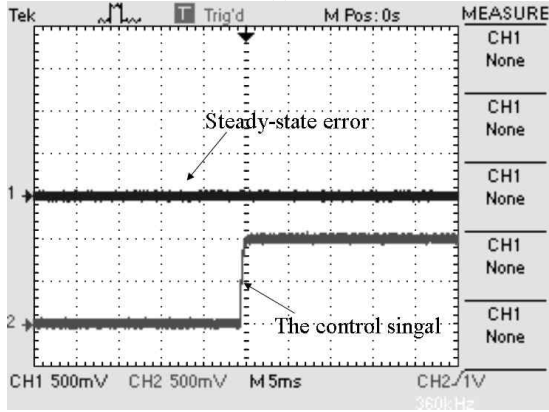
##### A. Noise Model of SRF-PLL

If the utility is unbalanced and its output voltage contains some high order harmonics, such as the 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup>..., then the voltage vector expression in the  $dq$  plane in Eq.(1) may be modified as follows:

$$\begin{aligned} \mathbf{u}_{dq}^N &= \begin{bmatrix} u_d^N \\ u_q^N \end{bmatrix} = U^+ \begin{bmatrix} \cos[\omega_0 t - \hat{\theta}] \\ \sin[\omega_0 t - \hat{\theta}] \end{bmatrix} \\ &+ \sum_{n=2}^{\infty} U_{2n-1}^+ \begin{bmatrix} \cos[(2n-1)\omega_0 t - \hat{\theta}] \\ \sin[(2n-1)\omega_0 t - \hat{\theta}] \end{bmatrix} \\ &+ \sum_{n=1}^{\infty} U_{2n-1}^- \begin{bmatrix} \cos[-(2n-1)\omega_0 t - \hat{\theta}] \\ \sin[-(2n-1)\omega_0 t - \hat{\theta}] \end{bmatrix} \end{aligned} \quad (22)$$



(a)



(b)

Fig. 11. Experimental waveforms of SRF-PLL when a amplitude step of the utility voltage is applied. (a) Utility voltage. (b) Waveform of steady-state error.

The formula of (22) can be rewritten in the following compact form:

$$u_q^N = U_q + U_N \quad (23)$$

where

$$U_q = U^+ \sin[\omega_0 t - \hat{\theta}]$$

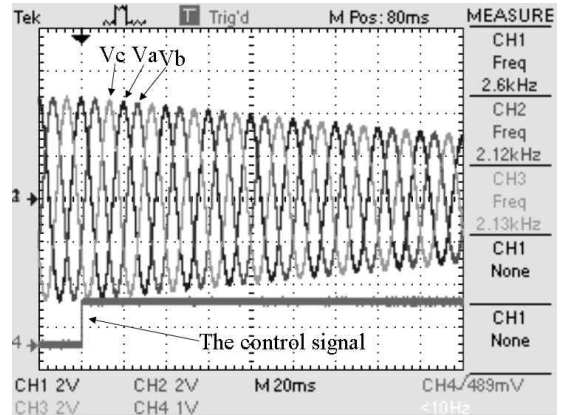
$$U_N = \sum_{n=2}^{\infty} U_{2n-1}^+ \sin[(2n-1)\omega_0 t - \hat{\theta}] + \sum_{n=1}^{\infty} U_{2n-1}^- \sin(-(2n-1)\omega_0 t - \hat{\theta})$$

Assuming that the positive-sequence component is locked in the steady state, and then the formula of (22) becomes:

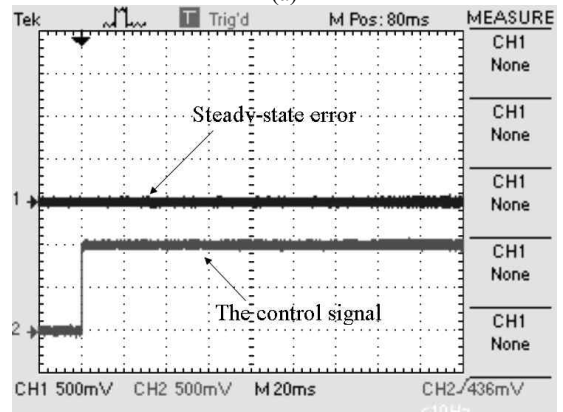
$$\begin{aligned} u_{dq}^N &= \begin{bmatrix} u_d^N \\ u_q^N \end{bmatrix} = U^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} \\ &+ \sum_{n=2}^{\infty} U_{2n-1}^+ \begin{bmatrix} \cos 2(n-1)\omega_0 t \\ \sin 2(n-1)\omega_0 t \end{bmatrix} \\ &+ \sum_{n=1}^{\infty} U_{2n-1}^- \begin{bmatrix} \cos 2n\omega_0 t \\ -\sin 2n\omega_0 t \end{bmatrix} \end{aligned} \quad (24)$$

The first term of Eq. (24) is the fundamental component of the positive-voltage, the summation term is the high order harmonic components and the third is the negative-voltage component.

The  $q$  component of Eq. (24) can be expressed as:



(a)



(b)

Fig. 12. Experimental waveforms of SRF-PLL a amplitude ramp of utility voltage is applied. (a) Utility voltage. (b) Waveform of steady-state error.

$$u_q^N(t) \approx \sum_{n=2}^{\infty} U_{2n-1}^+ \sin 2(n-1)\omega_0 t - \sum_{n=1}^{\infty} U_{2n-1}^- \sin 2n\omega_0 t = U_N \quad (25)$$

Hence, the noise source is represented by  $U_N$ , as illustrated in Fig. 1.

The small-signal linearized model of the SRF-PLL, shown in Fig. 3, can be modified to achieve the noise model of the SRF-PLL, shown in Fig. 13. Here,  $k_o$  is the sensitivity of the voltage-controlled frequency oscillator (VCO), and it is equal to 1.

### B. Noise Performance

By applying the Mason formula to the block diagram of the noise model shown in Fig. 13, the input-to-output transfer function  $H_N(s)$  is given by:

$$H_N(s) = \frac{U_{eN}(s)}{U_N(s)} = \frac{1}{U^+ k_o} \times \frac{s(s/Q+1)}{(s/\omega_n)^2 + s/\omega_n Q + 1} \quad (26)$$

where  $\omega_n^2 = U^+ k_i$ ,  $\zeta = \sqrt{U^+ k_p / 4k_i}$ ,  $Q = 1/2\zeta$ .

If a PI controller is used, and the parameters are:  $U^+ = 466.62$ ,  $k_p = 28.277$  and  $k_i = 3.73 \cdot 10^3$ , frequency response of  $H_N(s)$  is depicted in Fig. 14.

The following conclusions can be drawn from Fig. 14. The frequency response of  $H_N(s)$  exhibits a high-pass characteristic

TABLE I  
THE PERFORMANCE OF CONVENTIONAL SRF-PLL

title	Formula
normalized second-order closed-loop transfer function	$H_\theta = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$
natural frequency and damping factor	$\omega_n^2 = U^+ k_i, \quad \zeta = \sqrt{U^+ k_p / \omega_z} / 2$
capture time	$t_s = 4.6 / \zeta\omega_n$
-3dB bandwidth	$\omega_{-3dB} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2)^2 + 1}}$ $\omega_{-3dB} = 2.06\omega_n, \text{ for } \zeta = 0.7$
product of capture time and bandwidth	$\omega_{-3dB} t_s \approx 2.3, \text{ for } \zeta = 0.7$
capture range	$\Delta\omega_H = \infty$ for PI Controller
steady-state error	
phase step	$\lim_{t \rightarrow \infty} e_\theta(t) = 0$
frequency step	$\lim_{t \rightarrow \infty} e_\omega(t) = 0$
frequency ramp	$\lim_{t \rightarrow \infty} e_\omega(t) = 1 / \omega_n^2$
amplitude step	$\lim_{t \rightarrow \infty} e_u(t) = 0$
amplitude ramp	$\lim_{t \rightarrow \infty} e_u(t) = 0$

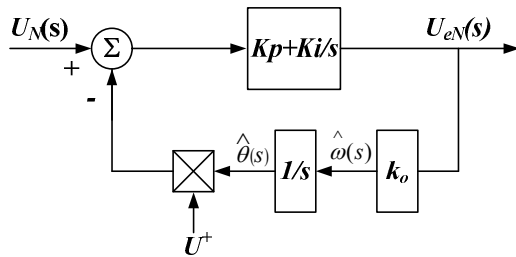


Fig. 13. Noise model of SRF-PLL.

with a cutoff frequency  $f_c = \sqrt{U^+ \frac{k_i}{k_p}}$ . The cutoff frequency  $f_c$

is smaller than the grid frequency  $f_o$ . In other words, according to Eq. (25), the all components of  $U_N$  can pass through the controller directly without any attenuation and reach to the input terminal of the VCO. Therefore, the SRF-PLL does not have the ability to reject noise.

Usually, a low-pass filter is included in the loop to alleviate noise as shown in Fig. 15. Since  $1/T_L \ll 2\omega_o$  is satisfied, and the noise cannot reach the terminal of the VCO, the SRF-PLL has the ability to reject noise.

The open-loop transfer function  $T(s)$  is modified as:

$$T(s) = U^+ k_i \frac{(s/\omega_z + 1)}{s^2 (s/\omega_p + 1)}, \omega_z = \frac{k_i}{k_p}, \omega_p = \frac{1}{T_L} \quad (27)$$

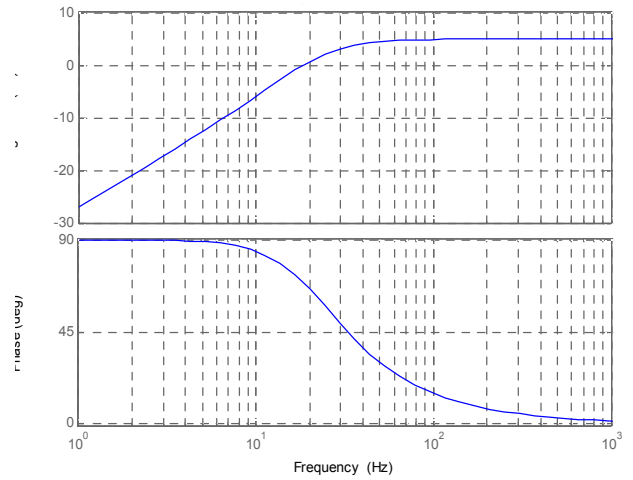


Fig. 14. Frequency response of the noise transfer function  $H_N(s)$ , the parameters are:  $U^+=466.62$ ,  $f_c=2.7\text{kHz}$ ,  $k_p=28.277$  and  $k_i=3.73 \cdot 10^3$ .

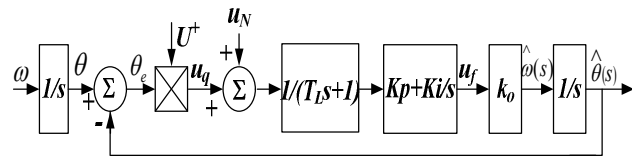


Fig. 15. Small-signal linearized model of SRF-PLL with low-pass filter.

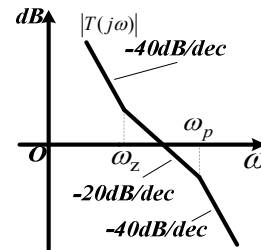


Fig. 16. The bode diagram of the open-loop transfer function  $T(s)$  of SRF-PLL with low pass filter.

The zero of the PI controller  $\omega_z$  should be selected to be lower than  $\omega_p$ , and the amplitude frequency response of  $T(s)$  can be plotted, as shown in Fig. 16. The phase margin is determined by the middle-frequency-band of  $(\omega_p - \omega_z)$ . Usually, let  $\omega_p / \omega_z \approx 5-10$  so that the phase margin is about 30-60 degrees, and the crossover frequency is equal to  $\omega_p / 3$ .

A low-pass filter is added into the loop to alleviate noise. However, the above analysis indicated that the crossover frequency is rather low, and the fast dynamic response is not satisfied.

Fig. 17 shows a simulation result using MATLAB with the following parameters:  $\omega_p = 314\text{rad/s}$ ,  $\omega_z = 40\text{rad/s}$ , and  $\omega_p / \omega_z = 7.8$ . The simulation result demonstrates that the



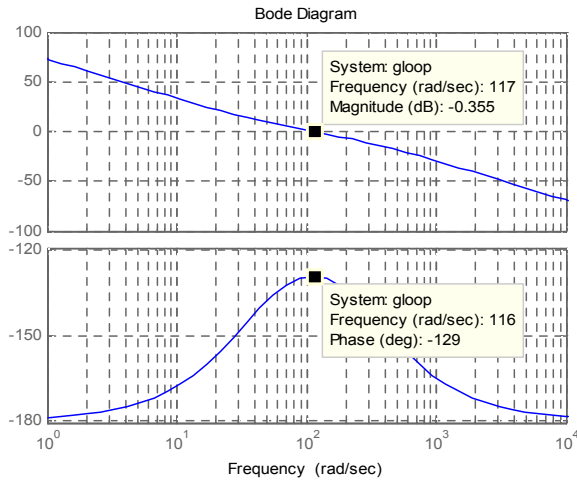


Fig. 17. Frequency response of the open-loop transfer function  $T(s)$  of SRF-PLL with low pass filter.

crossover frequency is only 18Hz, and phase margin is about 50 degrees.

The experimental results are shown in Fig. 18. In Fig. 18(a), CH1, CH2 and CH3, are three-phase utility voltage, and CH4 is a control signal. A phase step of 180 degrees is applied, and a 3<sup>th</sup> harmonic component with a value of five percent is injected into the grid. As shown in Fig. 18(b), CH1 and CH2 represent the input and output signals of the low-pass filter. This shows that the harmonic component is eliminated with the low-pass filter, but the capture time  $t_s$  is about 50ms. In sum, the ability to suppress noise and the dynamic response are mutually contradictory for the SRF-PLL.

C. SNR (signal-to-noise ratio) of the SRF-PLL

Based on the noise model of the SRF-PLL shown in Fig. 13 and Eq. (26), the input noise voltage of the VCO is given by:

$$U_{eN}(s) = H_N(s)U_N(s) = \frac{1}{U^+k_o} \times \frac{s(s/Q+1)}{(s/\omega_n)^2 + s/\omega_nQ + 1} U_N(s) \quad (28)$$

Eq. (25) shows that the noise contains two parts: unbalance noise and high harmonic noise. For grid-connected inverters, unbalance noise is dominant. However, the high order harmonic noises should be considered for micro-grid inverters.

1) Case 1, SNR for unbalance noise: For grid-connected inverters, unbalanced noise is dominant. Therefore, Eq. (28) is employed to compute the unbalance noise response, such as:

$$U_{eN}(jf)|_{f=2f_o} = \frac{1}{U^+k_o} \times \frac{j2f_o(j2f_o/Q+1)}{1-(2f_o/f_n)^2 + j2f_o/f_nQ} \times U_N(j2f_o) \quad (29)$$

It can be seen from Fig. 14 that the amplitude is 4.88dB, and the phase is 14 degree at  $f=100$ Hz. If the noise voltage is  $U_N(t) = U_N \sin(2\omega t)$ , the input voltage of the VCO is:

$$U_{eN}(t) = 1.75U_N \sin(2\omega t + 14^\circ) = U_{NB} \sin(2\omega t + 14^\circ) \quad (30)$$

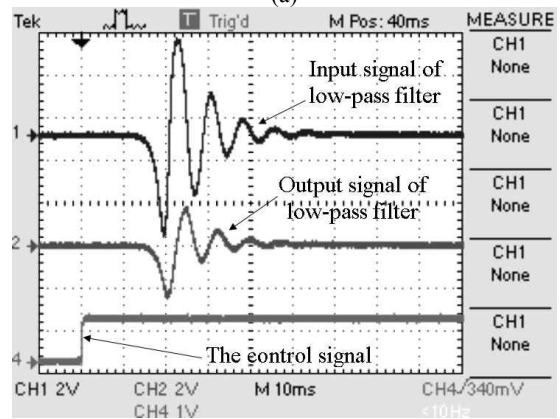
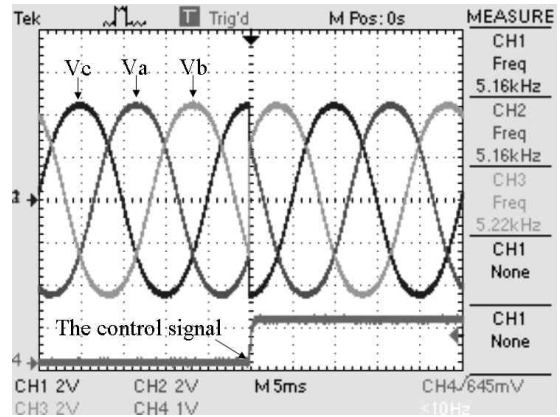


Fig. 18. Experimental waveform of SRF-PLL with low pass filter when phase step of the three-phase voltage is applied. (a) Utility voltage. (b) Waveform of steady-state error.

The output of the VCO is a constant with value of 50Hz under ideal conditions. If the utility voltage is unbalanced, the output frequency of the VCO is given by:

$$\hat{\omega}(t) = 100\pi + U_{NB} \sin(2\omega t + 14^\circ) \quad (31)$$

Eq. (31) indicates that the output frequency of the PLL becomes a frequency modulation signal instead of a constant frequency, as shown in Fig. 19.

The signal-noise-ratio is defined as:

$$SNR_{UB} = \frac{\text{grid frequency}}{\text{noise magnitude}} = 20 \lg \frac{\omega_o}{U_{NB}} = 20 \lg \frac{100\pi}{|H_N(j200\pi)|U_N} \quad (32)$$

For example, when the parameters are:  $U_N = 0.3U^+$ , the SNR is only  $SNR_{UB} = 2.14dB$ .

It is obvious that the SNR of the SRF-PLL is so low that the output frequency of the SRF-PLL is seriously distorted.

2) Case 2, SNR for high harmonic noise: The grid voltage may be distorted in the case of micro-grids working in the island condition or in weak grids with a high grid impedance because their gridvoltage is prone to notable distorted by

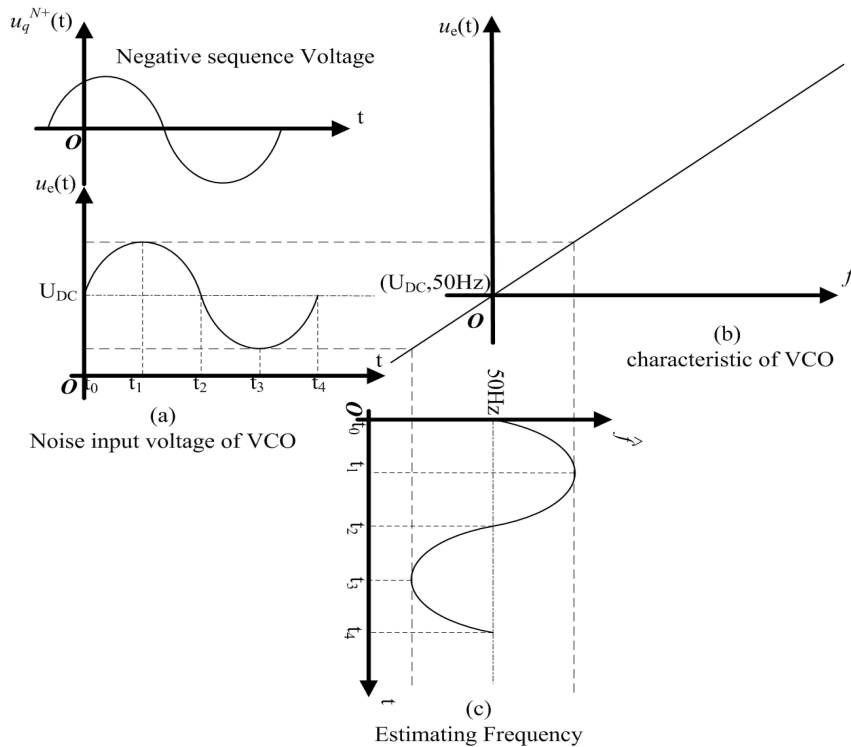


Fig. 19. Estimating frequency waveforms of the PLL by affecting the unbalance noise.

harmonics, switching notches and noise. Therefore, the high-order harmonic noise needs to be considered in this case.

If the noise voltage is defined as:

$$U_N(t) = \sum_{i=2}^{\infty} U_{2n-2}^+ \sin 2(n-1)\omega t$$

The voltage of the input terminal of the VCO is:

$$U_{eN}(t) = 1.75 \sum_{i=2}^{\infty} U_{2n-2}^+ \sin 2(n-1)\omega t \quad (33)$$

The output frequency of the VCO is given by:

$$\hat{\omega}(t) \approx 100\pi + 1.75 \sum_{i=2}^{\infty} U_{2n-2}^+ \sin 2(n-1)\omega t \quad (34)$$

The signal-noise-ratio is defined as:

$$SNR_{UB} = \frac{\text{grid frequency}}{\text{noise magnitude}} = 20 \lg \frac{100\pi}{1.75 \sqrt{\sum_{i=2}^{\infty} (U_{2n-2}^+)^2}} \quad (35)$$

Therefore, the output frequency of the PLL is  $100\pi$  plus the even harmonic components if the utility voltage is distorted.

### V. CONCLUSIONS

It is difficult to investigate the electric characteristics of PLLs because they are nonlinear systems. This results from the coordinate transformation in the control block. In this paper, a canonical small-signal linearized model of the SRF-PLL has been developed to study the following issues: (1) the phase-locked process and operational principle; (2) the

determination of the controller parameters; (3) the performance under various conditions.

By adopting the canonical small-signal linearized model, the following conclusions are obtained:

(1) The SRF-PLL with a PI controller is a normalized second-order system, and several formulas have been supplied in this paper to calculate its significant specifications such as the capture time, the capture rang, the bandwidth, the product of capture time and bandwidth as well as the parameters of the PI controller.

(2) It is revealed by analysis and experiment results that the steady-state error of the SRF-PLL is zero under the conditions of phase step, frequency step, amplitude step and ramp. However, the SRF-PLL has a constant error in case of a frequency ramp.

Noise analysis is also an extremely important issue for the PLL used in the control of grid-connected power inverters or macro grid inverters. In the performance analysis in the presence of noise, the following results and conclusions can be achieved:

(1) A noise model of the SRF-PLL has been proposed to investigate the performance of the SRF-PLL in the presence of noise.

(2) The SRF-PLL is incapable of rejecting noise. However, a low-pass filter in the loop can attenuate the noise at the cost of increasing the capture time.

(3) Two categories of the SNR have also been calculated.

In summary, this paper presents a detailed derivation of small-signal analysis methods to study the SRF-PLL.

Valuable conclusion can be achieved with this method. These conclusions are verified and validated by simulation and experimental results.

Moreover, the conventional SRF-PLL can be commonly used as an essential block in some advanced PLLs, such as DDSRF-PLL [14], IPT-PLL [15], PQ-PLL [15], DSC-PLL [16], [17], DSOAF-PLL [18], FRF-PLL [19] and SSI-PLL [20]. They have a small-signal linearized model that is identical to that of the conventional SRF-PLL. As a result, the proposed model and analysis method are suitable for the other typical PLLs.

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