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Fault-Tolerant Control of Cascaded H-Bridge Converters Using Double Zero-Sequence Voltage Injection and DC Voltage Optimization

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Abstract

Cascaded H-Bridge (CHB) converters can be directly connected to medium-voltage grids without using transformers and they possess the advantages of large capacity and low harmonics. They are significant tools for providing grid connections in large-capacity renewable energy systems. However, the reliability of a grid-connected CHB converter can be seriously influenced by the number of power switching devices that exist in the structure. This paper proposes a fault-tolerant control strategy based on double zero-sequence voltage injection and DC voltage optimization to improve the reliability of star-connected CHB converters after one or more power units have been bypassed. By injecting double zero-sequence voltages into each phase cluster, the DC voltages of the healthy units can be rapidly balanced after the faulty units are bypassed. In addition, optimizing the DC voltage increases the number of faulty units that can be tolerated and improves the reliability of the converter. Simulations and experimental results are shown for a seven-level three-phase CHB converter to validate the efficiency and feasibility of this strategy.

Key words: Cascaded H-bridge converter, DC voltage balancing, DC voltage optimization, Fault-tolerant control, Star connection, Zero-sequence voltage

I. INTRODUCTION

CHB converters have become an important topic of research in the application domain of large-capacity grid connections for renewable energy and large-capacity energy storage systems [1]-[3]. This type of converter can be connected to a medium-voltage grid without using a transformer and can be easily implemented in a modular structure with low switching loss and total harmonic distortion (THD). However, because numerous switches are used in the converter, the failure rate will increase if more cascaded units are added. Therefore, a fault-tolerant control strategy is crucial for improving the reliability of CHB converters after a unit fault [5]-[7].

The two major fault-tolerant processing methods are reconfiguring the topology after a fault and bypassing the unit that includes the faulty switches. References [5], [6] address the scope of the first method. They introduce methods based on carrier-based pulse width modulation (PWM) and space vector modulation (SVM), respectively. These methods improve fault tolerance and expand the output voltage range. However, to determine the fault type of the switch, the switch status must be detected efficiently and precisely. Moreover, an increase in the number of faulty switches would make any reconfiguration more complex and thus difficult to extend. References [7]-[14] introduce different controls based on the second method. Reference [7] only focuses on a single-phase CHB converter. The symmetrical bypassing method introduced in reference [8] bypasses not only the faulty unit but also two healthy units in other phases. This method is easy to implement but demands a high converter redundancy and weakens the fault tolerance. To improve the fault tolerance, references [9]-[14] discuss a "neutral shift" (zero-sequence voltage injection) method for the fault-tolerant control of medium-voltage AC drives. These methods can balance the output line voltages even if the output phase voltages cannot remain balanced after a faulty unit is bypassed. However, these methods assumes

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that the output voltage of each unit is identical without considering the power flow between the phases, making them unsuitable for the fault-tolerant control of grid-connected CHB converters. By injecting the zero-sequence voltage into a battery energy storage system, the method proposed in reference [15] solves the fault-tolerant problem of grid-connected CHB converters with faulty units in a single phase. However, there is an issue in the definition of the current phase that limits its usage for faults in multiple units of different phases. References [16] and [17] apply an interphase DC voltage balance control. However, they do not consider the solution under fault conditions.

This paper summarizes a zero-sequence voltage injection control strategy for DC voltage balancing and fault-tolerance based on a mathematical model of each phase cluster of a CHB converter. This study demonstrates the necessity of optimizing the DC voltage by monitoring the output voltage of a seven-level three-phase CHB converter. It also proposes a fault-tolerant control strategy based on double zero-sequence voltage injection and DC voltage optimization. This strategy can rapidly adjust the interphase power after bypassing a faulty unit and thus balance the DC voltage rapidly. It can also increase the DC voltage reference value when the output voltage of the phase cluster is insufficient to maintain stability and to improve the fault tolerance of the CHB converter. Finally, this strategy is verified through simulations and experimental results.

II. MATHEMATICAL ANALYSIS FOR THE FAULT-TOLERANT CONTROL OF A CHB CONVERTER

A. Topology of a Grid-Connected CHB Converter

Fig. 1 presents the entire configuration of a CHB converter, in which the three-phase clusters with star connections are connected to the power grid by inductors and each phase cluster is connected in series by identical power units. Fig. 2 presents the topology of each power unit. The bypass component applies a bidirectional thyristor to achieve a rapid bypass without considering the fault type of the power unit. The load or power source is connected to the DC side of an H-bridge through an isolated DC/DC component that can provide the necessary isolation with a high-frequency transformer (without this isolated component, a high-voltage isolation should be considered between the loads or power sources to provide isolation of the DC sides of the H-bridges) [18]. The DC/DC converter facilitates the implementation of maximum power point tracking (MPPT) for photovoltaic applications [18] and charging curve fittings for battery storage systems [19].

B. Analysis of Double Zero-Sequence Voltage Injection

If the phase clusters shown in Fig. 1 can only output a positive-sequence voltage within a balanced grid voltage, then the average power of each phase cluster will maintain consistency so that they cannot be adjusted under faulty conditions. The method analyzed in this paper indicates that by injecting double zero-sequence voltages into the output voltage of each phase cluster, the power can be well adjusted, and the interphase DC voltage balance and fault control can be achieved simultaneously.

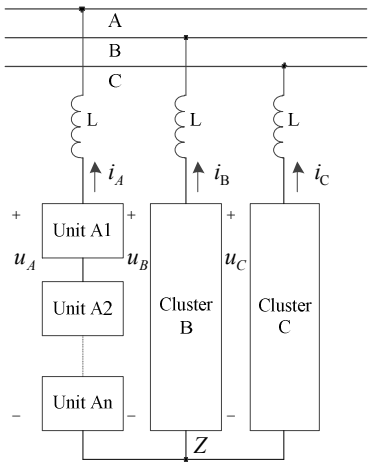


Fig. 1. Configuration of the CHB converter.

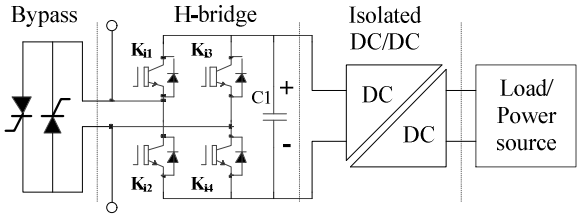


Fig. 2. Topology of the power unit.

Fig. 3 presents a simplified circuit model of a single phase, in which e_s is the phase voltage of a power grid. Because the neutral point of a star connection is ungrounded, injecting a zero-sequence voltage is equivalent to connecting a controlled voltage source u_z to the neutral point Z. The current i_p is only determined by the positive voltage u_p. It is not influenced by the zero-sequence voltage u_z. However, the injected zero-sequence voltage can change the average power of each phase cluster to adjust the interphase power.

According to the switch function S_i, the circuit model of Fig. 3 is represented by the following equation:

$$e_s + L\frac{di_P}{dt} = \sum_{i=1}^{n} S_i u_{dci} - u_Z = u_P , \qquad (1)$$

where u_{dci} is the DC voltage of the i^{th} power unit. S_i of a faulty unit is equal to zero, and S_i of a healthy unit is defined as follows:

$$S_i = K_{i1}K_{i4} - K_{i2}K_{i3} \qquad K \in \{0,1\} \quad , \qquad (2)$$

where K_{i1}~K_{i4} represent the status of the four switches in the H-bridge of the i^{th} power unit.

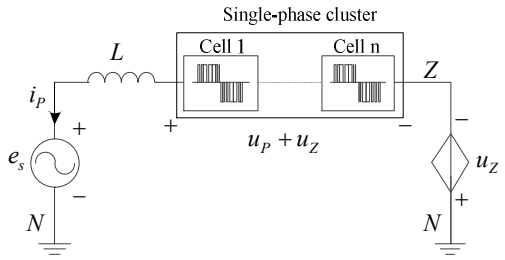


Fig. 3. Simplified single-phase circuit model.

Using the phase voltage of the power grid as a reference, the phase voltages and line currents of the three phases can be defined in the following equations:

$$\begin{cases} e_A = E_p \sin(\omega t) \\ e_B = E_p \sin(\omega t - \frac{2}{3}\pi) \\ e_C = E_p \sin(\omega t + \frac{2}{3}\pi) \end{cases} \tag{3}$$

$$\begin{cases} i_A = I_P \sin(\omega t + \varphi_P) \\ i_B = I_P \sin(\omega t + \varphi_P - \frac{2}{3}\pi) \\ i_C = I_P \sin(\omega t + \varphi_P + \frac{2}{3}\pi) \end{cases} \tag{4}$$

The injected zero-sequence voltage is assumed to be:

$$u_z = V_z \sin(\omega t + \varphi_z) \tag{5}$$

E_p is the amplitude of the positive phase voltage, and I_p and φ_p are the amplitude and original phase angle of the output positive current. φ_p can be either 0 or π depending on the current direction. V_z and φ_z are the amplitude and original phase angle of the zero-sequence voltage that is used to adjust the power between the phase clusters.

The active power produced by the inductor can be ignored; therefore, the active power produced by each phase cluster of the CHB converter can be calculated as:

$$\begin{aligned} P_{Link} &= \frac{1}{T}\int_0^T i \cdot (\sum_{i=1}^{n} S_i u_{dci}) d(\omega t) \\ &= \frac{1}{T}\int_0^T i \cdot (e_s + u_z) d(\omega t) \end{aligned} \tag{6}$$

Based on Equation (6), the active power of the three-phase clusters can be expressed as:

$$\begin{cases} P_A = \frac{1}{2}E_P I_P \cos\varphi_P + \frac{1}{2}V_Z I_P \cos(\varphi_Z - \varphi_P) \\ P_B = \frac{1}{2}E_P I_P \cos\varphi_P + \frac{1}{2}V_Z I_P \cos(\varphi_Z - \varphi_P + \frac{2}{3}\pi) \\ P_C = \frac{1}{2}E_P I_P \cos\varphi_P + \frac{1}{2}V_Z I_P \cos(\varphi_Z - \varphi_P - \frac{2}{3}\pi) \end{cases} \tag{7}$$

Equation (7) indicates that the active power produced by the power grid is the same for each cluster and that the sum of the active powers produced by the zero-sequence voltages equals zero. As a result, there is no effect on the total power. The active power can be adjusted by regulating the values of V_z and φ_z. By defining the second parts on the right side of Equation (7) as ΔP_A, ΔP_B and ΔP_C to simplify the calculation, they can be transformed with an abc/αβ conversion as follows:

$$\begin{bmatrix} \triangle P_\alpha \\ \triangle P_\beta \end{bmatrix} = \frac{\sqrt{2}}{2}\begin{bmatrix} \sqrt{3}\triangle P_A \\ \triangle P_B - \triangle P_C \end{bmatrix} \tag{8}$$

By substituting ΔP_A, ΔP_B and ΔP_C from Equation (7) into (8), the amplitude V_z and original phase angle φ_z are derived by:

$$V_z = \frac{2}{3I_p}\sqrt{6(\triangle P_\alpha^2 + \triangle P_\beta^2)} \tag{9}$$

$$\varphi_z = \begin{cases} \pi \cdot g(\triangle P_\alpha) - \tan^{-1}\frac{\triangle P_\beta}{\triangle P_\alpha} + \varphi_P & \triangle P_\alpha \neq 0 \\ -\frac{\pi}{2} sign(\triangle P_\beta) + \varphi_P & \triangle P_\alpha = 0 \end{cases} \tag{10}$$

where g(x) is determined by the value of x:

$$g(x) = \begin{cases} 1 & x < 0 \\ 0 & x > 0 \end{cases} \tag{11}$$

The calculated zero-sequence voltage u_z based on Equations (9)-(11) can be used to adjust the slight interphase unbalanced power under normal conditions and the major interphase unbalanced power caused by bypassing faulty units. However, in this paper, the zero-sequence voltage is separately injected to rapidly regulate the interphase power when there are bypassed faulty units.

Assume that n is the cascaded number in each phase cluster; n_A, n_B and n_C are the amounts of the faulty units in the three phases. Because the zero-sequence voltage u_z' is only applied for fault control when there is a faulty unit, the power of each unit is assumed to be balanced as shown below.

$$\frac{P_A}{n - n_A} = \frac{P_B}{n - n_B} = \frac{P_C}{n - n_C} \tag{12}$$

Based on Equations (7) and (12), the injected zero-sequence voltage u_z' after bypassing a faulty unit is obtained as:

$$V_Z' = \frac{\sqrt{2[(n_A - n_B)^2 + (n_B - n_C)^2 + (n_C - n_A)^2]}}{3n - n_A - n_B - n_C} E_P \cos\varphi_P \tag{13}$$

$$\varphi_Z' = \begin{cases} \pi \cdot g(n_B + n_C - 2n_A) + \\ \tan^{-1}\frac{\sqrt{3}(n_B - n_C)}{n_B + n_C - 2n_A} + \varphi_P & n_B + n_C - 2n_A \neq 0 \\ \frac{\pi}{2} sign(n_B - n_C) + \varphi_P & n_B + n_C - 2n_A = 0 \end{cases} \tag{14}$$

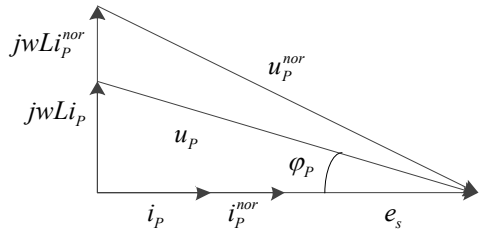


Fig. 4. Steady-state AC side vector relation of the converter.

C. Necessity of DC Voltage Optimization

When faulty units are bypassed, the full-load current of the CHB converter becomes:

$$I_P = \frac{3n - n_A - n_B - n_C}{3n} I_P^{nor} \tag{15}$$

where I_P^{nor} is the rated full-load current without a faulty unit.

Fig. 4 presents a steady-state AC side vector diagram before and after a fault, where e_s is the system phase voltage. The output voltage of the converter u_p decreases after the full-loaded current decreases, and the ratio between this voltage and the full-loaded output voltage u_p^{nor} under normal conditions is:

$$\frac{|u_P|}{|u_P^{nor}|} = \sqrt{\frac{1+(\omega L I_P / |e_s|)^2}{1+(\omega L I_P^{nor} / |e_s|)^2}} \tag{16}$$

To quantitatively analyze the change in the output voltage of a healthy unit after the fault-tolerant control and further validate the necessity of DC voltage optimization, assume that when a seven-level three-phase CHB converter works within its rated capacity, the modulation ratio is m and the voltage of inductor consumes 10% of the system phase voltage. Based on Eqs. (13)-(16), the output voltages of the healthy units are calculated as follows:

1) $n_A = 1, n_B = n_C = 0$

$$\begin{cases} u_{Ai} = 1.129 m U_{dc} \sin(\omega t - 1.89^\circ) \\ u_{Bi} = 1.163 m U_{dc} \sin(\omega t - 130.07^\circ) \\ u_{Ci} = 1.125 m U_{dc} \sin(\omega t + 131.69^\circ) \end{cases}$$

2) $n_A = n_B = 1, n_C = 0$

$$\begin{cases} u_{Ai} = 1.296 m U_{dc} \sin(\omega t - 15.48^\circ) \\ u_{Bi} = 1.378 m U_{dc} \sin(\omega t - 136.42^\circ) \\ u_{Ci} = 1.281 m U_{dc} \sin(\omega t + 121.32^\circ) \end{cases}$$

3) $n_A = 2, n_B = n_C = 0$

$$\begin{cases} u_{Ai} = 1.311 m U_{dc} \sin(\omega t - 7.43^\circ) \\ u_{Bi} = 1.407 m U_{dc} \sin(\omega t - 139.19^\circ) \\ u_{Ci} = 1.336 m U_{dc} \sin(\omega t + 142.86^\circ) \end{cases}$$

The calculation results are presented in Fig. 5, where u_A, u_B and u_C are the output voltages of each cluster, and u_{Ai}, u_{Bi} and u_{Ci} are the output voltages of the healthy units in each cluster.

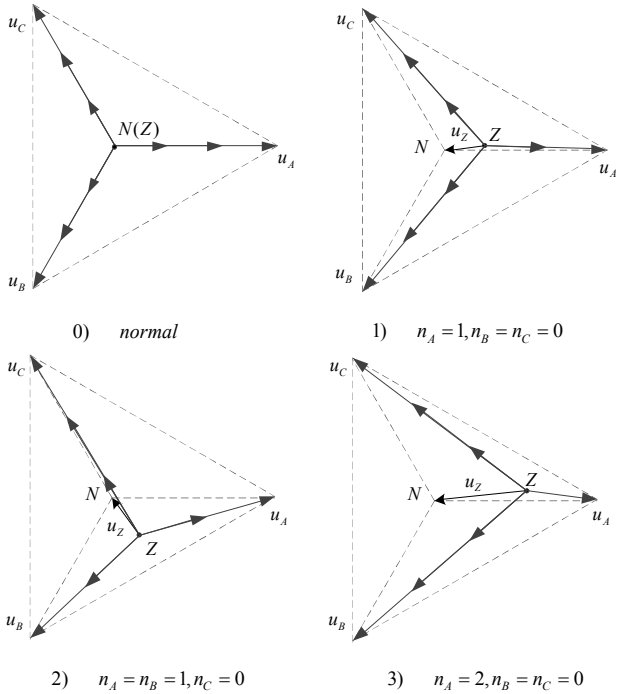


Fig. 5. Phasor diagrams of the output voltage with zero-voltage injection.

These results indicate that by injecting a zero-sequence voltage, the demanded voltage that is used to maintain the balance of the line voltage can be reduced when compared to the symmetrical bypassing method. For example, in Fig. 5, the line voltages after a No. 3 fault are balanced with the symmetrical bypassing method using three times the healthy unit voltage. However, with a zero-sequence voltage injection, the amount of voltage required can be reduced to 1.407 times the healthy unit voltage. However, the demanded voltage will increase if there are additional faulty units, especially if there are faulty units within one phase cluster.

If the demanded DC voltage is set to a high value to maintain a low m, then more faulty units can be tolerated in the converter by using a DC voltage control with a constant reference value. However, a low modulation can lead to higher THD in the output voltages and currents under normal conditions, thus affecting the normal grid-connected operations. If the demanded voltage is set to a value based on the normal state, this setting can result in over-modulation during a multi-unit fault scenario and a reduced fault tolerance. The strategy proposed in this paper optimizes the DC voltage when there is a faulty unit. Both the operational capability under normal conditions and the fault tolerance are considered. Assume that the value of m equals 0.83 in the rated capacity when a No. 1 fault occurs. The maximum modulation ratio becomes 0.97 and the converter can operate normally. However, when a No. 2 fault occurs, the modulation ratio equals 1.14 and leads to

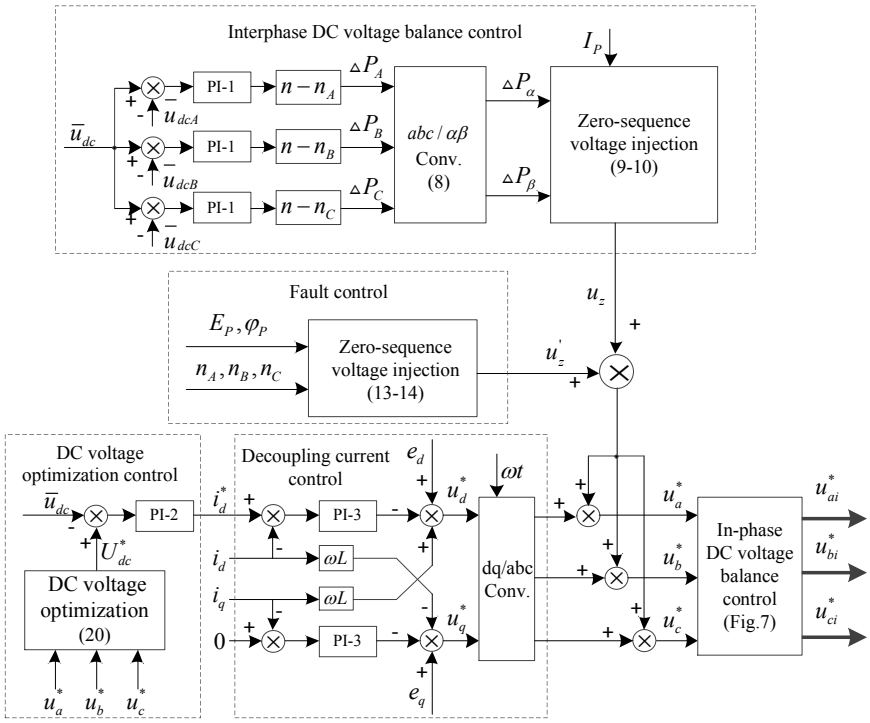


Fig. 6. Entire control block diagram.

over-modulation. However, by increasing the DC voltage by 1.14-fold, the grid-connected CHB converter can continue normal operation, and the tolerance range expands 4-fold. A greater DC voltage can address a No. 3 fault in terms of fault tolerance. However, the hardware parameters should reserve a greater safety margin.

III. Implementation of the Fault-Tolerant Control Strategy

The goals of a fault-tolerant control strategy are to balance the DC voltages of healthy units under normal or faulty conditions, adjust the input power factor and maintain sinusoidal input currents. The entire control block is shown in Fig. 6. It contains five control components: a current decoupling control, interphase DC voltage balance control, in-phase DC voltage balance control, fault control and DC voltage optimization control.

The status of the i^{th} unit in the x-phase cluster can be defined as:

$$f_{xi}=\begin{cases}1 & normal\\ 0 & bypass\end{cases}(x=A,B,C;i=1,\cdots,n) \quad (17)$$

Therefore, the average DC voltage of the three-phase is:

$$\overline{u}_{dc}=\frac{\sum_{i=1}^{n}(f_{Ai}u_{dcAi}+f_{Bi}u_{dcBi}+f_{Ci}u_{dcCi})}{3n-n_A-n_B-n_C} \quad (18)$$

The average DC voltage for each phase cluster is:

$$\overline{u}_{dcx}=\frac{1}{n-n_x}\sum_{i=1}^{n}f_{xi}u_{dcxi} \qquad (x=A,B,C) \quad (19)$$

A. Decoupling Current Control

A PI controller is adopted for this component. The difference between the average voltage $\overline{u}_{dc}$ and the reference DC voltage u_{dc}^{*} is converted into a reference current i_d^{*} on the d-axis after this controller. This current then becomes one of the inputs of this component. The other two inputs are the components of the feedback current on the d-axis i_{d} and the q-axis i_{q}. The reference voltages on the d-axis and q-axis can then be expressed as:

$$\begin{bmatrix}u_d^{*}\\ u_q^{*}\end{bmatrix}=\begin{bmatrix}e_d\\ e_q\end{bmatrix}+\begin{bmatrix}0 & \omega L\\ -\omega L & 0\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix}-(k_{p3}+\frac{k_{i3}}{s})\begin{bmatrix}i_d^{*}-i_d\\ -i_q\end{bmatrix} \quad (20)$$

in which k_{p3} and k_{i3} are parameters of the PI controller, and e_{d} and e_{q} are d-axis and q-axis components of the system voltage.

The positive-sequence voltages, which can be derived from the dq/abc conversions of u_{d}^{*} and u_{q}^{*}, and the injected zero-sequence voltages u_{z}' and u_{z}, together constitute the commanded voltages u_{a}^{*}, u_{b}^{*} and u_{c}^{*} of the three-phase clusters shown in Fig. 6.

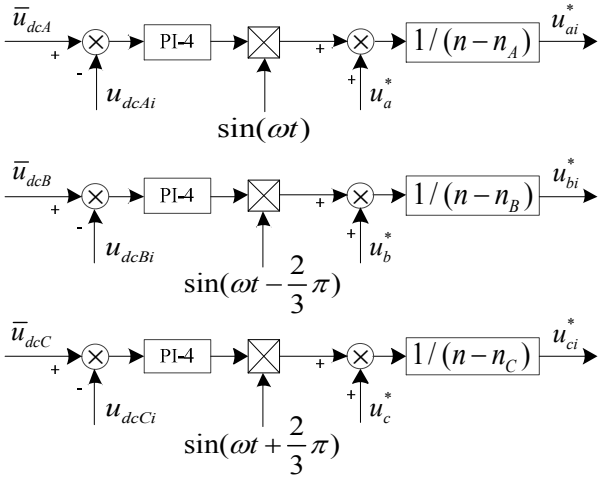


Fig. 7. Control diagram of in-phase DC voltage balancing.

B. Interphase DC Voltage Balance Control

In this component, the zero-sequence voltage is calculated according to Equations (9) and (10) with the difference power of the three-phase values ΔP_A, ΔP_B and ΔP_C. The basic control principle of this component adjusts the interphase power without changing the total power. This principle can be expressed as $\Delta P_A+\Delta P_B+\Delta P_C=0$, meaning that there are three PI controllers designed with the same parameters.

C. In-phase DC Voltage Balance Control

Fig. 7 presents a detailed diagram of the in-phase DC voltage balance control. After processing by the PI controllers, the differences between u_{dcAi}, u_{dcBi} and u_{dcCi} and their corresponding average values $\overline{u}_{dcA}$, $\overline{u}_{dcB}$ and $\overline{u}_{dcC}$ can be used to correct the active components of the modulation voltages for the three-phase clusters to obtain the reference voltages u_{ai}^*, u_{bi}^* and u_{ci}^* of the healthy units. The coefficients $sin(\omega t)$, $sin(\omega t\text{-}2\pi/3)$ and $sin(\omega t+2\pi/3)$ are produced by a phase-locked loop (PLL).

D. Fault Control

The fault control block is responsible for injecting another zero-sequence voltage according to the number of faulty units in each phase cluster. Detailed information on this can be found in Equations (13) and (14). When compared to the zero-sequence voltage injected by the interphase DC voltage control component, this injection can achieve a rapid DC voltage adjustment after a faulty unit is bypassed. Moreover, it can avoid sudden changes in the DC voltage, and increase the reliability of the converter.

E. DC Voltage Optimization Control

The objective of the DC voltage optimization control is to improve the fault tolerance of the CHB converter in the case of faults. A constant reference value is applied to the DC voltage under normal conditions. However, when a fault occurs, this value can be properly increased to less than its maximum value in order to ensure safety operation of capacitors. As shown in Fig. 6, the DC voltage optimization component uses the reference voltages of the three-phase clusters u_a^*, u_b^* and u_c^* as inputs for obtaining the DC reference voltage u_{dc}^*. By regulating the DC reference voltage, the voltage levels of u_a^*, u_b^* and u_c^* can be adjusted to a value between n-n_x-1 and n-n_x based on the peak values. The maximum value is then selected as U_{dc}^*:

$$U_{dc}^* = \begin{cases} V_{DC}^{\min} & \textit{normal} \\ \max\left(\dfrac{\sqrt{\dfrac{2}{T}\int_t^{t+T}(u_x^*)^2 d\tau}}{n-n_x-1/2}\right) \quad (x=A,B,C) & \textit{bypass} \end{cases} \tag{21}$$

where $V_{DC}^{\min} \le U_{dc}^* \le V_{DC}^{\max}$.

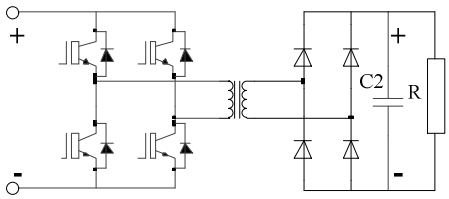


Fig. 8. Topology of the DC/DC module used in the simulation and experiment.

TABLE I
SIMULATION PARAMETERS

Line voltage of grid	3 kV
AC inductor: L	3 mH
Cascaded number: n	3
DC capacitor capacitance: C_1,C_2	8,000 μF
Load resistor: R	20 Ω
Carrier frequency for PWM	2 kHz
Voltage reference of C_2	1,000 V
Max. voltage reference of C_1	1,200 V
Min. voltage reference of C_1	1,000 V

IV. SIMULATION RESULTS

Fig. 8 presents the topology of the DC/DC module used in the simulation and experiment. The power flows from the grid side to the load side in this topology. During the simulation and experiment, this block is used to maintain the stability of the output DC voltage. The current and voltage waveforms of the DC/DC module are not shown because they are too numerous.

The simulation parameters are listed in Table I. The simulation process comprises three stages. The first stage is t < 0.5 s, in which all of the power units are engaged until they can operate in the steady state. The second stage is 0.5 s < t < 1 s, during which power unit A1 is bypassed after a fault. The third stage is 1 s < t < 1.5 s, where the faulty unit B1 is bypassed. Fig. 9 presents the DC voltage waveforms of the

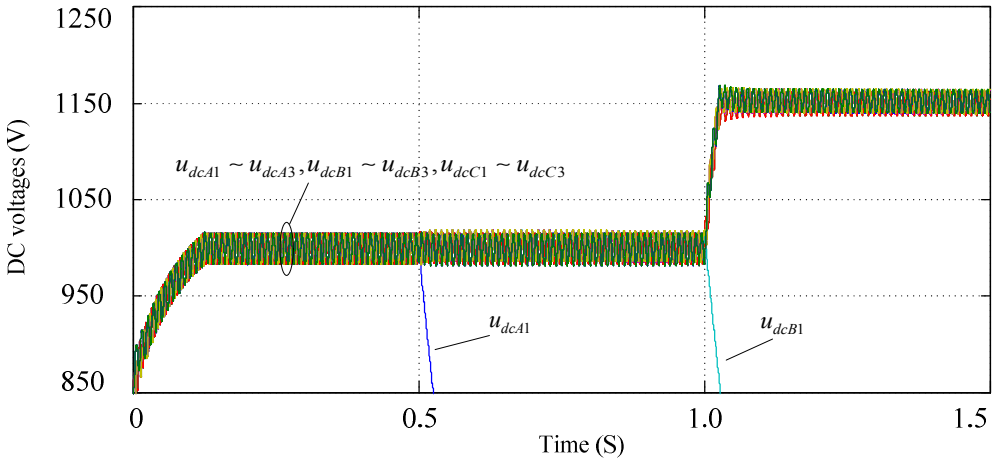
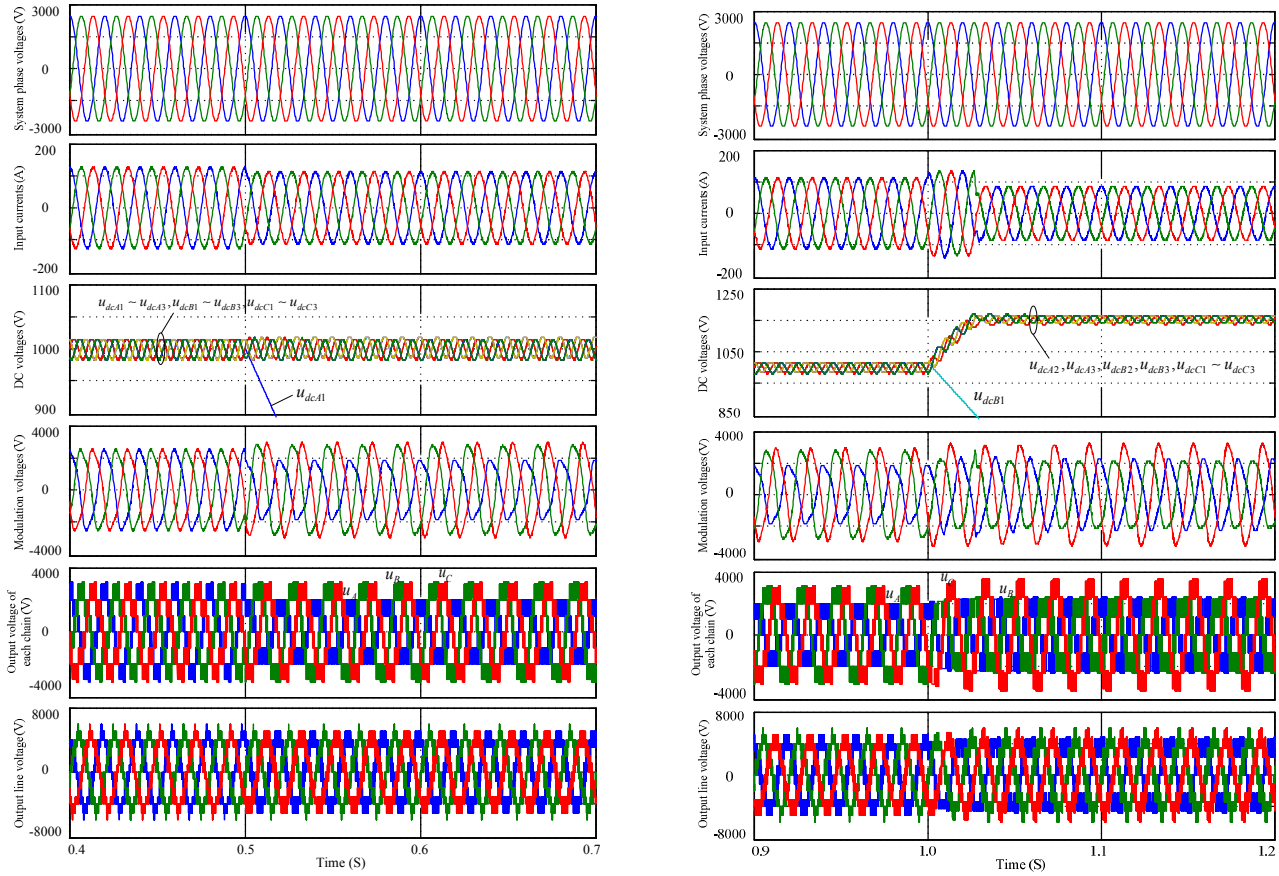


Fig. 9. Waveforms of the DC voltages in the simulation.



(a) Waveforms of the stage switching before and after A1 is bypassed. (b) Waveforms of the stage switching before and after B1 is bypassed.

Fig. 10. Waveforms of the simulation using the proposed strategy.

nine units. The voltages of the healthy units are maintained at approximately 1,000 V during the first and second stages, and they increase to 1,150 V in the third stage. In Fig. 9, the DC voltages of the faulty units A1 and B1 rapidly decrease due to the load effects after the bypass. Fig. 10 presents the waveforms of the stage switching. Fig. 10(a) presents the waveforms from the first stage switching to the second stage. The output voltages of the three-phase clusters cannot remain balanced because the zero-sequence voltage is quickly injected after unit A1 is bypassed. However, the line voltages and DC voltages of the healthy units remain balanced. Fig. 10(b) presents the waveforms from the second stage switching to the third stage. The output voltage of each phase cluster cannot reach the modulating voltage after unit B1 is bypassed. The modulating voltages of phases A and B exceed 2,000 V, and phase C exceeds 3,000 V. However, through the

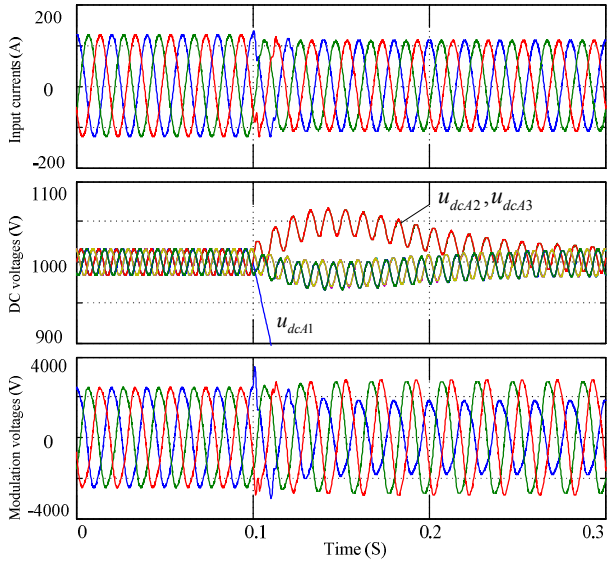


Fig. 11. Contrast simulation using a single zero-voltage.

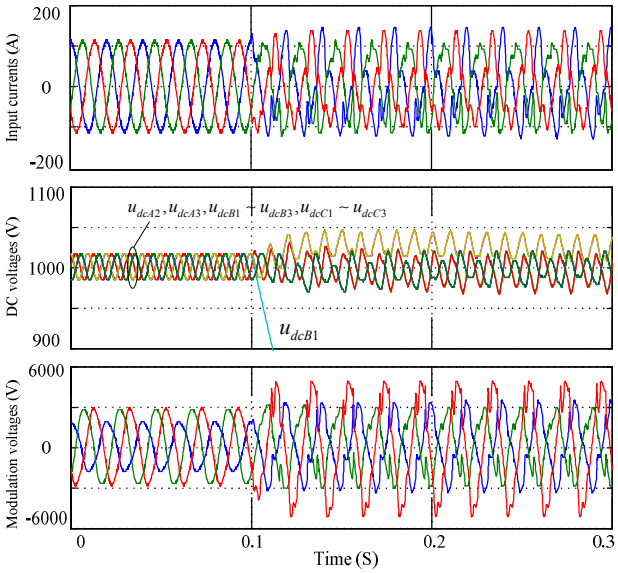


Fig. 12. Contrast simulation using the constant DC voltage reference.

DC voltage optimization control, the DC voltage of each healthy unit is raised to 1,150 V and the line voltage remains balanced. The total power decreases proportionately after bypassing the faulty units. As a result, the currents of the three phases also decrease.

Figs. 11 and 12 present simulation results for comparison. Instead of injecting a double zero-sequence voltage, this simulation only injects the single zero-sequence voltage produced by the interphase DC voltage balance control component. Compared with the results before and after the A1 unit bypass shown in Fig. 10(a), Fig. 11 illustrates that the DC voltages of healthy units can be slowly adjusted to the steady state. There is a brief period of current distortion because of the DC voltage jump. Fig. 12 presents results for comparison with Fig. 10(b) before and after the B1 unit bypass. Because of the constant DC voltage reference, the output voltage of each phase cluster cannot reach the modulating voltage after B1 is bypassed. Therefore, the voltages of the healthy units cannot continue to balance and the currents of the three phases are out of control. The above comparison demonstrates that by injecting double zero-sequence voltages, the DC voltage of a healthy unit can avoid fluctuations after bypassing faulty units and the possibility of current fluctuation can be reduced. In addition, the converter can allow for more faulty units and achieve improved fault-tolerant abilities through the DC voltage optimization control.

TABLE II
EXPERIMENTAL PARAMETERS

Line voltage of grid	350 V
AC inductor: L	3 mH
Cascaded number: n	3
DC capacitor capacitance: C_1,C_2	4,500 μF
Load resistor: R	7.8 Ω
Carrier frequency for PWM	1.6 kHz
Voltage reference of C_2	150 V
Max. voltage reference of C_1	180 V
Min. voltage reference of C_1	150 V

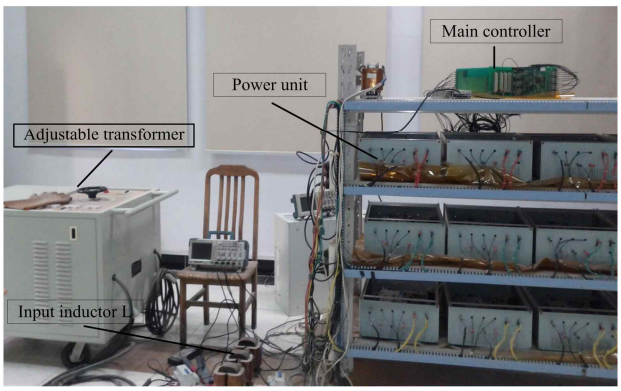
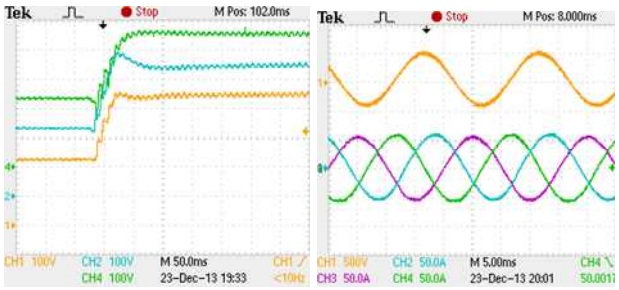


Fig. 13. Experimental platform.

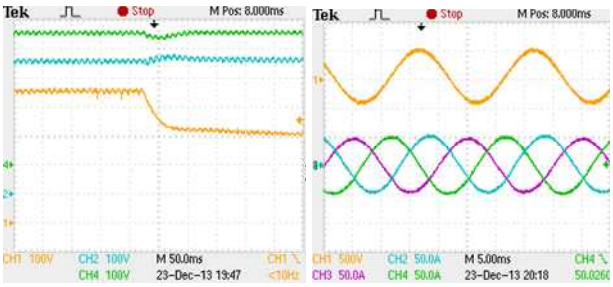
V. EXPERIMENTAL RESULTS

To further validate the proposed control strategy, an experimental platform with nine power units (Fig. 13) has been established. It adopts a master-slave control mode. The master controller applies a DSP+FPGA architecture, in which the DSP is used for the main control algorithm and the FPGA is used to send control commands and to receive power unit information. All of the power unit controllers apply the same architecture with chips of lower performance, where the DSP is responsible for the control of the isolated DC/DC block. The FPGA not only receives the control commands from the master controller and then produces PWM pulse signals but it



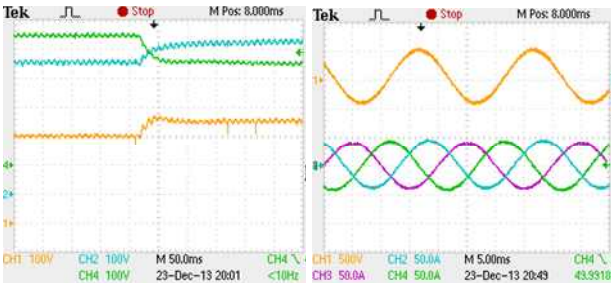
(a) (b)

Fig. 14. Experimental waveforms during start-up. (a) CH1: total DC voltage of the A-phase cluster; CH2: total DC voltage of the B-phase cluster; CH4: total DC voltage of the C-phase cluster. (b) CH1: system line voltage between A and B; CH2: input current i_A; CH3: input current i_B; CH4: input current i_C.



(a) (b)

Fig. 15. Experimental waveforms before and after A1 is bypassed. (a) CH1: total DC voltage of the A-phase cluster; CH2: total DC voltage of the B-phase cluster; CH4: total DC voltage of the C-phase cluster. (b) CH1: system line voltage between A and B; CH2: input current i_A; CH3: input current i_B; CH4: input current i_C.



(a) (b)

Fig. 16. Experimental waveforms before and after C1 is bypassed. (a) CH1: total DC voltage of the A-phase cluster; CH2: total DC voltage of the B-phase cluster; CH4: total DC voltage of the C-phase cluster. (b) CH1: system line voltage between A and B; CH2: input current i_A; CH3: input current i_B; CH4: input current i_C.

also collects the power unit information and sends this information to the master controller. The input side of the three-phase clusters is connected with an adjustable transformer. The experimental parameters are provided in Table II.

As in the simulation, the entire experimental process is separated into three stages. The results of these three stages are shown in Figs. 14-16. Due to the limited number of oscilloscope channels, the DC voltages of all of the power units are measured after being summed by an analog circuit.

Fig. 14 presents the start-up waveforms after the converter is successfully soft-charged. In Fig. 14(a), the total DC voltage of each phase cluster is raised from 220 V to 450 V. As a result, the DC voltage of each unit reaches the reference (150 V). Fig. 14(b) presents the line voltage and phase current waveforms of the system side under the steady state. The input side realizes the unit power factor rectifier and it maintains the balance of the three-phase currents, whose peak values are approximately 60 A. Fig. 15 presents the waveforms before and after an A1 fault. The total DC voltage of the A-phase cluster decreases to 300 V after the fault, whereas those of the other clusters remain the same. This indicates that the DC voltages of the healthy units remain the same. Because A1 withdraws operation, the peak value of the input current decreases to 53 A and remains balanced due to the effect of the zero-sequence voltage. Fig. 16 presents the waveforms before and after bypassing faulty unit C1. As a result of the DC voltage optimization control, the total DC voltage of the A-phase cluster increases to 350 V and the total DC voltage of the B-phase cluster increases to 525 V. However, the total DC voltage of the C-phase cluster decreases to 350 V. This result means that the DC voltage of the healthy units increases to 175 V. Meanwhile, the peak value of the input current is reduced to 46 A. These experimental results confirm that the proposed control strategy possesses the advantages of rapid DC voltage balancing and improved fault tolerance.

VI. CONCLUSIONS

This paper introduces a novel fault-tolerant control strategy using a grid-connected CHB converter. By injecting double zero-sequence voltages, this strategy efficiently solves the problems of DC voltage jumps and slow recovery when bypassing faulty units and it ensures reliable operation. In addition, this strategy applies a DC voltage optimization control method to increase the DC voltage reference when there are more faulty units, which further improves the fault tolerance. Simulation and experimental results obtained from a seven-level three-phase platform verify the feasibility and efficiency of the control strategy. This strategy exhibits good universality and can be extended to any cascaded number. It can also provide application values for the large-capacity grid connections for renewable energy and large-capacity energy storage.

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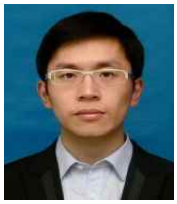

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