

Simplified SVPWM that Integrates Overmodulation and Neutral Point Potential Control

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Abstract

A simplified and effective space vector pulse-width modulation (SVPWM) algorithm with two and three levels for three-phase voltage-source converters is proposed in this study. The proposed SVPWM algorithm only uses several linear calculations on three-phase modulated voltages without any complicated trigonometric calculations adopted by conventional SVPWM. This simplified SVPWM also avoids choosing the vector sector required by conventional SVPWM. A two-level overmodulation scheme is integrated into the proposed two-level SVPWM to generate the output voltage that increases from a linear region to a six-step state with a smoothly linear transition characteristic and a simple overmodulation process without a lookup table and complicated nonlinear functions. The three-level SVPWM with a proportional-integral controller effectively balances the neutral point potential of the neutral point clamped converter. Results from the simulation in MATLAB/Simulink and the experiment based on a digital signal processor are provided to clearly demonstrate the validity and effectiveness of the proposed strategies.

Key words: Asynchronous induction motor, Grid inverter, Neutral point potential, Overmodulation, Simplified SVPWM, Three-level converter, Two-level converter

I. INTRODUCTION

Power electronic converters, which have an important role in the field of modern power systems, have been increasingly used in dispersed generation in recent decades, particularly in photovoltaic generators, wind power systems, fuel cells, high-voltage direct current transmission, microgrids, and highly efficient power drives, among others [1]-[5]. The performance of power electronic converters relies on the pulse-width modulation (PWM) technique, which influences converter harmonics, switching losses, and so on.

The PWM technique generally includes two categories, namely, sinusoidal PWM (SPWM) [6], [7] and space vector PWM (SVPWM). Compared with SPWM, SVPWM has several merits, such as high utilization ratio of direct current (DC)-link voltage, less harmonic, easily digitized implementation, and optimized switching sequence. Therefore, SVPWM is widely used in modern power electronic converters [8]-[14]. However, given that the

traditional SVPWM technique uses trigonometric functions to calculate the dwell times of selected vectors and distinguish the vector sector, modulation is more time-consuming and complex than that in the SPWM technique.

To obtain a highly efficient utilization of DC-link voltage and increase the output voltage of an inverter, an overmodulation scheme was adopted in [15]-[18]. The modulated region of SVPWM was divided into linear and nonlinear regions according to the amplitude of the modulated voltage vector. If the modulated voltage vector trajectory is located at the linear region, then SVPWM is simple; however, DC-link voltage cannot be sufficiently utilized. In [15], [16], the overmodulation region was divided into overmodulation modes I and II. Only the amplitude of the reference vector was adjusted in mode I, whereas both the angle and amplitude of the reference vector were rectified in mode II. The methods for rectifying the amplitude and angle of the reference vector are based on the nonlinear functions of the modulation index. Off-line calculation and a lookup table are typically employed to reduce calculation. A single overmodulation mode was adopted in [17]. Although this mode is simple, harmonics increase and the fundamental voltage gain of the inverter deteriorates. A two-mode overmodulation that uses limited trajectories was introduced to achieve linear and real-time modulation in the nonlinear

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region in [18]. Based on [18], the present study proposes a simplified SVPWM-based overmodulation strategy. This strategy obtains linear gains of the fundamental voltage by using simple calculations to rectify modulated voltages. Overmodulation is convenient, simple, and exhibits no complex function.

Three-level neutral point clamped (NPC) inverters, which produce less harmonics and low du/dt as well as bear a half voltage of the DC link on each power semiconductor switch compared with two-level inverters, are widely used in medium-voltage and large-capacity systems [9], [19], [20]. In [21], a traditional three-level SVPWM was introduced. However, this SVPWM is complex and requires trigonometric operations. A three-level SVPWM was modulated by transforming a normal reference frame into a 60° reference frame in [11]. The physical significance of the frame is unclear and the calculation of the phase voltage is complicated in [9]. A reference vector decomposition strategy for a three-level SVPWM was presented in [19]. The calculation of the dwell time of the active vectors is the same as that in conventional two-level SVPWM. The current study analyzes the characteristics of reference vector decomposition, simplifies the modulation process, and presents an absolute two-level modulation for three-level NPC converters.

Neutral point potential (NPP) fluctuation is a serious drawback for three-level NPC converters because it can result in different voltage stresses on semiconductor switches, which may potentially damage semiconductor switches and DC-link capacitors. Consequently, converter lifetime can be reduced and system performance can be influenced. Thus, the voltage of the capacitor must be balanced. Methods for NPP balance control have been proposed. Redundant vectors were chosen by a hysteresis controller according to differences in capacitor voltages to balance NPP in [22]. Meanwhile, the dwell times of redundant vectors were rearranged according to the direction of a neutral line or a three-phase current and voltage deviation of the DC link in [23]. Zero-sequence voltage was injected in [24]. In the present study, NPP is controlled by regulating the dwell time of redundant vectors.

This study proposes a simplified two-level SVPWM. This SVPWM integrates overmodulation into a two-level converter and extends to a three-level SVPWM with NPP control.

The remaining parts of this paper are organized as follows. Section II introduces the simplified SVPWM and its intrinsic relationship with the conventional SVPWM. Section III presents an overmodulation strategy for two-level converters. The frequency spectrum characteristics in different modulation modes are analyzed based on the proposed SVPWM. The simulation and experimental results are then provided. Section IV presents a three-level SVPWM. NPP is controlled by a proportional and integral (PI) controller. The simulation and experimental results are shown to demonstrate

the validity of the three-level SVPWM. Finally, Section V concludes the paper.

II. SIMPLIFIED TWO-LEVEL SVPWM

A. Simplified SVPWM Algorithm

A two-level voltage vector structure is shown in Fig. 1(a). When a reference vector is located at sector $N1$, (1) can be obtained via volt-second balance theory according to the traditional SVPWM algorithm. T_1 and T_2 are the dwell times of active vectors V_1 and V_2 , respectively. In (2), calculation includes trigonometric functions, which expends the computational periods of the microprocessor. As the solution of dwell times is based on the vector sector, conventional SVPWM complicates the control program and the distribution of the three-phase dwell times is not intuitional.

$$\begin{cases} T_1 V_1 + T_2 V_2 + T_0 V_{0,7} = V_f T_s \\ T_{0,7} = T_s - T_1 - T_2 \end{cases}, \quad (1)$$

$$\begin{cases} T_1 = \frac{\sqrt{3}|V_f|}{V_{dc}} T_s \sin\left(\frac{\pi}{3} - \theta\right) \\ T_2 = \frac{\sqrt{3}|V_f|}{V_{dc}} T_s \sin\theta \\ T_{0,7} = T_s - T_1 - T_2 \end{cases}, \quad (2)$$

where V_{dc} is the DC-link voltage, and $T_{0,7}$ is the dwell time of the zero vector (ZV; 000, 111).

Therefore, a simplified SVPWM is proposed to simplify calculations. The calculation steps of the simplified SVPWM are as follows.

Step 1: $M_j = \min U_j^*$; ($U_j^* = U_j/V_{dc}$); the smallest phase voltage is chosen.

Step 2: $S_j = T_s (U_j^* - M_j)$; S_j represents the dwell time of the driver signal that is equal to 1 in phase j , T_s is a switching period.

Step 3: $t_z = T_s - \max S_j$; t_z is the duration of ZV.

Step 4: $t_{cmj} = (T_s - S_j - t_z/2)/2$; t_{cmj} is a compared value of phase j for seven-segment switching ,

where $j = (a, b, c)$, which represents phases a , b , and c .

Compared with conventional SVPWM, the proposed SVPWM is simpler and easier to digitize.

B. Validating the Simplified SVPWM

The consistency of the simplified and conventional SVPWM algorithms and the validity of the proposed SVPWM are verified through theoretical deduction in this section. Fig. 1(b) shows the relationship between the phase angle of the modulated voltage and the vector sectors. In sector $N1$, the phase angle changes from 90° to 150° , and the relationship of phases a , b , and c is $U_a > U_b > U_c$, with $U_c < 0$. $\text{Min}(U_a^*, U_b^*, U_c^*) = U_c^*$ can be obtained according to step 1.

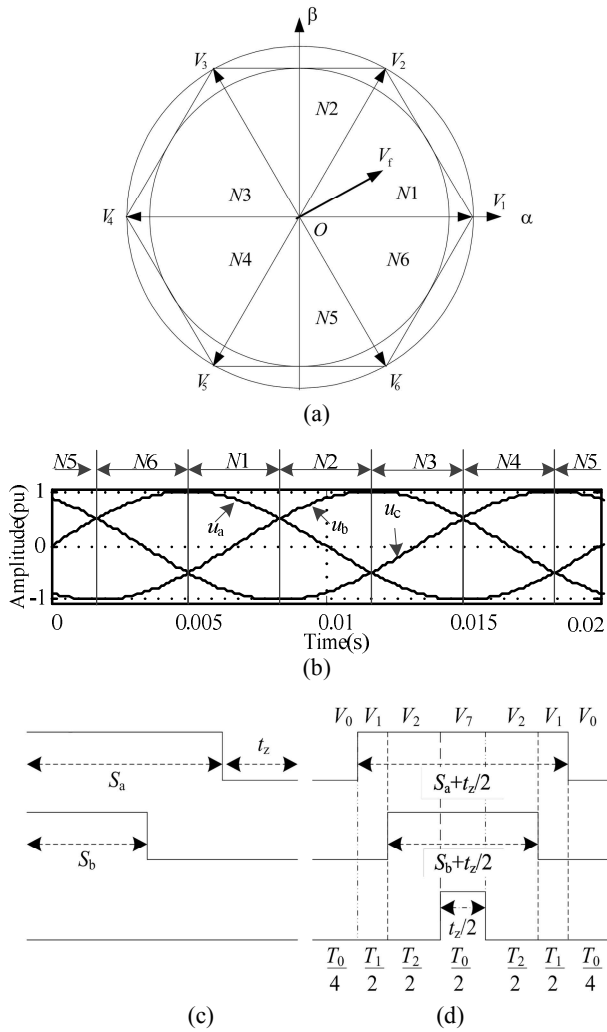


Fig. 1. Two-level space vector. (a) Two-level voltage vector structure. (b) Relationship between voltage phase angle and the sector. (c) Duration time of high potential in each phase. (d) Duration allocation.

By substituting U_c^* into step 2, it can be obtained:

$$\begin{cases} S_a = T_s(U_a^* - U_c^*) \\ S_b = T_s(U_b^* - U_c^*), U_j^* = \frac{U_j}{V_{dc}} \\ S_c = 0 \end{cases} \quad (3)$$

where $S_a \geq S_b$.

The corresponding dwell times expressed in (3) are shown in Fig. 1(c). The three nearest vectors are chosen directly by (3).

Substituting S_a into step 3, the dwell time of ZV (000, 111) can be obtained as follows:

$$t_z = T_s - S_a = T_s(1 - U_a^* + U_c^*). \quad (4)$$

According to step 4,

$$\begin{cases} t_{cma} = (T_s - S_a - t_z/2)/2 = T_s(1 - U_a^* + U_c^*)/4 \\ t_{cmb} = (T_s - S_b - t_z/2)/2 = T_s(1 + U_a^* - 2U_b^* + U_c^*)/4 \\ t_{cmc} = (T_s - S_c - t_z/2)/2 = T_s(1 + U_a^* - U_c^*)/4 \end{cases} \quad (5)$$

When the conventional SVPWM algorithm is used, (1) can be expressed as follows:

$$V_f T_s = V_1 T_1 + V_2 T_2. \quad (6)$$

According to the principle of the three nearest vectors and by simplifying (6), it is obtained the following:

$$\begin{cases} |V_f| \cos \theta T_s = |V_\alpha| T_s = |V_1| T_1 + |V_2| T_2 / 2 \\ |V_f| \sin \theta T_s = |V_\beta| T_s = \sqrt{3} |V_2| T_2 / 2 \end{cases}, \quad (7)$$

where $|V_1| = |V_2| = 2V_{dc}/3$.

$$\begin{cases} T_1 = (3|V_\alpha| - \sqrt{3}|V_\beta|) T_s / 2V_{dc} \\ T_2 = \sqrt{3}|V_\beta| T_s / V_{dc} \\ T_0 = T_s - T_1 - T_2 \end{cases} \quad (8)$$

The dwell times of T_0 , T_1 , and T_2 are shown in Fig. 1(d). Equations (6) and (7) indicate that sector number should be determined first. Then, based on the sector number, the three nearest vectors are chosen to calculate T_0 , T_1 , and T_2 . Considering that the three nearest vectors vary in different sectors, the calculations of T_0 , T_1 , and T_2 differ in each sector, which increases the complexity of the conventional SVPWM. The calculation of the simplified SVPWM in (3) depends only on the modulated voltage value. Therefore, the simplified SVPWM is indeed simpler than the conventional SVPWM.

Comparing (8) with (3) is difficult because of the variables in different coordinate frames. By transforming the variables in (8) into a three-phase stationary coordinate frame to compare the results clearly, it can be obtained the following:

$$\begin{cases} T_1 = T_s(U_a^* - U_b^*) \\ T_2 = T_s(U_b^* - U_c^*) \\ T_0 = T_s - T_s(U_a^* - U_c^*) \end{cases}, U^* = \frac{U}{V_{dc}}. \quad (9)$$

For the proposed SVPWM, S_a , S_b , and S_c in (3) are the durations of the driver signal that are equal to 1 for phases a , b , and c , respectively. In (9), T_0 , T_1 , and T_2 are the dwell times of the three nearest vectors V_0 (000, 111), V_1 (100), and V_2 (110) shown in Fig. 1(a), respectively. Without ZV (111), the duration of the driver signal that is equal to 1 for phase a is $T_2 + T_1 = T_s(U_a^* - U_c^*)$ and that for phase b is $T_2 = T_s(U_b^* - U_c^*)$, which are the same as in (3).

Using a seven-segment switching sequence for modulation, the compared value can be obtained as follows:

$$\begin{cases} t_{cma} = T_0/4 = T_s(1 - U_a^* + U_c^*)/4 \\ t_{cmb} = t_{cma} + T_1/2 = T_s(1 + U_a^* - 2U_b^* + U_c^*)/4 \\ t_{cmc} = t_{cmb} + T_2/2 = T_s(1 + U_a^* - U_c^*)/4 \end{cases} \quad (10)$$

Equations (10) and (5) are the same. Based on the deductions and results in this section, vector modulation in other sectors can be validated and is omitted.

C. Physical Significance of the Simplified SVPWM

To explain the simplified SVPWM intuitively, the synthetic process of reference vector V_r is introduced in this section. Given that reference vector V_r is located at sector M1, as shown in Fig. 1(a), calculation is conducted through (3) to (5). The high-level duration of each phase may be obtained through (3), as shown in Fig. 1(c). Based on (3) and Fig. 1(c), ZVs (V_0, V_7) and two vectors V_1 and V_2 are used to synthesize reference vector V_r , which satisfies the principle of the three nearest vectors. The compared values are obtained via (5) according to seven-segment switching, as shown in Fig. 1(d). The relationship between (3) and (5) is shown in Figs. 1(c) and 1(d). With the proposed SVPWM, the high-level duration of each phase can be easily generated by using simple arithmetic operations on the three-phase modulated voltages. The preceding analyses reveal that physical significance is clear, and (3) to (5) are intuitively expressed in Figs. 1(c) and 1(d).

According to the seven-segment modulation, the relationships among the dwell times of vectors T_0, T_1 , and T_2 and the compared values of each phase for the conventional SVPWM are shown in Fig. 1(d).

III. OVERMODULATION FOR THE SIMPLIFIED SVPWM

The ratio of the actual and maximum amplitudes of the output phase voltage by the converter is defined as the modulation index [25], that is,

$$m = U_r/U_b, \quad (11)$$

where U_r is an amplitude of the converter output phase voltage, and $U_b = 2*V_{dc}/\pi$ is the maximum amplitude of the phase voltage when the converter works at a six-step state.

According to the magnitude of the modulation index, the modulation region may be divided into three categories, namely, the linear modulation mode, overmodulation mode I, and overmodulation mode II, as shown in Fig. 1(a). In the linear modulation region, index m is between 0 and 0.969, and voltage vector trajectory is within the inscribed circle of the vector hexagon. In overmodulation mode I, the value of m changes from 0.9069 to 0.9514, and its region is between the inscribed circle and the hexagon. In overmodulation mode II, m increases from 0.9514 to 1, and vector trajectory is on the hexagon. These descriptions indicate that the trajectory of the voltage space vector is continuous in linear modulation mode and overmodulation mode I. However, the trajectory is discontinuous in overmodulation mode II. The most extreme condition is that the voltage vector is located only at six endpoints of the hexagon when $m = 1$.

A. Principle of Limited Trajectory

According to linear theory, if a variable $B \in [A, C]$, then B can be expressed as follows [18]:

$$B = (1 - k)A + kC \quad (k \in [0, 1]). \quad (12)$$

Therefore, A, C , and k can synthesize B by using the linear relationship if B is between A and C . If A is a constant, then a constant k must exist to satisfy the relationship in (12). Similar to the linear relationship among constants, if voltage space vector \bar{v}_{ref} is between \bar{v}_{in} and \bar{v}_{out} , then a constant k may be found to synthesize $\bar{v}_{ref} = (1 - k)\bar{v}_{in} + k\bar{v}_{out}$ in [18].

By transforming the modulated voltage vector into a three-phase stationary reference frame, we obtained the follows:

$$U_{j_ref} = (1 - k)U_{j_in} + kU_{j_out}, j = (a, b, c), \quad (13)$$

where U_{j_ref} is the rectified voltage vector; and U_{j_in} and U_{j_out} are the inner and outer boundary voltages, respectively.

For a reference voltage, the modulation index can be obtained and expressed by B . By substituting B and boundary modulation indices A and C into (12), an equivalent modulation index k is derived. Given that U_{j_in} and U_{j_out} in (13) are the inner and outer boundary voltages with modulation indices A and C , respectively, the rectified reference vector is achieved by substituting k , as well as the inner and outer boundary voltages, into (13). The rectified reference vector satisfies the modulation index requirement and constrains the voltage space vector trajectory within the hexagon.

Based on the previous analyses, an overmodulation strategy is easily integrated into the simplified SVPWM, which may keep vector transits in different modulation modes smooth. The process is studied in detail in the following sections.

B. Linear Modulation Mode

In linear modulation mode, the boundary conditions of the modulation indices are $A = 0$ and $C = 0.9069$, and the reference vector modulation index is $B = m$, where $0 \leq B \leq 0.9069$. Substituting them into (12) results in $k = m/0.9069$. The rectified vector can be obtained by substituting k , as well as the inner and outer unit vectors, into (13). The simplified SVPWM strategy can be used directly because the inner vector boundary is zero, and the outer reference boundary is the inscribed circle of the hexagon.

C. Overmodulation Mode I

Given that the region of overmodulation mode I is between the inscribed circle and the hexagon, two boundary modulation indices exist. The inner one is the maximum linear modulation index, and the external one is the maximum modulation index of overmodulation mode I. These indices are chosen as boundary conditions A and C , respectively. Thus, $A = 0.9069$, $C = 0.9514$, and $B = m$. By substituting A, B , and C into (12), it can be obtained that $k = (m - 0.9069)/(0.9514 - 0.9069)$. By substituting k into (13), the rectified voltage can be expressed as follows:

$$U_{j_rec} = [(1 - k)0.557 + k/U_{j1}]U_j; \quad (j = a, b, c), \quad (14)$$

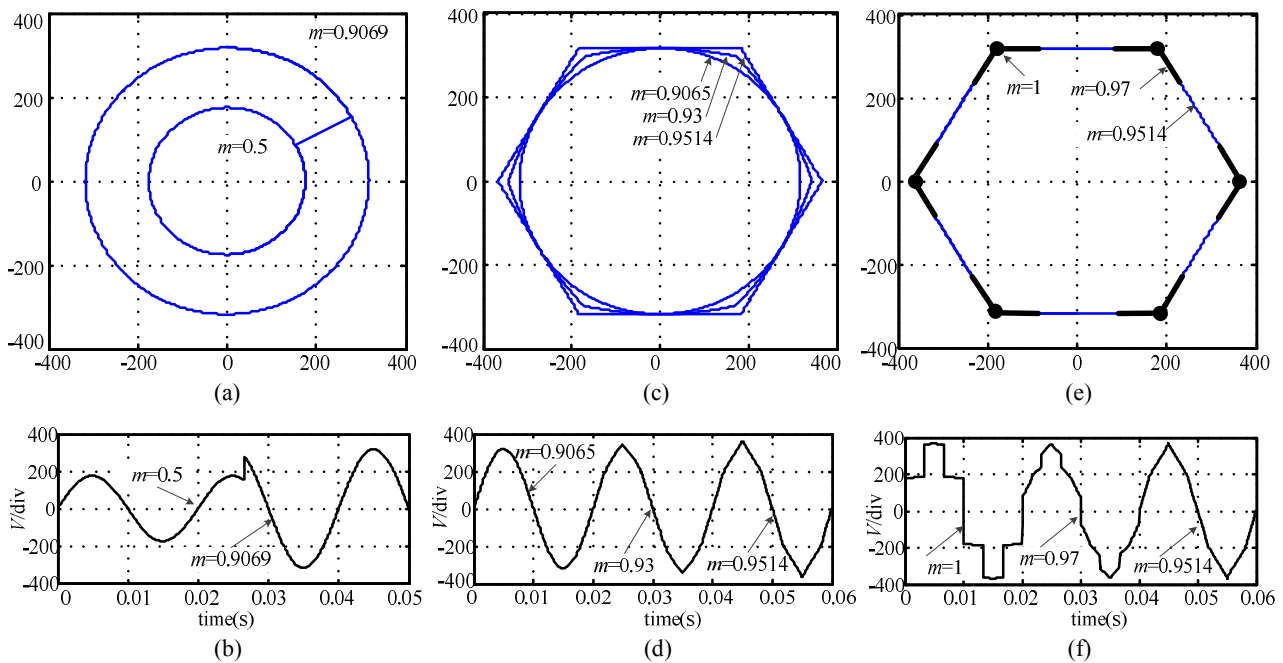


Fig. 2. Different modulation modes. (a) Voltage trajectory at the linear modulation region with $m = 0.5, 0.9069$. (b) Phase voltage at the linear modulation region with $m = 0.5, 0.9069$. (c) Voltage trajectory at overmodulation mode I with $m = 0.9069, 0.93, 0.9514$. (d) Phase voltage at overmodulation mode I with $m = 0.9069, 0.93, 0.9514$. (e) Voltage trajectory at overmodulation mode II with $m = 0.9514, 0.97, 1$. (f) Phase voltage at overmodulation mode II with $m = 0.9514, 0.97, 1$.

TABLE I

BOUNDARY VALUES OF U_{A1}, U_{B1}, U_{C1} AND U_{A2}, U_{B2}, U_{C2}

Sector N	U_{j1} ($j = a, b, c$) $U_{a1} = U_{b1} = U_{c1}$	Sector M	U_{j2} ($j = a, b, c$)		
			U_{a2}	U_{b2}	U_{c2}
1	$U_a - U_c$	1	0	1	0
2	$U_b - U_c$	2	1	1	0
3	$U_b - U_a$	3	1	0	0
4	$U_c - U_a$	4	0	1	1
5	$U_c - U_b$	5	0	0	1
6	$U_a - U_b$	6	1	0	1

Sectors N and M are based on the voltage space vector.

M lags N by 30° .

All variables are in per unit and base value is modulated voltage amplitude.

where voltage vector U_j is a unit vector, and $0.577U_j$ is the inner boundary vector. kU_j/U_{j1} is the external boundary vector. The equivalent modulation index k is generated from (12), which may guarantee that the amplitude of rectified vector U_{j_rec} is equal to those of the reference vector and the voltage trajectory within the hexagon.

D. Overmodulation Mode II

Considering that the overmodulation mode II region is outside the overmodulation mode I region, the two boundary conditions are the maximum modulation indices of overmodulation modes I and II, respectively. Therefore, $A = 0.9514$, $C = 1$, and $B = m$. By substituting A , B , and C into (12), we can obtain $k = (m - 0.9514)/(1 - 0.9514)$. According to (13) and Table I, we have

$$U_{i_ref} = (1 - k)U_j/U_{j1} + kU_{j2}; (j = a, b, c). \quad (15)$$

Rectifying the three-phase reference voltage by (14) and (15), the amplitude of the rectified voltage is equal to that of the reference voltage, and the trajectory of the rectified reference voltage vector is within the hexagon. The inner and external voltages in different modulation regions are summarized in Table I.

E. Simulation Results

The reference vector in different modulation regions is simulated in MATLAB/Simulink. Fig. 2 shows the waveforms of the voltage vector trajectories and output phase voltages in the three modulation modes. Figs. 2(a) and 2(b) show the results in the linear modulation region. The vector trajectories are circles and the phase voltage waveforms are sinusoidal. When the modulation index increases from 0.5 to 0.9069, the amplitude of the output phase voltage also increases. Figs. 2(c) and 2(d) show the voltage vector trajectories and output phase voltages in overmodulation mode I. The trajectory changes from a circle to a hexagon when the modulation index increases from 0.9069 to 0.9514. The vector trajectories and output voltage shown in Figs. 2(e) and 2(f) are the results in overmodulation mode II. When modulation index $m=0.9514$, the vector trajectory is a hexagon. When modulation index = 1, the vector trajectory is located at six endpoints of the hexagon and the converter works at a six-step state. Fig. 2 shows that the amplitude of phase voltage increases with increasing modulation index.

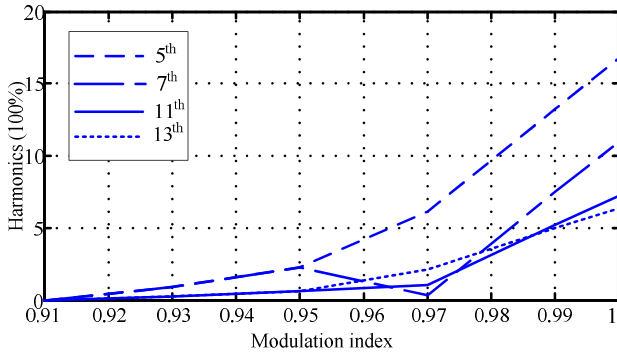


Fig. 3. Harmonic analysis with different modulation indices.

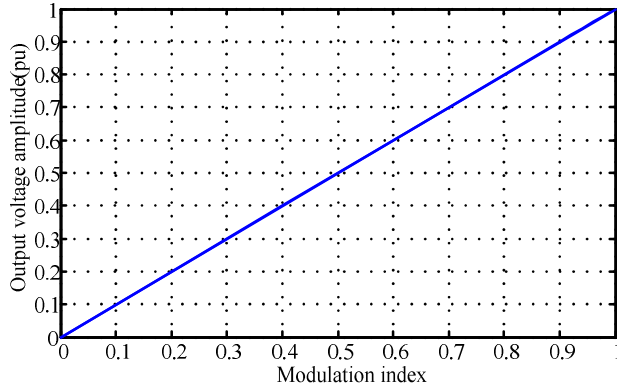


Fig. 4. Fundamental components of the output voltage as a function of the modulation index.

F. Voltage Harmonics Analysis

Based on previous analyses of the overmodulation strategy, the mathematical expressions of a three-phase modulated voltage can be determined by (14) and (15), as well as Table I, by choosing U_{j1} and U_{j2} . The modulated three-phase voltage is expanded by the following Fourier series:

$$U_j(\omega t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)). \quad (16)$$

The main components of the phase voltage frequency spectrum are low-order harmonics such as 5th-, 7th-, 11th-, and 13th-order harmonics. Fig. 3 shows the frequency spectrum of the output phase voltage with different modulation indices. The percentages of harmonics increase correspondingly with increasing modulation index.

The linear characteristic of the fundamental components of the output phase voltage versus the modulation index is shown in Fig. 4. The effectiveness of the proposed SVPWM based on an overmodulation scheme in obtaining a continuous output voltage from linear modulation to overmodulation with a linear characteristic is highlighted.

G. Experiment Results

A 10 kW two-level inverter prototype is set up to verify the proposed method by using a 2.2 kW asynchronous induction squirrel-cage motor. Fig. 5(a) shows the structure diagram of

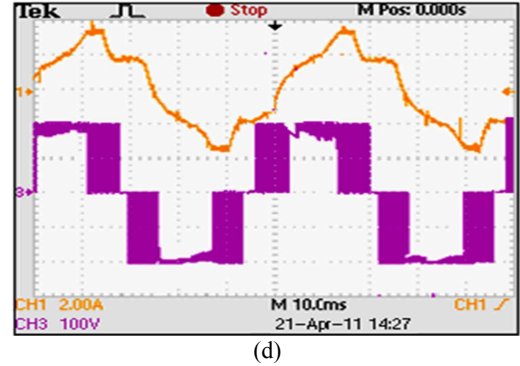
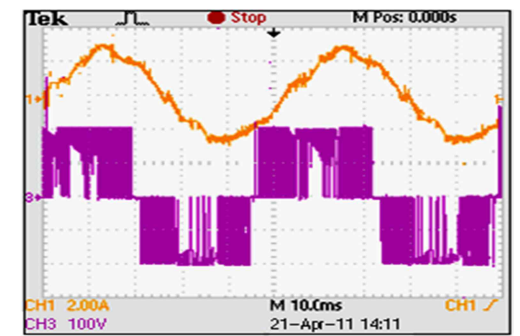
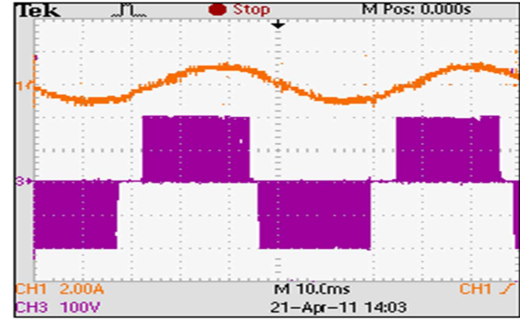
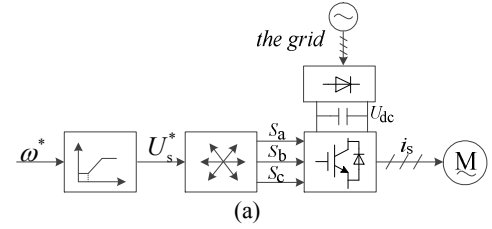


Fig. 5. Experimental structure diagram and waveforms. (a) Structure of the motor controlled by the two-level inverter. (b) Line voltage u_{ab} and phase current i_a in the linear modulation region. (c) Line voltage u_{ab} and phase current i_a at overmodulation mode I. (d) Line voltage u_{ab} and phase current i_a at overmodulation mode II.

the two-level inverter based on a motor drive system. The induction motor is driven via the two-level inverter controlled by a TMS320LF2812 digital signal processor (DSP, Texas Instruments Inc., Texas, USA) with a 5 kHz switching frequency. The electrical parameters of the motor are given in Table IV. LA28-NP and LV28P are used to measure current and voltage, respectively. A BSM 50 GB 120 DLC insulated-

gate bipolar transistor (IGBT) is used as a switch for the two-level inverter. A constant V/f control is employed to control the motor.

Figs. 5(b) to 5(d) show the stator line voltage and phase current waveforms when the inverter works at linear modulation mode, overmodulation mode I, and overmodulation mode II, respectively. With increasing modulation index, total harmonic distortion increases in overmodulation modes. The current is smooth and sinusoidal in linear mode. By contrast, the current waveforms are distorted in overmodulation modes I and II.

The stator current may be influenced by the dead time, switch nonlinear characteristic, sampling error and delay, and so on. Given that the induction motor is controlled by a simple and basic V/f control, speed and current loops are not employed. Stator current may also be directly influenced by stator voltage and other factors. If stator current is controlled by a PI controller, then stator current waveforms will be smooth and stator current distortions will be obviously reduced.

IV. THREE-LEVEL SVPWM

A. Simplified Three-Level SVPWM

Based on the decomposition algorithm introduced in [19], the simplified three-level SVPWM is studied in this section. A three-level vector hexagon is divided into six small sub-hexagons (labeled with S_1, S_2, \dots, S_6). Each hexagon represents a two-level space vector hexagon, as shown in Fig. 6(b). The simplified two-level SVPWM is employed directly in each small sub-hexagon. Two power semiconductor switches are attached to each leg of the two-level converter. An output state variable S , with a value equal to 1 or 0, is defined to represent output voltage. When $S=1$, output voltage is V_{dc} ; when $S=0$, output voltage is 0, but the three-level converter has three switching states. Fig. 6(a) shows that each phase includes four semiconductors; for example, S_{a1}, S_{a2}, S_{a3} , and S_{a4} are in phase a . The switching states of S_{a1} and S_{a2} , as well as of S_{a3} and S_{a4} , are opposite. The output of phase a is simultaneously determined by S_{a1} and S_{a2} . One of these semiconductors is decided by the central vector, which is at the center of the sub-hexagons (S_1 to S_6). Another semiconductor adjusts the amplitude of the output voltage vector. For example, if the central vector is 001 in sub-hexagon S_5 , $S_{a1}=0, S_{b1}=0$, and $S_{c2}=1$ in a switching period. For a central vector expressed by abc , if $a=0$, then $S_1=0$; if $a=1$, then $S_2=1$. When $S_{a1}=0$, phase voltage is 0 or $-V_{dc}/2$; when $S_{a2}=1$, output phase voltage is $V_{dc}/2$ or 0. The relationship among the three-level switching variables that are associated with sub-hexagon number is listed in Table II.

The sub-hexagon number and central vector can be directly obtained from the modulated voltage. During a switching period, one of the switching variables is constantly equal to 0 or 1 as determined by the sub-hexagon number. Therefore,

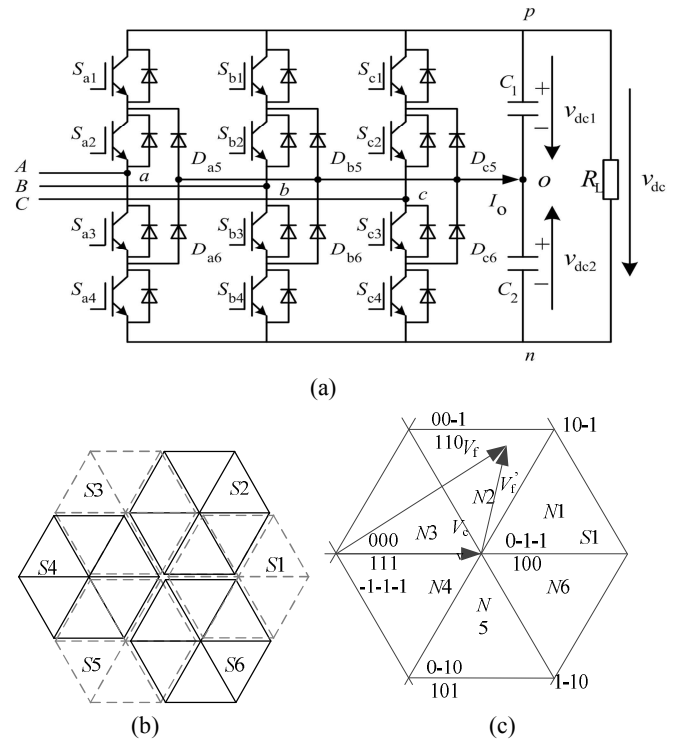


Fig. 6. Three-level converter and vector diagram. (a) Structure of the diode-clamped three-level converter. (b) Region division of the decomposed three-level space vector diagram. (c) Decomposition of a voltage reference vector.

TABLE II
RELATIONSHIP AMONG SECTOR, CENTRAL VECTOR, AND SWITCHING STATE

Sub-hexagon	Central vector V_{cv}	Switching variable state	Central voltages
S_1	100	$S_{a2}=1,$ $S_{b1}=0,$ $S_{c1}=0$	$U_{ac} = V_{dc}/3,$ $U_{bc} = U_{cc} = -V_{dc}/6$
S_2	110	$S_{a2}=1,$ $S_{b2}=1,$ $S_{c1}=0$	$U_{cc} = -V_{dc}/3,$ $U_{ac} = U_{bc} = V_{dc}/6$
S_3	010	$S_{a1}=0,$ $S_{b2}=1,$ $S_{c1}=0$	$U_{bc} = V_{dc}/3,$ $U_{ac} = U_{cc} = -V_{dc}/6$
S_4	011	$S_{a1}=0,$ $S_{b2}=1,$ $S_{c2}=1$	$U_{ac} = -V_{dc}/3,$ $U_{bc} = U_{cc} = V_{dc}/6$
S_5	001	$S_{a1}=0,$ $S_{b1}=0,$ $S_{c2}=1$	$U_{bc} = -V_{dc}/3,$ $U_{ac} = U_{cc} = V_{dc}/6$
S_6	101	$S_{a2}=1,$ $S_{b1}=0,$ $S_{c2}=1$	$U_{cc} = V_{dc}/3,$ $U_{ac} = U_{bc} = -V_{dc}/6$

only one switching variable remains to be modulated for each leg. The three-level SVPWM is then equivalent to a two-level SVPWM.

B. Neutral Potential Control

A three-level space vector consists of 27 vectors, which can be divided into four groups, namely, ZV, small vector

(SV), middle vector (MV), and large vector, depending on their magnitudes. Given that SV and MV directly connect to the neutral point, the neutral potential can be fluctuant when different SVs and MVs are chosen. Each SV includes a pair of redundant vectors with an opposite influence on the neutral potential and the same effect on synthesizing the reference vector. SVs can be divided into two categories, namely, positive SV (PSV) and negative SV (NSV), according to their influence on the neutral potential. Neutral potential balance may be achieved by adjusting the duration of PSV and NSV during each switching period.

Voltage drop V_L across an inductance connected in series with the converter is generally less than 30% of grid voltage E . By neglecting the internal resistance of the inductance and maintaining converter work at a unit power factor state, the impedance angle $r = \arctan(|V_L|/|E|) < \arctan 0.3 = 17.7^\circ$ is obtained. The waveforms of three-phase voltages and currents when the converter works as a rectifier are shown in Fig. 7. If the converter works as an inverter, $r = 180^\circ$ to $17.7^\circ = 162.3^\circ$. According to Fig. 7, the relationships between neutral current and NSV in different regions are shown in Table III.

NSV increases the neutral potential, whereas PVS decreases it. In [26], an adjusted coefficient f was used to control the NPP. The coefficient is given as follows:

$$\begin{cases} t_p = (1+f) \cdot t_z / 2 \\ t_n = (1-f) \cdot t_z / 2 \end{cases} \quad (17)$$

where t_n and t_p are the duration times of NSV and PSV, respectively.

When the coefficient f is controlled by a hysteresis [22], that is,

$$f = \begin{cases} -1 & V_{dc1} - V_{dc2} < 0 \\ 1 & V_{dc1} - V_{dc2} > 0 \end{cases} \quad (18)$$

The f value is decided by the voltage difference of the upper and lower capacitor voltages in the DC link, as shown in Fig. 6(a). If $f=1$ in (17), then $t_n=0$ and $t_p=t_z$, which indicate that only PSV is selected as an active vector in the current switching period. Otherwise, NSV is chosen. If f is equal to 1 or -1 , then the switching sequence changes from seven segments to five segments. For example, according to seven-segment switching, a vector sequence, that is, 0-1-1, 00-1, 10-1, 100, 10-1, 00-1, and 0-1-1, is used to synthesize a reference vector in $S1N1$, as shown in Fig. 6(c). When $V_{dc1} - V_{dc2} > 0$, $f=1$, $t_n=0$, and $t_p=t_z$, the vector sequence becomes 00-1, 10-1, 100, 10-1, and 00-1. The switch state changes from 1 to -1 , which increases harmonics and switching loss.

To avoid the aforementioned problems, a PI controller is used to replace the hysteresis controller based on a control strategy for the neutral potential balance control. The coefficient is redefined as follows:

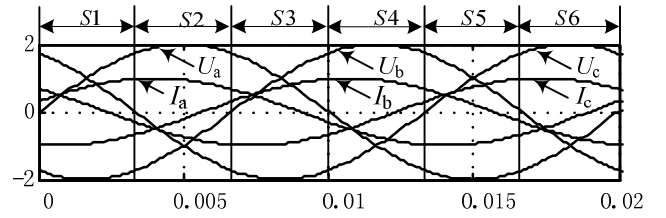


Fig. 7. Reference voltage and current of the converter ($r = 17.7^\circ$).

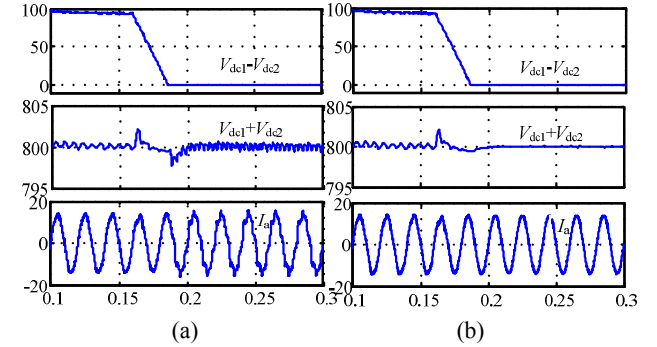


Fig. 8. Current waveforms of phase a. (a) Neutral potential controlled by the PI controller. (b) Neutral potential controlled in (16).

TABLE III
RELATIONSHIP AMONG SECTORS, NEUTRAL CURRENT, AND PHASE CURRENT

Sub-hexagon	Initial NSV	Phase current	Neutral line current
S1	0-1-1	$I_a > 0$	$I_0 = I_a$
S2	0 0-1	$I_c < 0$	$I_0 = -I_c$
S3	-1 0-1	$I_b > 0$	$I_0 = I_b$
S4	-1 0 0	$I_a < 0$	$I_0 = -I_a$
S5	-1-1 0	$I_c > 0$	$I_0 = I_c$
S6	0-1 0	$I_b < 0$	$I_0 = -I_b$

$$f = K_p \frac{\tau_S + 1}{\tau_S} (V_{dc1} - V_{dc2}), \quad (19)$$

where K_p is the proportional gain of the PI controller, and τ is an integral time constant.

The PI controller-based voltage balancing method is similar to the hysteresis controller-based strategy. The difference between them is obtaining coefficient f . For the hysteresis controller, when NPP deviates from zero, $f=1$ or -1 ; for the PI controller, the coefficient f is within -1 to 1 . If $f = \pm 1$, then the situation is the same as that in the hysteresis controller-based strategy. The switching mode is changed from seven-segment to five-segment. The PI controller can guarantee that f continuously changes within -1 to 1 , and the modulation mode is seven-segment switching at a steady state. Therefore, the PI controller-based method can improve performance, maintain seven-segment modulation, and reduce the switching loss at a steady state.

The simulation results based on MATLAB/Simulink show the dynamic response of the phase current and DC-link voltage of a diode clamped three-level voltage-source rectifier by using the two methods shown in Fig. 8.

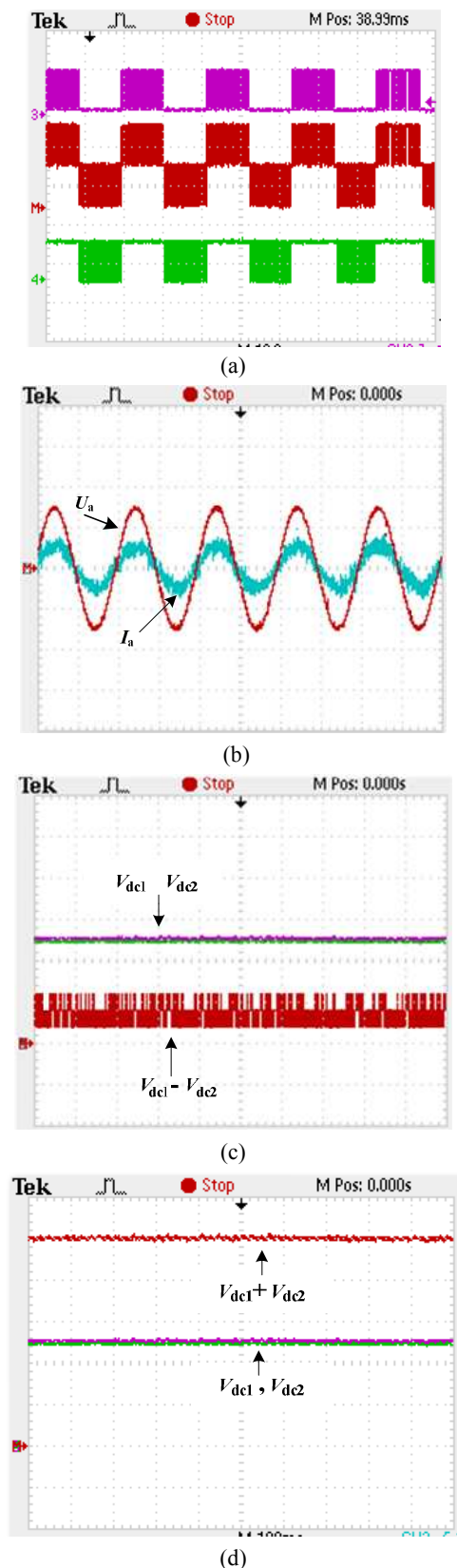


Fig. 9. Waveforms of the three-level voltage-source converter. (a) PWM of phase *a*. (b) Voltage and current of phase *a*. (c) Voltages of V_{dc1} and V_{dc2} and their difference. (d) Voltages of the DC link, V_{dc1} , and V_{dc2} .

Neutral voltage deviation is 100 V, and neutral voltage is controlled at 0.16 s. With the hysteresis controller, ripples occur in the DC-link voltage, and the alternating current (AC) is distorted at a steady state. With the PI controller, the DC-link voltage and AC current are both smooth. The dynamic responses of the two methods are nearly the same because both methods are based on the change in dwell times of PVS and NVS. Hence, the PI controller-based method may improve performance, particularly at a steady state.

C. Experiment Results

A three-level NPC rectifier prototype is built in the laboratory. A TMS320C2812 DSP is used to sample voltage and current, process data, and generate PWM drive signals. A Eupec BSM 50 GB 120 DLC IGBT driven by CONCEPT 2SD315A is used as the power switch. The parameters of the converter are listed in Table V in the Appendix, and the waveforms are obtained by a TPS2024 oscilloscope.

Fig. 9(a) shows the PWM drive signals, and Fig. 9(b) presents the grid voltage and current of phase *a*. The converter works at a unit power factor state, the peak voltage value is 311V, and the current is 3.9A. Fig. 9(c) shows the upper capacitor voltage V_{dc1} and lower capacitor voltage V_{dc2} , which are both 400V. The voltage difference between V_{dc1} and V_{dc2} is smaller than $\pm 1.5V$. Thus, the proposed method effectively suppresses neutral potential deviation. The total DC-link voltage that is equal to the sum of V_{dc1} and V_{dc2} is smooth, as shown in Fig. 9(d).

V. CONCLUSIONS

This study proposes a simplified SVPWM strategy. The intrinsic relationship between the simplified and conventional SVPWMs is deduced to verify the theoretical validity of the proposed SVPWM. The proposed SVPWM reduces computational requirements, such as avoiding trigonometric operations and vector sector selection. Moreover, digital implementation is easy. The proposed SVPWM is useful for high-performance converters.

A simplified SVPWM-based overmodulation strategy for a two-level converter is also proposed to increase output voltage with a linear characteristic. This strategy only requires arithmetic calculations to rectify three-phase modulated voltages.

Based on the central vector, the three-level SVPWM is equivalent to a two-level SVPWM for the NPC converter. A PI-based NPP strategy suppresses voltage deviation at the upper and lower capacitors with nearly no influence on the DC-link voltage. This strategy also reduces current harmonics and improves dynamic and steady state performances.

The proposed strategies are all based on simple and linear calculations, which reduce the requirements for the processor and control program design. The simulation and experiment results clearly demonstrate the validity and feasibility of the

proposed strategies. The overmodulation control strategy is easily expanded to a three-level SVPWM. However, this strategy should be combined with neutral potential control, which will be the subject in a future work.

APPENDIX

TABLE IV
PARAMETERS OF THE INDUCTION MOTOR

Parameter	Value
Power (kW)	2.2
Frequency (Hz)	50
Voltage (kV)	0.38
Stator resistance/inductance (Ohm/mH)	2.94/255.7
Rotor resistance/inductance (Ohm/mH)	2.39/255.7
Mutual inductance (mH)	235.07
Pair of poles	2

TABLE V
PARAMETERS OF THE THREE-LEVEL VOLTAGE-SOURCE
CONVERTER

Parameter	Value
Power (kW)	10
Frequency (Hz)	50
Voltage (kV)	0.38
Filter internal resistance (Ohm)	0.5
Filter inductance (mH)	5
DC-link capacitor (F)	2200e-6
DC-link voltage	800

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