

Enhanced Variable On-time Control of Critical Conduction Mode Boost Power Factor Correction Converters

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Abstract

Critical conduction mode boost power factor correction converters operating at the boundary of continuous conduction mode and discontinuous conduction mode have been widely used for power applications lower than 300W. This paper proposes an enhanced variable on-time control method for the critical conduction mode boost PFC converter to improve the total harmonic distortion characteristic. The inductor current, which varies according to the input voltage, is analyzed in detail and the optimal on-time is obtained to minimize the total harmonic distortion with a digital controller using a TMS320F28335. The switch on-time varies according to the input voltage based on the computed optimal on-time. The performance of the proposed control method is verified by a 100W PFC converter. It is shown that the optimized on-time reduces the total harmonic distortion about 52% (from 10.48% to 5.5%) at 220V when compared to the variable on-time control method.

Key words: Critical conduction mode, Digital control, Power factor correction, Total harmonic distortion, Variable on-time control

I. INTRODUCTION

Along with the remarkable developments in power electronics, the usage of non-linear loads has drastically increased. The increase usage of non-linear loads generates more harmonic current than in the past. The harmonic components of an input current are not involved in power transfer, but just circulate through transmission lines and increase the RMS value of the input current, which increases the conduction losses of the transmission lines and generates heat [1]. Because of these problems, international regulations on harmonic currents such as IEC61000-3-2 have been established. To satisfy these regulations, AC-DC converters should contain power factor correction (PFC) circuits as a pre-regulator.

For power applications less than 300W, a critical conduction mode (CRM) boost PFC converter has been widely used [2]-[5]. The main advantages of the CRM boost

PFC converter, when compared to the continuous conduction mode (CCM) boost PFC converter, are that it has no reverse recovery problem in the diode and it is easy to achieve zero voltage switching (ZVS) or quasi-ZVS without auxiliary circuits. When compared to the discontinuous conduction mode (DCM) boost PFC converter, it has less current stresses on the active and passive components, and a smaller input filter.

The current mode control method has been widely used to control CRM boost PFC converters. The current mode control method senses the rectified line voltage and generates a current reference signal by multiplying the sensed information with the output voltage of the error amplifier [6]. Then the current reference signal is compared with the sensed inductor current information to make the peak inductor current follow the waveform of the rectified line voltage. This is the best way for the power factor correction, because the inductor current is directly controlled to follow the sinusoidal reference waveform. The most popular control IC using the current mode control for the CRM boost PFC converter is the L6561/2 from STMicroelectronics. However, many semiconductor companies have started developing control ICs using the voltage mode control method for CRM boost PFC converters to reduce both the external components and

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the power loss [7]-[9]. The voltage mode CRM PFC control IC compares a ramp signal with the output voltage of the error amplifier and then the switch on-time is controlled to be constant irrespective of the line voltage. Because the inductor current is zero when the switch is turned on, the peak inductor current is proportional to the rectified line voltage. Therefore, the line current can follow the line voltage waveform achieving a unity power factor. In addition, the voltage mode CRM PFC control IC does not need a multiplier to generate the sinusoidal reference that is necessary for the current mode control IC. Because of this benefit, the internal IC circuit is simpler and the external circuit design is easier than those of the current mode CRM PFC ICs. Therefore, many applications including LCD TVs and notebook adapters are using the voltage mode CRM PFC IC and the number of applications adopting the voltage mode CRM PFC IC is increasing.

The conventional control method of the voltage mode CRM boost PFC converter is a constant on-time (COT) control. Fig. 1 shows a voltage mode CRM boost PFC converter circuit, which determines the switch turn-off instant by comparing the internal ramp signal and the output voltage of the error amplifier. Theoretically, the input current should follow the input line voltage waveform if the switch is turned on right after the inductor current reaches zero. However, there is some delay time before the switch is turned on because of the zero current detection (ZCD) circuit. The ZCD circuit is necessary to sense the instant that the inductor current reaches zero and an auxiliary winding coupled with the inductor is used for zero current detection. As shown in the waveforms of Fig. 2, the switch output capacitor (C_{oss}) starts to be discharged resonating with the inductor after the diode is turned off. Then, the auxiliary winding voltage drops starting from $n \cdot (V_o - V_{in})$. If this voltage is lower than the threshold voltage (V_{ON_ZCD}), the switch is turned on. The ZCD circuit introduces some delay time before the switch is turned on after the inductor current reaches zero and this delay time can be controlled to achieve zero voltage switching (ZVS) or quasi-ZVS by using R_{ZCD} and C_{ZCD} as shown in Fig. 1. However, this delay time causes some distortion of the input line current. Several methods have been proposed to solve this problem [6], [10]-[16]. However, some of these methods are empirical and one method is analytical. However, it cannot be applicable to wide input voltage applications.

This paper first describes some of the existing methods in section II. Then, an enhanced variable on-time (eVOT) control method is proposed in section III. Unlike the conventional control methods, the proposed method computes the switch on-time by analyzing key waveforms of the CRM boost PFC converter. The switch on-time is derived from the computation for compensating the zero-crossing distortion and the input current shaping at every switching

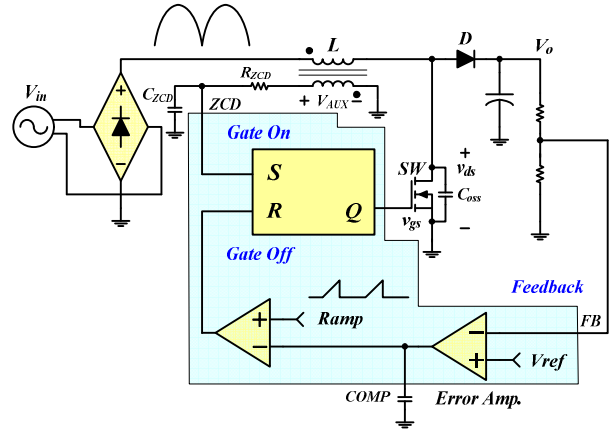


Fig. 1. Voltage mode CRM boost PFC converter circuit.

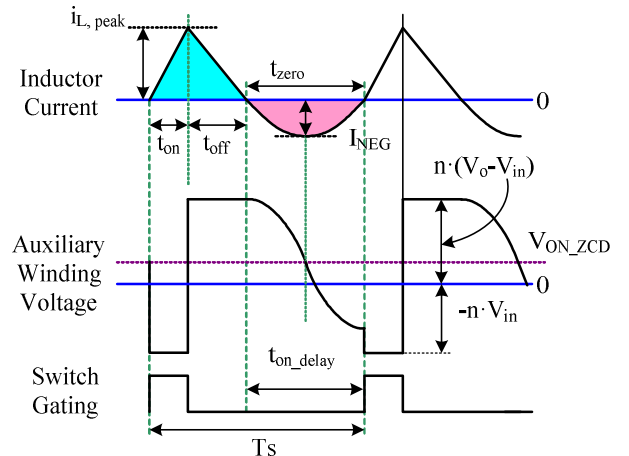


Fig. 2. ZCD circuit related waveforms.

instant. The performance of the proposed method is verified with a 400V, 100W boost PFC rectifier controlled by a digital signal controller (DSC) in section IV. Section V provides some conclusions.

II. EXISTING CONTROL METHODS TO IMPROVE CURRENT DISTORTION

A. Variable On-Time (VOT) Control Method

The CRM boost PFC converter circuit shown in Fig. 1 is analyzed when the input voltage has a positive value. As the CRM boost PFC converter has a zero-crossing detection (ZCD) circuit to detect the turn-on instant, the switching frequency of the CRM boost PFC converter is variable depending on the input voltage and the output power. The ZCD circuit is set when the inductor current is zero. A switch SW is turned on at every zero-crossing event and is turned off when the ramp signal meets the output voltage of the error amplifier. In the CRM boost PFC converter, the input current over a switching period is expressed as (1).

$$I_{in} = \frac{1}{2} i_{L,peak} = \frac{V_{in}}{2L} t_{on} \quad (1)$$

If the on-time of the switch, t_{on} , is constant, the input current follows the waveform of the input voltage as shown in (1).

This allows for a unity power factor with a sinusoidal input voltage. However, to achieve ZVS or quasi-ZVS, the turn-on instant of the switch is delayed until the switch drain-source voltage reaches zero or valley to minimize the switching loss. Because the delay time is almost constant and the t_{off} shown in Fig. 2 decreases as the input voltage decreases, the effect of the delay time is dominant around the zero crossing of the input voltage so that the THD of the input current can increase. A variable on-time control (VOT) method has been proposed to improve the THD of the input current by controlling the switch on-time as shown in Fig. 3 [6]. It simply adds a resistor R_2 between the auxiliary winding and the MOT pin. The MOT pin is for setting the internal ramp slope to control the on-time. The voltage of the MOT pin, V_{MOT} , is constant and if a resistor R_1 is used, an internal current source that is proportional to V_{MOT}/R_1 charges an internal capacitor to make a ramp signal. Without R_2 , the ramp slope is constant and the switch on-time is controlled to be constant. However, if R_2 is used, $(V_{MOT}-V_{AUX})/R_2$ current is added to V_{MOT}/R_1 . Then, the internal ramp slope changes according to the input voltage because V_{AUX} is negatively proportional to the input voltage when the switch is turned on. The ramp signal generated by I_2 varies according to the input voltage, and this signal is added to the constant ramp signal generated by I_1 as shown in Fig. 4. The internal ramp signal consists of the constant ramp signal and a ramp signal that varies according to the input voltage as shown in (2).

$$V_{Ramp} = \frac{I_1 + I_2}{C_{Ramp}} \cdot t_{on} = \frac{t_{on}}{C_{Ramp}} \cdot \left(\frac{V_{MOT}}{R_1} + \frac{V_{MOT}}{R_2} \right) + \frac{t_{on}}{C_{Ramp}} \cdot \frac{n \cdot V_{in}}{R_2} \quad (2)$$

where, C_{Ramp} is the internal capacitor for ramp generation, and n is the turn ratio of the inductor.

As the input voltage decreases, the on-time increases from t_{on1} to t_{on3} . Therefore, t_{on} is at its maximum near the AC line zero crossing point and is at its minimum at the AC line peak point. This method is very simple and effective. However, R_2 should be obtained based on experiments to find the value that minimizes the THD.

B. Perturbation On-Time (POT) Control Method

Another variable on-time control method has been proposed as shown in Fig. 5 [16]. The inductor current information and the internal ramp signal are added to be compared with the output voltage of the error amplifier. This method is another implementation of [6], because the inductor current information is proportional to the input voltage. In addition, the current limiting circuit might be triggered if too high a R_{CS} is used to improve the THD performance. This method is also empirical.

C. Analytical On-Time Adjustment Scheme

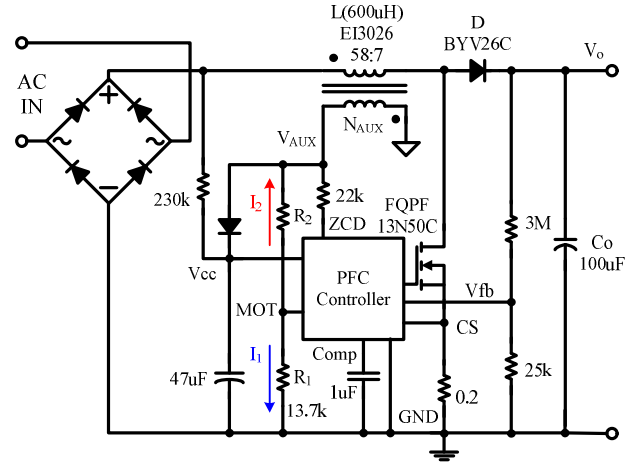


Fig. 3. Variable on-time CRM boost PFC converter.

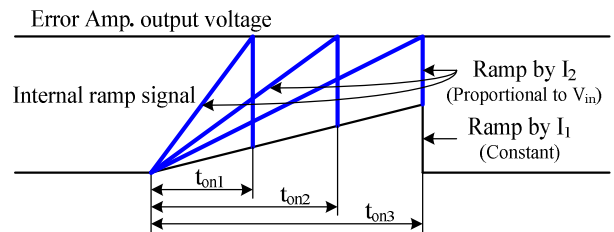


Fig. 4. Internal ramp signal of the VOT control method.

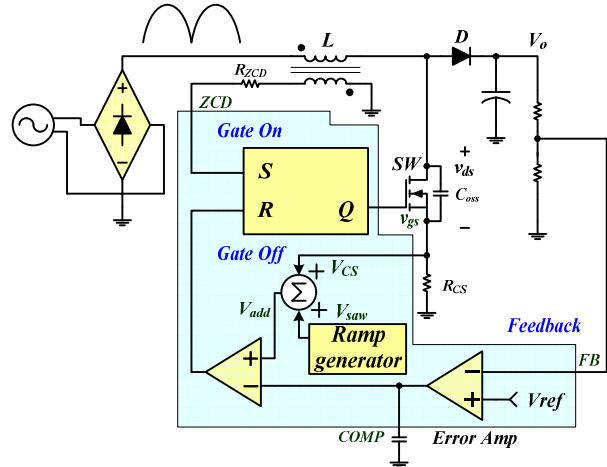


Fig. 5. Perturbation on-time CRM boost PFC converter.

There is an attempt to adjust the on-time analytically in [14]. This scheme senses the switch v_{ds} voltage to determine the ZVS instant. However, it cannot be applicable if the input voltage is higher than half of the output voltage, because the switch voltage does not become zero after the inductor current reaches zero. In addition, the analysis is performed only when the input voltage is lower than half of the output voltage.

III. PROPOSED CONTROL METHOD

Several methods have been proposed to improve the THD performance of the voltage mode CRM boost PFC converter but the methods are empirical and the analysis does not cover

all the operating conditions as described in section II. In this section, a new control method is proposed based on an analysis of the input current.

A. Analysis of the Input Current

An analysis of the inductor current is necessary to determine the variations of the switch on-time. The waveform of the inductor current during the ZCD delay time varies according to the rectified input voltage. If the rectified input voltage of the CRM boost PFC converter is higher than half of the output voltage V_o , the energy stored in the inductor when the current is negative is not sufficient to make the switch voltage v_{ds} zero. On the other hand, if the rectified input voltage of the CRM boost PFC converter is lower than half of the output voltage, the inductor is charged sufficiently so that the switch voltage drops to zero. This results in a difference in the waveform of the inductor current and the compensated on-time is determined by separate equations according to the magnitude of the input voltage.

Fig. 6 shows the waveforms of the switch gating signal, the inductor current i_L , the inductor voltage v_L , and the MOSFET drain-source voltage v_{ds} during one switching period, when V_{in} is higher than $V_o/2$. As shown in Fig. 6, the switch is turned on when the drain-source voltage reaches the valley by resonance between the switch parasitic capacitor and the boost inductor to achieve the minimum voltage switching. In this condition, the inductor current during one switching period is divided into three periods; the switch conduction period (t_0 - t_1), the diode conduction period (t_1 - t_2) and the LC resonance period (t_2 - t_3). The input current of the CRM boost PFC converter is equal to the average inductor current over one switching period. The average input current considering the delay time is expressed as (3).

$$I_{in} = \langle i_L \rangle_{T_s} = \frac{1}{T_s} \int_{T_s} i_L dt = \frac{1}{T_s} \left(\frac{1}{2} \frac{V_{in}}{L} t_{on} (t_{on} + t_{off}) - S_{neg1} \right) \quad (3)$$

where, S_{neg1} is the area of the inductor current for t_{d1} . S_{neg1} is obtained from the integral of the inductor current over a half of the resonance period after the inductor current has become zero. S_{neg1} is obtained by (4).

$$S_{neg1} = \int_{t_{d1}} \sqrt{\frac{C_{oss}}{L}} (V_o - V_{in}) \sin \omega_r t dt = 2C_{oss} (V_o - V_{in}) \quad (4)$$

where, t_{d1} is one-half of the resonance period, $\pi\sqrt{LC_{oss}}$, and ω_r is the frequency of the resonance, $1/\sqrt{LC_{oss}}$.

Equation (5) can be obtained by substituting (4) into (3) to get the average input current over one switching period.

$$I_{in} = \frac{V_{in}}{2L} \cdot \frac{1}{t_{on} + t_{off} + t_{d1}} (t_{on} (t_{on} + t_{off}) - 4LC_{oss} (M-1)) \quad (5)$$

where, $M = V_o/V_{in}$.

When V_{in} is lower than $V_o/2$, the waveforms of the switch gating signal, the inductor current i_L , the inductor voltage v_L , and the MOSFET drain-source voltage v_{ds} during one switching period are shown in Fig. 7.

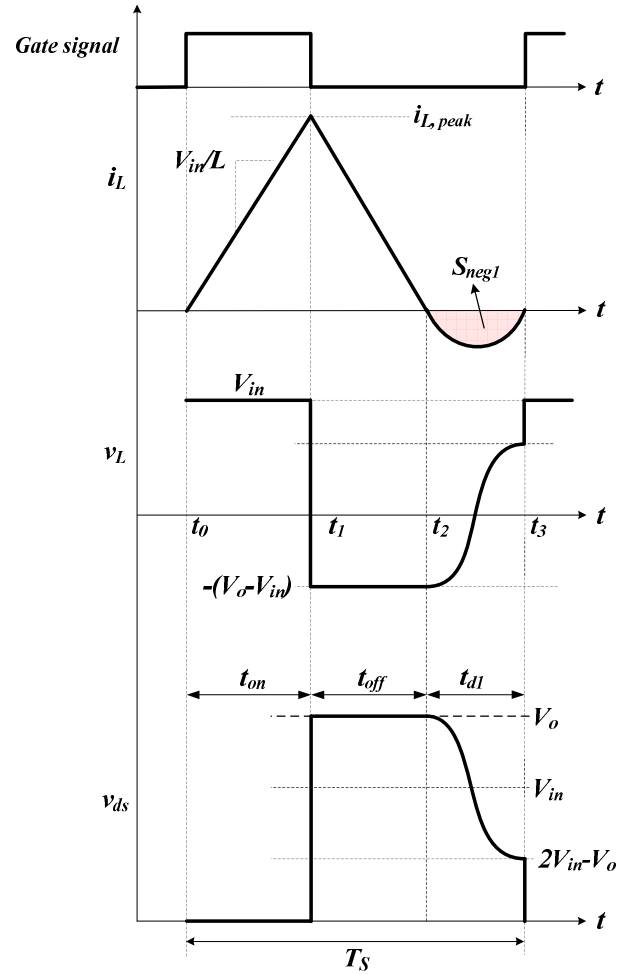


Fig. 6. Key waveforms when $V_{in} > V_o/2$.

The waveforms in Fig. 7 have one more mode when compared to Fig. 6. While the drain-source voltage falls down to the valley at t_3 when $V_{in} > V_o/2$, it reaches zero at t_4 when $V_{in} < V_o/2$. After t_4 , the MOSFET body diode starts conducting and the inductor current increases linearly during t_4 - t_6 . The time duration from t_2 to t_4 , the instant that the drain-source voltage reaches zero, is given by (6).

$$t_{res} = \frac{1}{\omega_r} \cos^{-1} \left(\frac{V_{in}}{V_{in} - V_o} \right) \quad (6)$$

And the inductor current at t_4 is obtained by (7).

$$i_L(t_4) = -\sqrt{\frac{C_{oss}}{L}} V_o (V_o - 2V_{in}) \quad (7)$$

Because the magnitude and the slope of the inductor current when the inductor current increases linearly are known, the instant that the inductor current reaches zero can be obtained. The period when the inductor current increases linearly is shown in (8).

$$t_{lin} = \sqrt{LC_{oss}} \cdot \frac{V_o - V_{in}}{V_{in}} \cdot \sin \left(\cos^{-1} \left(\frac{V_{in}}{V_{in} - V_o} \right) \right) = \frac{\sqrt{LC_{oss}} V_o (V_o - 2V_{in})}{V_{in}} \quad (8)$$

where, t_{lin} is the period from t_4 to t_6 . Therefore, when the

input voltage is lower than half of the output voltage, the area that the inductor current has a negative value, S_{neg2} , is divided into two parts; the LC-resonance period (t_2-t_4) and the linearly increasing period (t_4-t_6).

The area of the inductor current during t_{res} (t_2-t_4) is

$$S_{res} = \int_{t_2}^{t_4} i_L(t) dt = \left| \int_{t_{res}} -\sqrt{\frac{C_{oss}}{L}} (V_o - V_{in}) \sin \omega_r t dt \right| = C_{oss} \cdot V_o \quad (9)$$

and during t_{lin} (t_4-t_6), it is shown in (10).

$$S_{lin} = \frac{1}{2} |i_L(t_4)| \cdot t_{lin} = \frac{V_o}{2} \cdot C_{oss} \cdot (M - 2) \quad (10)$$

Then, the total area when the inductor current has a negative value is obtained by (11).

$$S_{neg2} = S_{res} + S_{lin} = \frac{1}{2} C_{oss} V_o M \quad (11)$$

The total area that the inductor current has a negative value increases as the input voltage decreases. Substituting S_{neg2} into (3) instead of S_{neg1} results in (12).

$$I_{in} = \frac{V_{in}}{2L} \cdot \frac{1}{T_s} (t_{on} (t_{on} + t_{off}) - (LC_{oss} M^2)) \quad (12)$$

In addition, because the period that the inductor current increases linearly is infinite when the input voltage is close to zero as shown in (8), energy is seldom transferred in this region. For these reasons, the input current distortion deteriorates especially near the AC line zero crossing point. Therefore, a proper variable on-time control is necessary for the control of the CRM boost PFC converter to alleviate the current distortion.

B. Enhanced Variable On-Time Control Method

In this section, based on the analysis of the inductor current in the previous section, a proper on-time for the CRM boost PFC converter is computed. In (5) and (12), the variable k is defined as follows.

Equation (13) is a quadratic equation related to t_{on} . By applying this variable in (5) and (12), the relationship between the input voltage and the input current can be obtained by (14).

$$k = \begin{cases} \frac{1}{t_{on} + t_{off} + t_{d1}} (t_{on} (t_{on} + t_{off}) - 4LC_{oss} (M - 1)) & \text{when } V_{in} > V_o / 2 \\ \frac{1}{t_{on} + t_{off} + t_{d2}} (t_{on} (t_{on} + t_{off}) - (LC_{oss} M^2)) & \text{when } V_{in} < V_o / 2 \end{cases} \quad (13)$$

where, $t_{d1} = \pi \sqrt{LC_{OSS}}$, $t_{d2} = \sqrt{LC_{OSS}} (\theta + (M - 1) \sin \theta)$.

$$I_{in} = \frac{V_{in}}{2L} \cdot k = \frac{V_{in}}{R_{eq}} \quad (14)$$

where, R_{eq} is $2L/k$. If the variable k is constant, the waveform of the input current follows that of the input voltage. The resulting on-time of the CRM boost PFC converter is computed using (13). By solving (13), the on-time is obtained as shown in (15).

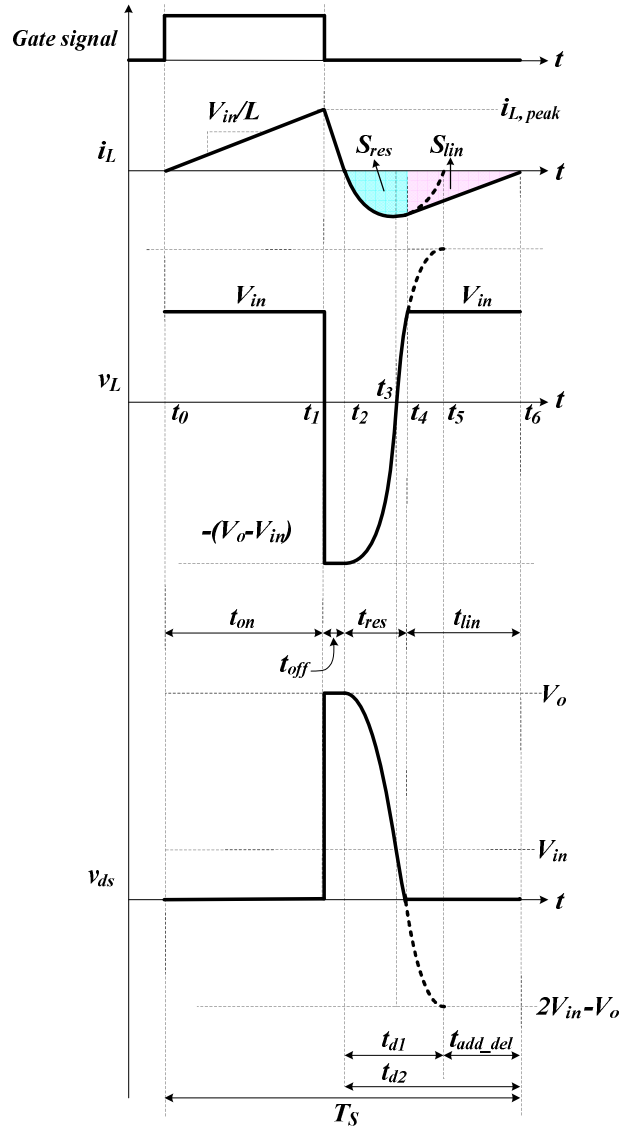


Fig. 7. Key waveforms when $V_{in} < V_o/2$.

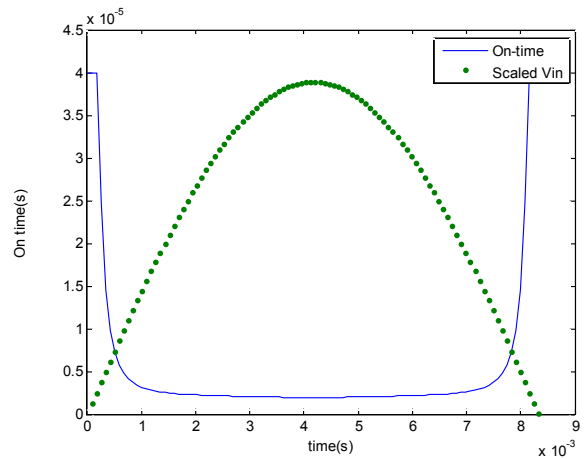


Fig. 8. Computed on-time and scaled input voltage of the CRM boost PFC converter over half of line period.

$$t_{on} = \begin{cases} \frac{k + \sqrt{k^2 + 4 \left(1 - \frac{1}{M}\right) \cdot \left(k + \frac{4t_{d1}}{\pi^2} \cdot (M-1)\right) \cdot t_{d1}}{2} & \text{when } V_{in} > V_o / 2 \\ \frac{k + \sqrt{k^2 + 4 \left(1 - \frac{1}{M}\right) \cdot \left(k + \frac{t_{d2}}{\pi^2} \cdot M^2\right) \cdot t_{d2}}{2} & \text{when } V_{in} < V_o / 2 \end{cases} \quad (15)$$

For the COT control, k can be obtained from (16) using (14) because the on-time is proportional to the output voltage of the error amplifier, v_c [7].

$$k = 2L \frac{P_o}{\eta \cdot V_{in,RMS}^2} = t_{on} = \alpha \cdot v_c \quad (16)$$

The same equation can be applied to the eVOT control, because v_c is almost constant over one AC line period and it changes according to the output load condition. Fig. 8 shows the calculated on-time of the CRM boost PFC converter controlled by the eVOT control method when the output power is 100W. When applying the eVOT control method, it is necessary to limit the maximum switch on-time because the compensated on-time goes infinite if there is no limiter in (15). Therefore, the on-time is limited to be less than 40 μ s in Fig. 8. As shown in Fig. 8, the on-time variation near the AC line zero crossing point is much larger than the variation when the input voltage is higher than half of the output voltage. In addition, it looks like that the on-time is almost constant when the input voltage is higher than half of the output voltage. The variation of the switch on-time is 16.4% when the input voltage is higher than half of the output voltage and that of the switch on-time is 1639% when the input voltage is lower than half of the output voltage. The effect of the on-time compensation when the input voltage is higher than half of the output voltage is little when compared to the effect when the input voltage is lower than half of the output voltage.

IV. EXPERIMENTAL RESULTS

The proposed control method is verified by a 100W prototype, as shown in Fig. 9. The circuit parameters for the prototype are listed in Table I. In Table I, C_{oss} is 380pF, which includes the MOSFET and diode junction capacitances. The line voltage is universal and the frequency is 60Hz. The maximum on-time is 40 μ s.

When the input voltage is close to zero, the switch off-time is reduced and the switching period can be shorter than the computation time of the DSC. Therefore, it is necessary to reduce the computation time of the DSC so that it is as short as possible. In the eVOT control method, a phase extraction and trigonometric function for the switch on-time calculation increase the computation time of the DSC. To solve this problem, t_{d2} in equation (15) can be approximated as below if it is assumed that t_{res} is $\pi/2$.

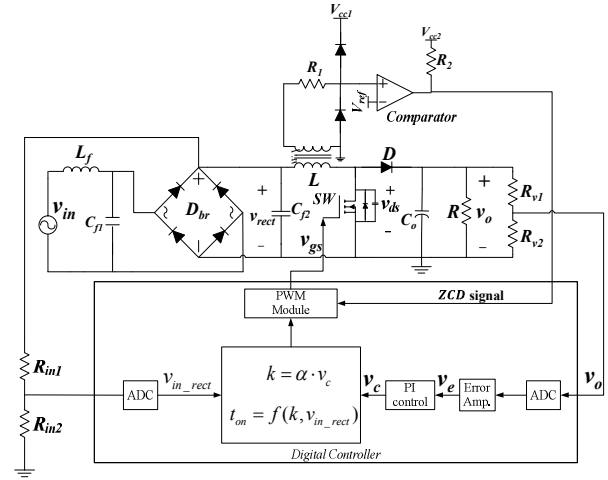


Fig. 9. Experimental circuit diagram.

TABLE I
CIRCUIT PARAMETERS

P_o	100W
V_o	400V
C_{oss}	380pF
L	430 μ H (n=8)
C_{f1}	470nF
C_{f2}	33nF
C_o	100 μ F
V_{in}	90V~264V

$$t_{d2} = \sqrt{LC_{oss}} \left(\frac{\pi}{2} + \frac{V_o - V_{in}}{V_{in}} \right) \quad (17)$$

Fig. 10 shows the error between the exact delay time and the approximate delay time, and Fig. 11 shows the error between the exact switch on-time and the switch on-time while adopting the approximate delay time. Although the error between the exact delay time and the approximate delay time has a maximum value of 18%, the switch on-time error has a maximum value of 4.7% and it is reasonable to use the approximate delay time. Fig. 12, Fig. 13, and Fig. 14 show the waveforms of a CRM boost PFC converter controlled by the COT, VOT, and eVOT control methods respectively when the AC line voltage is 220V. The periods during which the zero crossing distortion exists are about 1.48ms, 1.17ms, and 0.661ms, respectively. Fig. 15, Fig.16 and Fig. 17 show the line voltage and current of a PFC converter controlled by the COT, VOT, and eVOT control methods when the AC line voltage is 110V. When the line voltage is 110V, the periods during which the line current has zero value are about 1.28ms, 1.07ms, and 0.431ms, respectively. As mentioned previously, this period is caused because the switch on-time is not enough to transfer power to the load.

Therefore, to improve the distortion, the switch on-time should be increased near the AC line zero crossing point.

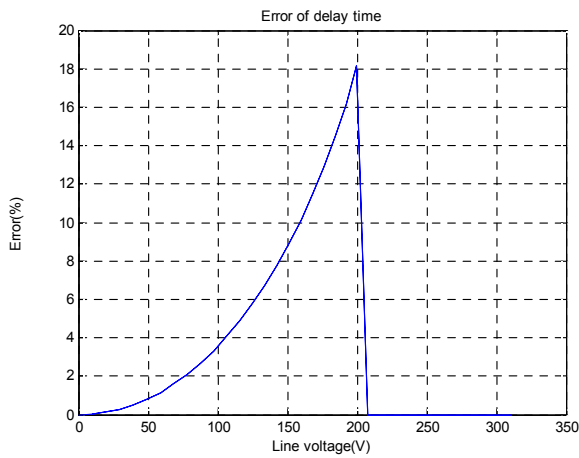


Fig. 10. Error between the exact delay time and the approximate delay time.

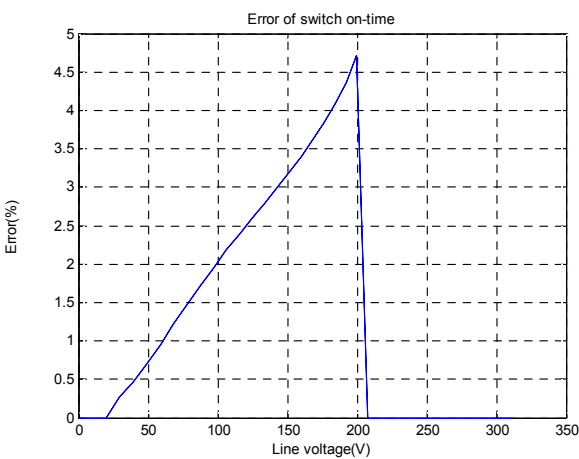


Fig. 11. Error between the exact on-time and the approximate on-time.

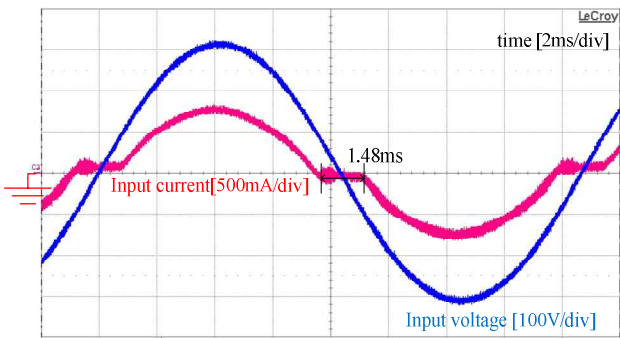


Fig. 12. Waveforms of input current and input voltage with COT control at 220V.

Fig. 18 shows the measured switch on-time of a CRM boost PFC converter controlled by the COT, VOT, and eVOT control methods near the AC line zero crossing point when the voltage is 110V and 220V.

As shown in Fig. 18, the switch on-time near the AC line zero crossing point is longest when the eVOT control method is applied. This result shows that the proposed eVOT control

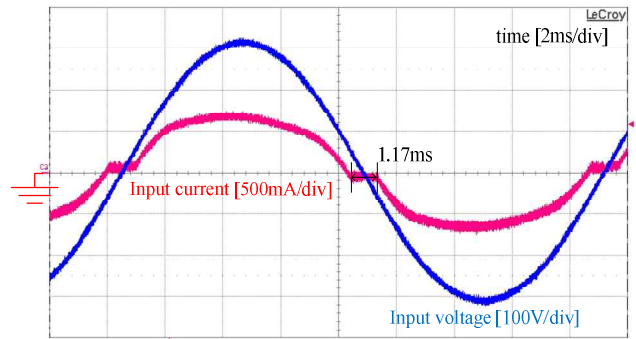


Fig. 13. Waveforms of input current and input voltage with VOT control at 220V.

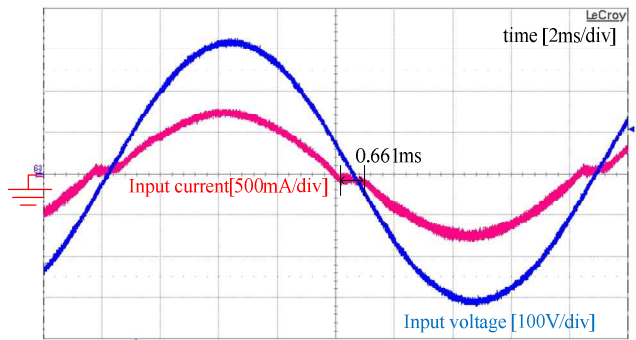


Fig. 14. Waveforms of input current and input voltage with eVOT control at 220V.

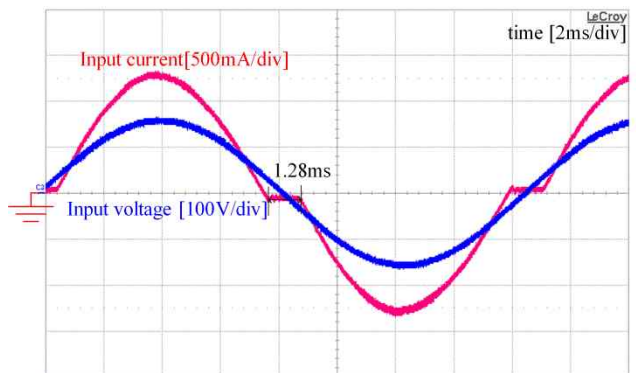


Fig. 15. Waveforms of input current and input voltage with COT control at 110V.

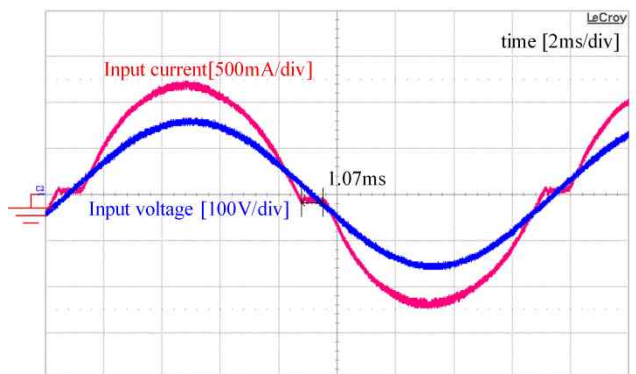


Fig. 16. Waveforms of input current and input voltage with VOT control at 110V.

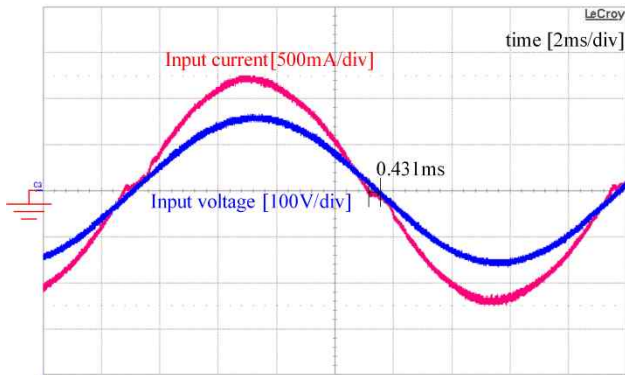


Fig. 17. Waveforms of input current and input voltage with eVOT control at 110V.

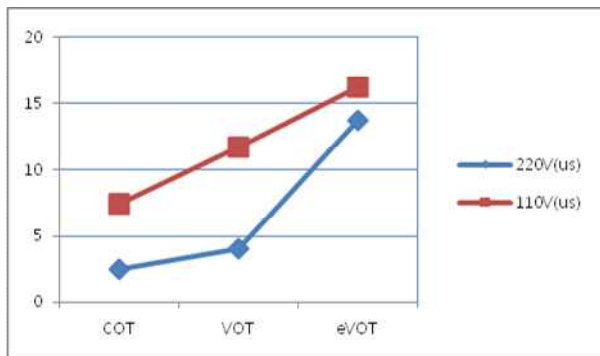


Fig. 18. Measured switch on-time near zero crossing point of AC line voltage when AC line voltage is 110V and 220V.

TABLE II

THD OF THE CRM BOOST PFC CONVERTER USING EACH CONTROL METHOD AT 100W

Input Voltage	COT	VOT	eVOT
265V	12.01%	7.67%	7.42%
220V	13.59%	10.48%	5.50%
110V	13.25%	6.87%	3.74%
90V	12.39%	6.04%	3.67%

method compensates the zero crossing distortion of the input current properly. Table II shows the THD of the CRM boost PFC converter controlled by the COT, VOT, and eVOT control methods when the output power is 100W. The THD of the CRM boost PFC converter controlled by the proposed eVOT control method shows superior performance when compared to those by the COT and VOT control methods. The THD of the eVOT control method is minimized by experiments.

In low power applications, using a TMS320F28335 is not reasonable because it is too expensive. In Fig. 19, the operation time of the DSC is shown and compared with the gate signal near the zero crossing point of the AC line voltage. During T_1 , an analog-to-digital converter (ADC)

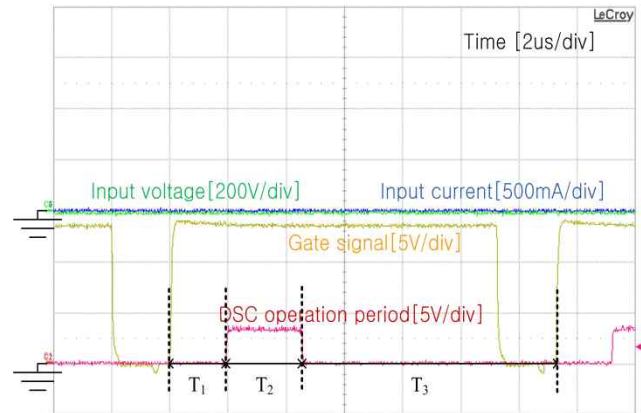


Fig. 19. Operation period of DSC near zero crossing point of AC line voltage.

converts the analog signal to digital data. After T_1 , a toggle is set and the DSC operator computes the next gate signal on-time based on the data of the ADC during T_2 . After the DSC operation, the toggle is set to off and the DSC stands by during T_3 . As shown in Fig. 19, the DSC can be replaced by a cheaper one. Because the million instructions per second (MIPS) of the TMS320F28335 is 150, a DSC whose MIPS is over 30 can replace the TMS320F28335.

V. CONCLUSIONS

This paper proposes an enhanced variable on-time control method for CRM boost PFC converters to improve the current distortion. Because of the delay time of ZVS or quasi-ZVS after the diode is turned-off in the CRM boost PFC converter, the input current distortion deteriorates especially near the AC line zero crossing point. To compensate this distortion, the optimized on-time is computed based on an analysis of the inductor current waveform. The performance of the CRM boost PFC converter controlled by the eVOT control method is demonstrated with experimental results. It is shown that the optimized on-time reduces the total harmonic distortion by about 52% (from 10.48% to 5.5%) at 220V and by 54% (from 6.87% to 3.74%) at 110V when compared to the variable on-time control method.

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