

# Improved Bridgeless Interleaved Boost PFC Rectifier with Optimized Magnetic Utilization and Reduced Sensing Noise

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## Abstract

An improved bridgeless interleaved boost power factor correction (PFC) rectifier to improve power efficiency and component utilization is proposed in this study. With combined conventional bridgeless PFC circuit and interleaved technology, the proposed rectifier consists of two interleaved and magnetic inter-coupling boost bridgeless converter cells. Each cell operates alternatively in the critical conduction mode, which can achieve the soft-switching characteristics of the switches and increase power capacity. Auxiliary blocking diodes are employed to eliminate undesired circulating loops and reduce current-sensing noise, which are among the serious drawbacks of a dual-boost PFC rectifier. Magnetic component utilization is improved by symmetrically coupling two inductors on a unique core, which can achieve independence from each other based on the auxiliary diodes. Through the interleaved approach, each switch can operate in the whole line cycle. A simple control scheme is employed in the circuit by using a conventional interleaved controller. The operation principle and theoretical analysis of the converter are presented. A 600 W experimental prototype is built to verify the theoretical analysis and feasibility of the proposed rectifier. System efficiency reaches 97.3% with low total harmonic distortion at full load.

**Key words:** Bridgeless, Circulating current, Coupled inductor, Interleaved boost, Magnetic integration, Power factor correction (PFC), Soft switching

## I. INTRODUCTION

Active power factor (PF) correction (APFC) techniques are commonly employed in many types of electronic equipment to increase the PF and decrease the total harmonic distortion (THD) factor.

The conventional APFC regulator generally comprises a bridge rectifier and a high-frequency single-ended DC–DC converter such as a boost circuit [1], as shown in Fig. 1.

However, for the boost PF correction (PFC) circuit, current flows through two rectifier diodes and one switching semiconductor (MOSFET or fast-recovery diode) during one operation cycle [2]-[5]. For low line input and high output-power applications, the high conduction loss caused by the forward voltage drop of bridge diodes dramatically degrades overall system efficiency [6]-[9]. The heat generated

within the bridge diode caused by high conduction losses can also destroy power devices [10].

To maximize system efficiency and optimize thermal performance, significant research efforts have been devoted to developing bridgeless PFC topologies [11]-[14]. In a bridgeless PFC circuit, the front-end diode bridge is removed to decrease the number of semiconductor switches in the current flowing path. Therefore, conduction losses are significantly reduced, which results in high system efficiency. A number of topologies to produce bridgeless PFC circuits have been developed [15]-[18]. One of the representative implementations is the dual-boost PFC rectifier based on the topology shown in Fig. 2 [19], [20]. In this circuit, the boost converter is combined with the input bridge diode and operates similarly to the conventional boost PFC converter.

For the dual-boost PFC circuit shown in Fig. 2, two boost converters are employed for each half line cycle. The operation of this circuit is symmetrical in two half line cycles of the input voltage [21]. Consequently, the line current simultaneously flows through only two semiconductors, which reduces

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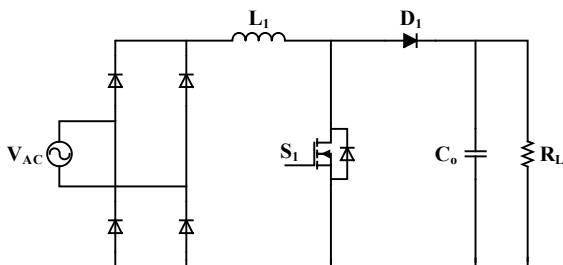


Fig. 1. Conventional boost PFC rectifier.

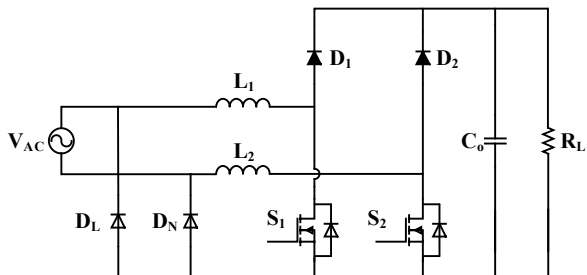


Fig. 2. Basic dual-boost bridgeless PFC rectifier.

conduction losses. The two inductors in this topology also lead to better thermal performance and improved space utilization compared with a single inductor in conventional boost topology [22]. Therefore, this converter increases system efficiency, particularly in high-power applications.

However, the dual-boost bridgeless PFC rectifier has several essential practical drawbacks [23]. As shown in Fig. 3, the undesired circulating loop marked by thicker lines can cause a large circulating current that leads to measurement errors through current-sensing resistor  $R_s$ . This problem can also cause a large electromagnetic noise and poor system control performance, particularly in average current mode control. These drawbacks make the dual-boost circuit unsuitable for practical applications. Another major drawback of this topology is the low utilization of switches and magnetic components [24]. Fig. 4 indicates that for the two boost cells, namely,  $L_1 - S_1 - D_1$  and  $L_2 - S_2 - D_2$ , each cell operates for a half line cycle, with one cell operating while the other one remains idle. As a result, the utilization of switches and magnetic components is only 50% that of the conventional boost PFC converter, which always utilizes all the components during the whole line cycle. Low component utilization can be a serious limitation in terms of system weight and power density.

To overcome these drawbacks of the dual-boost PFC, an improved interleaved boost bridgeless PFC rectifier was proposed in our previous report [25]. The proposed rectifier, which consists of two interleaved boost bridgeless PFC cells, is developed by combining the conventional dual-boost PFC rectifier with interleaved technology. In this study, a detailed analysis of the principle of improved component utilization, design consideration, comparison study of conventional PFC

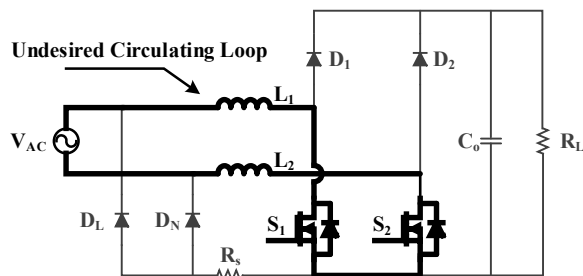
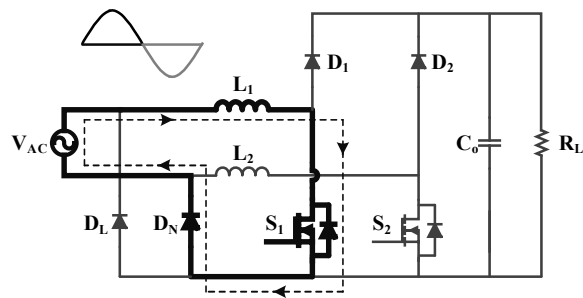
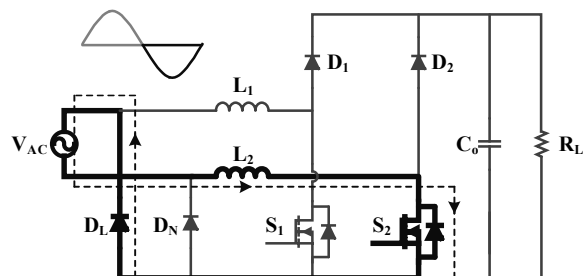


Fig. 3. Undesired circulating current loop in the dual-boost PFC rectifier.



(a)



(b)

Fig. 4. Operating stages of the dual-boost bridgeless PFC rectifier during. (a) Positive half line period. (b) Negative half line period.

circuits, and control strategy is discussed. Auxiliary blocking diodes are used to eliminate the undesired circulating current loop and improve sensing signal quality. To increase the utilization of magnetic components, the two inductors in the conventional dual-boost PFC circuit are symmetrically coupled in a single ferrite core. Hence, circuit size and cost can be reduced. The interleaved technique is also introduced to the conventional topology. Thus, the switches can operate during the whole line cycle, which increases MOSFET utilization. When operating in critical conduction mode (CrM), the switches can achieve soft switching to reduce switching loss and enhance conversion efficiency without any auxiliary circuit. Through the interleaved operation, the current waveform can exhibit lower ripple and smaller harmonic content than those of conventional topologies under the same power condition. Therefore, the sizes and losses of the boost inductors and filtering stages can be reduced and switching losses can be decreased. The design considerations on inductance value and

component current stresses of conventional continuous conduction mode (CCM) boost PFC, CrM dual-boost PFC, and the proposed PFC rectifier are discussed and compared in detail. A simple and effective control scheme is employed and explained.

The rest of this paper is organized as follows. Section II elucidates the circuit configuration and operation principle of the proposed PFC rectifier. Section III explains the design consideration of the power stage and control strategy, as well as the comparison study of conventional PFC topologies. Section IV presents the simulation and experimental results. Finally, Section V concludes the paper.

## II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

### A. Circuit Configuration

The proposed rectifier is formed by combining interleaved converters with a bridgeless PFC topology as shown in Fig.5.  $S_A$  and  $S_B$  are the main switches.  $D_1 \sim D_4$  are the boost diodes, while  $D_5 \sim D_8$ ,  $D_N$ , and  $D_L$  are slow diodes.  $L_1 \sim L_4$  are equivalent boost inductors.  $C_o$  is the output capacitor,  $R_L$  is the equivalent resistive load, and  $V_{AC}$  is the input.  $R_s$  is the current sensing resistor used for the system current control loop. In its configuration, the circuit has the same number of MOSFETs as the dual-boost PFC rectifier. The proposed rectifier requires four additional slow diodes in series with the MOSFETs to block the undesired current loop as well as two fast diodes parallel with the boosting diodes that are being operated out of phase to increase system power capacity.

The equivalent circuit of the proposed rectifier is shown in Fig. 6. The circuit consists of two interleaved boost converter cells. Each cell comprises two parallel boost phases. The interleaved cell A is composed of  $L_1 - D_6 - S_A - D_1$  as phase  $A_1$  and  $L_2 - D_8 - S_B - D_2$  as phase  $A_2$ , while cell B is composed of  $L_4 - D_5 - S_A - D_4$  as phase  $B_1$  and  $L_3 - D_7 - S_B - D_3$  as phase  $B_2$ . Therefore, switch  $S_A$  is shared by the first phase of each interleaved cell  $A_1$  and  $B_1$ , while switch  $S_B$  is shared by each second phase  $A_2$  and  $B_2$ . Because of the interleaved structure,  $S_A$  and  $S_B$  can operate in the entire line cycle of the input voltage.

### B. Coupled Inductors with Optimized Magnetic Utilization

In Fig. 6, coupled inductors  $L_A$  and  $L_B$  are represented by four decoupled inductors  $L_1 \sim L_4$ .  $L_1$  and  $L_4$  are coupled closely in the same ferrite core to comprise coupled inductor  $L_A$ , whereas  $L_2$  and  $L_3$  are coupled as  $L_B$ . Although two additional inductors are indicated, the magnetic core size can be smaller, with competitive component cost, through the interleaved operation compared with conventional PFC topologies in the same power level applications. In addition, core utilization can be improved significantly and thermal

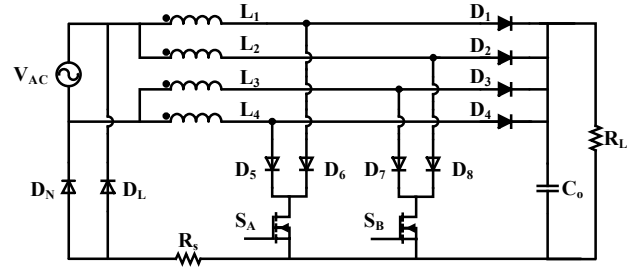


Fig. 5. Proposed interleaved boost bridgeless PFC rectifier.

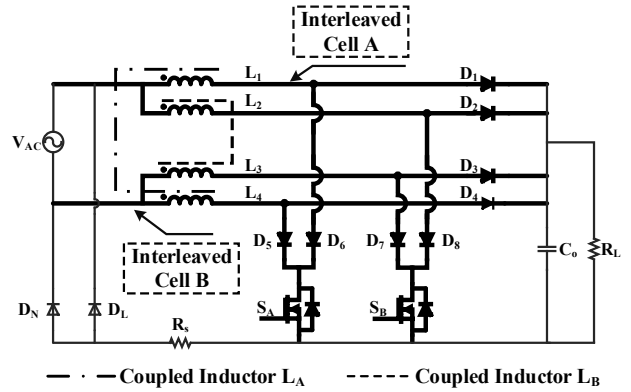


Fig. 6. Equivalent circuit of the proposed PFC rectifier.

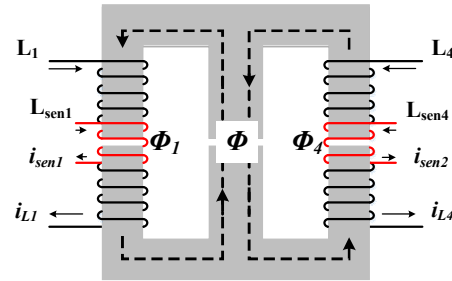


Fig. 7. Structure of the coupled inductor and current-sensing winding.

performance can be enhanced.

Fig. 7 shows the implementation structure of the coupled inductors  $L_1$  and  $L_4$  with reference polarity and magnetic flux. The two windings are wound on the two legs of the EE-type core in the same direction. As can be seen from Fig. 6 and Fig.7, current  $i_{L1}$  generates magnetic flux  $\Phi_1$  in the core leg during the on-state of  $S_A$ . The change of flux  $\Phi_1$  induces the electromotive force in winding  $L_4$ . Given that the current is blocked by diodes  $D_5$  and  $D_N$ , no circulating path exists for winding  $L_4$ . Thus, current  $i_{L4}$  is zero. Similarly, current  $i_{L1}$  is also zero when  $i_{L4}$ , which causes change of  $\Phi_4$ , flows through winding  $L_4$ .

Given that the winding structure is symmetric, that is,  $L_1 = L_4 = L$  and  $L_2 = L_3 = L$ , the turn numbers are obtained as  $N_1 = N_4 = N$  and  $N_2 = N_3 = N$ , respectively. According to Fig. 7, the flux linkages of the outer legs and the center leg can be described as follows:

$$\Psi_1 = \begin{cases} \Phi_1 N_1 = L_1 i_{L1}, & \text{during positive line cycle} \\ 0, & \text{during negative line cycle} \end{cases} \quad (1)$$

$$\Psi_4 = \begin{cases} 0, & \text{during positive line cycle} \\ \Phi_4 N_4 = L_4 i_{L4}, & \text{during negative line cycle} \end{cases} \quad (2)$$

$$\Psi = \begin{cases} \Psi_1, & \text{during positive line cycle} \\ \Psi_4, & \text{during negative line cycle} \end{cases} \quad (3)$$

According to the operation indicates that  $L_1$  and  $L_4$  work as coupled inductors with small leakage inductance. Consequently, inductors  $L_1$  and  $L_4$  are magnetically independent of each other and can be used as two inductors. The same conclusion can be drawn for coupled inductors  $L_2$  and  $L_3$ .

By referring to Fig. 7,  $L_{sen1}$  and  $L_{sen4}$  are the auxiliary current-sensing winding, which are coupled in the same legs with boost inductors  $L_1$  and  $L_4$ , respectively.  $i_{sen1}$  and  $i_{sen4}$  are the sensing signals of each current that can be used for peak current mode control.

### C. Principle for Eliminating Undesired Circulating Loop

As illustrated in Fig. 5 and Fig. 6, the current of each phase is blocked by employing  $D_5 \sim D_8$ . Thus, no circulating current loop exists among the boost phases. The current measurement error across sensing resistor  $R_s$  is accordingly eliminated, and sensing noise is reduced significantly. The electromagnetic interference (EMI) performance of the system can be improved significantly.

It should be noted that although the proposed circuit employs more diodes than the dual-boost PFC rectifier, its power capacity is higher because of interleaved operation. Considering that the forward voltage of the diode increases with rising passing current, lower conduction losses can be achieved from the proposed circuit than from the conventional signal phase boost PFC rectifier because of its lower current stresses.

Moreover, given that the input line frequency is sufficiently low (50 Hz or 60 Hz), slow-recovery diodes can be used for  $D_5 \sim D_8$ . To guarantee common-mode EMI performance,  $D_N$  conducts in the positive half line cycle, whereas  $D_L$  conducts in the negative half line cycle to connect the input to the system ground directly.

### D. Circuit Operation Principle with Improved Component Utilization

The equivalent operating circuits during the positive and negative half line periods are shown in Fig. 8(a) and Fig. 8(b), respectively. The operations of each half line cycle are explained below.

Fig. 8(a) shows that during the positive half line period, boost phases  $L_1 - D_5 - S_A - D_1$  and  $L_2 - D_8 - S_B - D_2$  operate alternatively. When  $S_A$  is turned on, current flows through  $L_1$ ,  $D_5$ ,  $S_A$ , and  $D_N$ , and energy is stored in  $L_1$ . When  $S_A$  is turned off, current flows through  $L_1$ ,  $D_1$ , and  $D_N$ , delivering the energy to the output. Similarly,  $L_2 - D_8 - S_B - D_2$  operates under the same principle with interleaved mode. During this half line

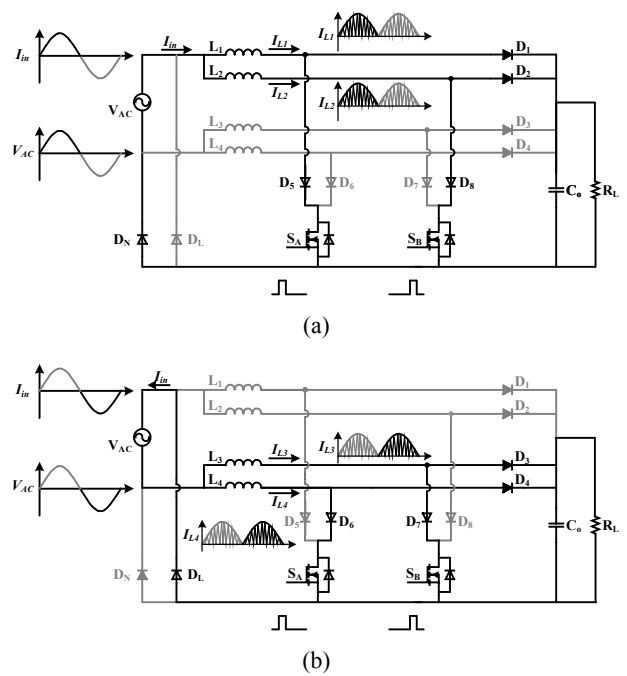


Fig. 8. Operating stages of the proposed converter in Fig.5: (a) during the positive half line period and (b) during the negative half line period.

period, boost phases  $L_4 - D_6 - S_A - D_4$  and  $L_3 - D_7 - S_B - D_4$  are in idle state. Inductors  $L_1$  and  $L_4$  are coupled in one ferrite core, whereas  $L_2$  and  $L_3$  are coupled in another ferrite core. Although  $L_3$  and  $L_4$  are idle, the magnetic cores are fully utilized.

Similar results can be obtained during the negative half line period. Fig. 8(b) shows that when  $S_B$  is turned on, energy is stored in  $L_3$  through  $D_7$ ,  $S_B$ , and  $D_L$ . When  $S_B$  is turned off, energy is released through  $L_3$ ,  $D_3$ , and  $D_L$ . Because of the interleaved operation,  $L_4 - D_6 - S_A - D_4$  operates out of phase in the same mode.

The operation analysis reveals that the switch  $S_A$  operates in phase  $A_1$ ,  $L_1 - D_5 - S_A - D_1$  during the positive half line cycle and in phase  $B_1$ ,  $L_4 - D_6 - S_A - D_4$  during the negative half line cycle. Switch  $S_B$  operates in phase  $A_2$ ,  $L_2 - D_8 - S_B - D_2$  during the positive half line cycle and in phase  $B_2$ ,  $L_3 - D_7 - S_B - D_4$ , during the negative half line cycle. Consequently,  $S_A$  and  $S_B$  can operate in the whole line cycle of the input voltage, and component utilization is improved.

### E. Operation Analysis of the Proposed Circuit

From the operation principle illustrated in Fig. 8(a) and Fig. 8(b), it can be observed that each boost phase has two slow diodes, that is, one MOSFET in the current flowing path during the on-state of the switch, as well as one slow diode and one fast diode in the current path during the off-state of the switch. This operation principle can reduce the number of conduction devices when compared with conventional boost PFC rectifiers. Hence, the conduction losses and the thermal stresses on the

TABLE I  
COMPARISON BETWEEN THE CONVENTIONAL AND PROPOSED PFC RECTIFIER IN CRM

Item	Conventional CCM boost PFC	CrM dual-boost PFC	Proposed PFC
Inductance RMS current	$\frac{P_i}{V_{i\_min}}$	$\frac{2P_i}{\sqrt{6}V_{i\_min}}$	$\frac{P_i}{\sqrt{6}V_{i\_min}}$
Inductance value	$\frac{V_{i\_min}^2 (V_o - \sqrt{2}V_{i\_min})}{2\rho V_o P_i f_{s\_min}} *$	$\frac{V_{i\_min}^2 (V_o - \sqrt{2}V_{i\_min})}{V_o P_i f_{s\_min}}$	$\frac{V_{i\_min}^2 (V_o - \sqrt{2}V_{i\_min})}{V_o P_i f_{s\_min}}$
Boost diode RMS current	$\frac{\sqrt{6}P_i}{V_{i\_min}} \sqrt{\frac{4\sqrt{2}V_{i\_min}}{\pi V_o}}$	$\frac{2P_i}{3V_{i\_min}} \sqrt{\frac{4\sqrt{2}V_{i\_min}}{\pi V_o}}$	$\frac{P_i}{3V_{i\_min}} \sqrt{\frac{4\sqrt{2}V_{i\_min}}{\pi V_o}}$
Slow diode conduction loss	$\frac{4\sqrt{2}P_i V_F}{\pi V_{i\_min}}$	zero	$\frac{\sqrt{6}P_i V_F}{12V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}}$
MOSFET RMS current	$\frac{\sqrt{2}P_i}{V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}}$	$\frac{\sqrt{2}P_i}{\sqrt{3}V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}}$	$\frac{P_i}{\sqrt{3}V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}}$
Output capacitor high-frequency RMS current	$\sqrt{\frac{8\sqrt{2}P_i^2}{3\pi V_{i\_min} V_o} - I_o^2}$	$\sqrt{\frac{4}{3} \cdot \frac{8\sqrt{2}P_i^2}{3\pi V_{i\_min} V_o} - I_o^2}$	$\sqrt{\frac{2}{3} \cdot \frac{8\sqrt{2}P_i^2}{3\pi V_{i\_min} V_o} - I_o^2}$
Rating output power capacity	High	Medium	High
Current path (switch on-state)	2 slow diodes, 1 MOSFET	1 slow diode, 1 MOSFET	2 slow diodes, 1 MOSFET
Current path (switch off-state)	2 slow diodes, 1 fast diode	1 slow diode, 1 fast diode	1 slow diode, 1 fast diode
Reverse recovery issue of the boost diode	Serious	Slight	Slight
Switch and magnetic core operation period	Whole line cycle	Half line cycle	Whole line cycle

\* $\rho$  is the required output current ripple in CCM.

semiconductor devices can be reduced. In addition, high integration and utilization of magnetic cores improve power density and reduce the overall weight of the PFC circuit.

The two power switches  $S_A$  and  $S_B$  are driven by out-phase control signals and follow the same operation principle as conventional interleaved boost topologies. This operation significantly simplifies the control scheme and can be easily implemented by using several industry standard interleaved controller ICs in the market.

According to the circuit analysis, there is no limitation in the system operation mode. However, several advantages can be obtained when the circuit is operated in CrM. Under CrM, the proposed rectifier can achieve zero current switching (ZCS) during the turn-on transition of the main switches and the reverse recovery period of the boost diodes. Compared with other operation modes, soft-switching and low current ripples increase system efficiency and reduce conducted EMI noise.

Another advantage of the proposed converter is current stress reduction for the power switch compared with conventional boost and dual-boost PFC rectifiers because of the interleaved operation.

### III. DESIGN CONSIDERATION OF THE PROPOSED CIRCUIT

#### A. Power Stage Design and Comparison Study

This section discusses the design consideration of the proposed rectifier. To design practical circuits of the proposed PFC, the key parameters of the power stage must be calculated, and the current and voltage stresses of the main power components must be carried out. During analysis and evaluation, all calculations are based on the assumptions that unity PF is realized in the proposed circuit. The reverse recovery issue of blocking diodes is neglected.

Considering that the parallel-operated boost phases are identical, the boost inductor is determined based on the inductance ripple current under low line-input conditions in CrM. Therefore, the inductor can be selected by

$$L = \frac{V_{i\_min}^2 (V_o - \sqrt{2}V_{i\_min})}{V_o P_i f_{s\_min}}, \quad (4)$$

where

- $V_{i\_min}$  input low line root mean square (RMS) voltage,
- $P_i$  rating input power,
- $V_o$  output voltage,
- $f_{s\_min}$  minimum switching frequency at low line input.

When operating in CrM, the average inductor current is 50% that of the peak value. Therefore, the RMS inductor current with one interleaved phase can be obtained as follows:

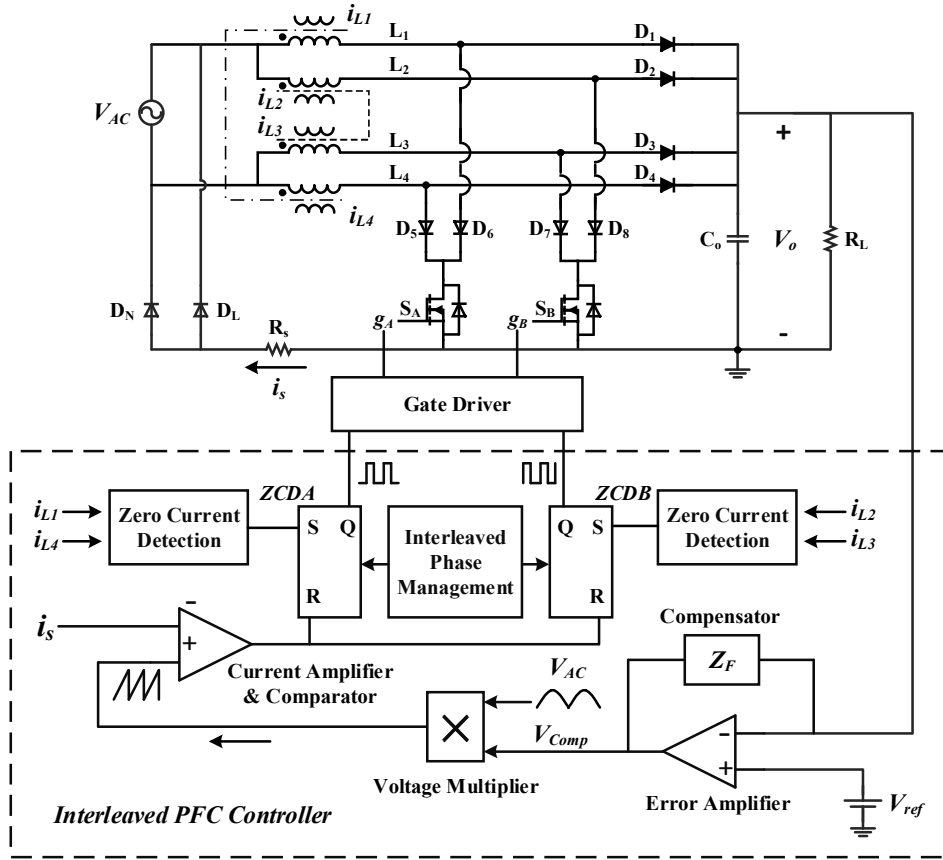


Fig. 9. Control part block diagram of the proposed circuit.

$$I_{L\_rms} = \frac{\sqrt{2}P_i}{V_{i\_min}} \frac{1}{4\sqrt{3}} = \frac{P_i}{4\sqrt{6}V_{i\_min}}. \quad (5)$$

Semiconductor devices should be determined mainly based on the power capacity requirements. For the proposed rectifier, the switches are selected according to the peak voltage stresses and RMS currents flowing through them. The RMS current of the boost diodes can be expressed as follows:

$$I_{D\_rms} = \frac{P_i}{6V_{i\_min}} \sqrt{\frac{4\sqrt{2}V_{i\_min}}{\pi V_o}}. \quad (6)$$

Given that the rectifier operates in CrM, no reverse recovery issue exists for the boost diodes. Therefore, only conduction losses should be considered.

The RMS current flowing through the MOSFET of each phase is given by

$$I_{S\_rms} = \frac{P_i}{\sqrt{3}V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}}. \quad (7)$$

Considering that each boost phase operates only for the half line cycle, the RMS currents of blocking slow diodes are calculated in the same manner as the inductor current as follows:

$$I_{SD\_rms} = \frac{\sqrt{6}P_i}{12V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}}. \quad (8)$$

With a forward voltage drop  $V_F$  across the slow diode, the power loss of the diode can be calculated by

$$P_{SD} = \frac{\sqrt{6}P_i}{12V_{i\_min}} \sqrt{1 - \frac{8\sqrt{2}V_{i\_min}}{3\pi V_o}} V_F. \quad (9)$$

Assuming a resistive load, the ripple current in the output capacitor is the combination of the twice-line-frequency ripple current and high-switching-frequency ripple current, which are typically used to select high-voltage electrolytic output capacitors. The RMS current that flows through the output capacitor is given by

$$I_{Crms} = \sqrt{I_{Crms\_LF}^2 + I_{Crms\_HF}^2}, \quad (10)$$

$$I_{Crms\_LF} = \frac{P_o}{\sqrt{2}V_o}, \quad (11)$$

$$I_{Crms\_HF} = \sqrt{\frac{16\sqrt{2}P_i^2}{9\pi V_{i\_min} V_o} - I_o^2}, \quad (12)$$

where  $P_o$  is the rating output power and  $I_o$  is the rating output current.

The comparison study among the conventional CCM PFC, dual-boost PFC in CrM, and the proposed PFC rectifier are summarized in Table. I. Since the proposed converter is constructed by connecting two converters, in which each converter operates as an interleaved boost circuit in CrM, the

current stresses of each inductance winding and semiconductor devices are reduced significantly compared with those of the conventional single-phase boost PFC and bridgeless dual-boost PFC rectifiers.

The switching performance of the proposed circuit remains as the advantages of bridgeless topologies and interleaved converters, which results in low switching and conduction losses. The input current in the proposed PFC circuit flows through fewer power devices compared with that in conventional boost converters. Moreover, the peak inductor current is reduced to 50% of that of conventional bridgeless converters.

Although more power components are needed in the proposed circuit than in the other topologies, the power capacity requirements for these components are lower than those for the other two topologies under the same output power level. Consequently, the quantities and costs of the components in the proposed circuit are competitive among the compared topologies.

### B. Control Strategy Consideration

Current mode control has been widely used and provides many advantages such as improved load regulation and fast current protection. To control the proposed rectifier, a control scheme based on peak current mode control is employed. The simplified scheme of the power stage and controller is shown in Fig. 9.

The control block includes the current control loop, voltage control loop, pulse-width modulation (PWM) control, and interleaved phase management. Similar to the conventional peak current mode control, the controller exhibits the function of regulating output voltage in CrM, and operation frequency varies constantly with time.

As shown in Fig. 9, with a current loop inside the voltage control loop, the controller enables active correction of the input current waveforms by working properly in high frequencies, which causes the inductor current to follow the shape of the input voltage waveform. The current-control loop and voltage-control loop operate together to sample system total current  $i_S$  and output voltage  $V_o$ , respectively.

The multiplier operates as a gain modulator. One input of the modulator is the current signal that is proportional to the input full-wave-rectified voltage  $V_{AC}$ . Another input comes from the voltage error amplifier, which takes in  $V_o$  and compares it with reference voltage  $V_{ref}$ . These two signals are considered and compared to determine the gain that is applied to the input of the current control.

The current amplifier and comparator use information from the multiplier and compares it with a sample of output current  $i_S$  to adjust the duty cycle of the PWM control. Output current  $i_S$  is used as a fast feed-forward of the inside loop and functions as the ramp to the current PWM comparator.

The zero current detection (ZCD) blocks (ZCDA and

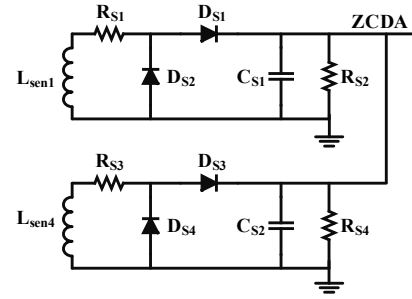


Fig. 10. Simplified ZCD circuit of the proposed circuit.

ZCDB) sense the multiphase inductor currents  $i_{L1}$  to  $i_{L4}$  and use the information as the reset signal to the PWM outputs. For CrM operation, the MOSFET is turned on when the valley of the inductor current is detected.

For each interleaved cell, two boost phases operate independently in an interactive phase approach, with each phase properly operating in CrM. Since two interleaved cells operate for each half line cycle, along with the inductors of one cell cross coupling with that of another cell, the ZCD of the multiphase inductors is significant. An effective and simple circuit is proposed to implement ZCD of the two phases from different interleaved cells. Fig. 10 shows the proposed ZCD circuit.

In this circuit, two current-sensing circuits of two legs from one coupled inductor are connected in parallel. During the positive half line period,  $L_{sen1}$  senses the inductor current of  $L_1$ .  $i_{Lsen1}$  is taken to the ZCDA port of the controller through  $D_{S1}$ . As the current of  $L_4$  is blocked,  $i_{Lsen4}$  becomes zero and is segregated from ZCDA by  $D_{S3}$ . Similarly, during the negative half line period,  $i_{Lsen4}$  is taken to the ZCDA port through  $D_{S3}$ , whereas  $i_{Lsen1}$  is segregated by  $D_{S1}$ . Thus, we can obtain the voltage of ZCDA port  $v_{ZCDA}$  as follows:

$$v_{ZCDA} = \begin{cases} i_{Lsen1} R_{S2}, & \text{positive line cycle} \\ i_{Lsen4} R_{S4}, & \text{negative line cycle} \end{cases} \quad (13)$$

The same results are obtained from the ZCDB circuit of another cell. Therefore, although four inductor channels exist in the power stage with two ZCD ports in the interleaved controller, the proposed circuit can effectively detect the inductor current valley of each channel. Thus, the interleaved boost bridgeless PFC circuit can be controlled by using the commercial interleaved PFC controller.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

### A. Simulation Results

A PSpice simulation model is developed to verify the analysis of the proposed PFC rectifier. The interleaving CrM PFC controller from Texas Instruments, Inc. (Texas, USA), UCC28063, is used as the system controller in the simulation. The simulation model is designed with the specifications shown in Table II.

TABLE II  
PARAMETERS OF THE SIMULATED POWER STAGE

Parameters	Symbol	Value
Input voltage	$V_{ac}$	85 V ~ 265 V
Line frequency	$f_L$	60 Hz
Output voltage	$V_o$	388 Vdc
Output power	$P_o$	600 W
Boost inductance	$L_1$ to $L_4$	210 $\mu$ H
Output capacitor	$C_{out}$	500 $\mu$ F

Fig. 11 illustrates the simulated switching waveforms of switches  $S_A$  and  $S_B$ .  $S_A$  and  $S_B$  are turned on under ZCS, whereas boost diodes  $D_1$  to  $D_4$  are turned off. Hence, minimal reverse recovery noise and significantly low switching losses can be achieved from the CrM principle.

The simulated interleaved inductor and output currents are shown in Fig. 12. The figure indicates that CrM operation is an efficient and cost-effective technique that does not require low reverse-recovery time diodes. Given that the two stages are operated out of phase, the current ripple is also significantly reduced. In particular, the RMS current within the bulk capacitor is dramatically reduced.

Fig. 13 presents the current waveforms of  $L_1$  and  $L_2$  of the conventional dual-boost bridgeless PFC rectifier shown in Fig. 2. The voltage waveforms across current-sensing resistor  $R_s$  are also measured. Based on inductor current waveforms, the undesired circulating current is significantly large, which causes considerable noise. Distortion of the current-sensing waveform is also serious in the conventional circuit. Furthermore, one of the magnetic cores becomes idle after a half line period, which leads to low component utilization.

For comparison, the current waveforms of switches  $S_A$  and  $S_B$ , as well as the current-sensing signal across  $R_s$  of the proposed circuit, under full-load conditions at 220 V line voltage are shown in Fig. 14. The input and output currents are also shown in this figure. As illustrated,  $S_A$  and  $S_B$  operate in the whole line cycle. Compared with Fig. 13, Fig. 14 shows no measurement error in the current-sensing signal, and the sensing noise is also reduced significantly.

The inductor current waveforms of the proposed circuit in whole line cycles are shown in Fig. 15. After a half line operation period, the inductor current becomes zero without a circulating loop.

The simulated waveforms of the input voltage, input current, and output voltage are shown in Fig. 16. The input current is in phase with the input voltage. The output voltage remains constant during the whole line period.

## B. Experimental Results

A 600 W experimental prototype circuit as shown in Fig. 17, is built and tested to verify the operation of the proposed circuit. The design specifications are the same as those for the simulation described in Table. II. The commercial interleaved

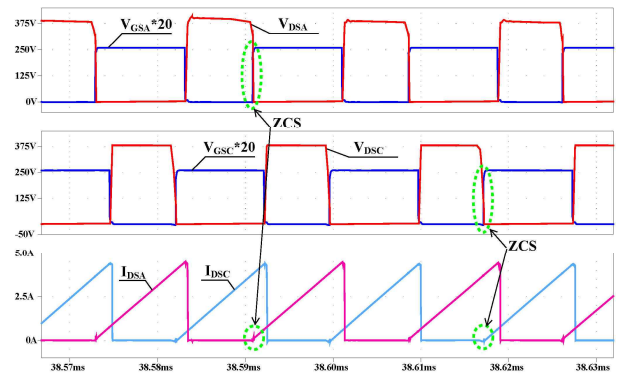


Fig. 11. Waveforms of driver signal  $V_{GS}$ , drain-to-source voltage  $V_{DS}$ , and drain-to-source current  $I_{DS}$  of  $S_A$  and  $S_B$ .

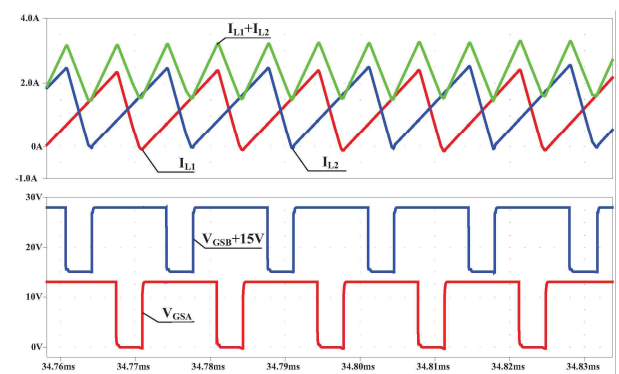


Fig. 12. Simulation results for the current waveforms of  $L_1$  and  $L_2$  with the driver signals of  $S_A$  and  $S_B$ .

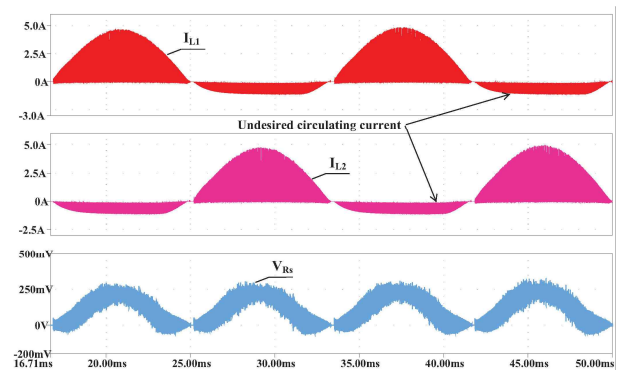


Fig. 13. Simulation waveforms of the dual-boost PFC circuit.  $I_{L1}$ ,  $I_{L2}$ : inductor current of  $L_1$  and  $L_2$ , respectively;  $V_{RS}$ : current sensing signal.

PFC controller, UCC28063, from Texas Instruments, Inc. (Texas, USA) is employed.

The experimental results of the proposed circuit are shown and analyzed as follows. The drain-to-source voltage waveforms of  $S_A$  and  $S_B$  are shown in Fig. 18. The switches operate in the whole line cycle, thereby improving component utilization. The voltage waveforms through  $D_5$  and  $D_6$  to the ground are shown in Fig. 19. The voltage waveforms of  $D_6$  and  $D_8$ , which are in two phases of one



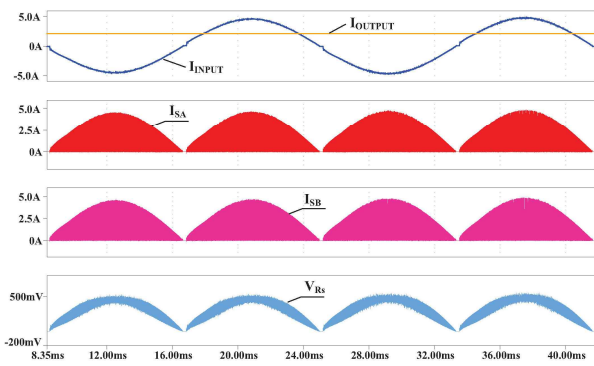


Fig. 14. Simulation waveforms of the input and output currents, switch current, and total current sensing signal of the proposed circuit.

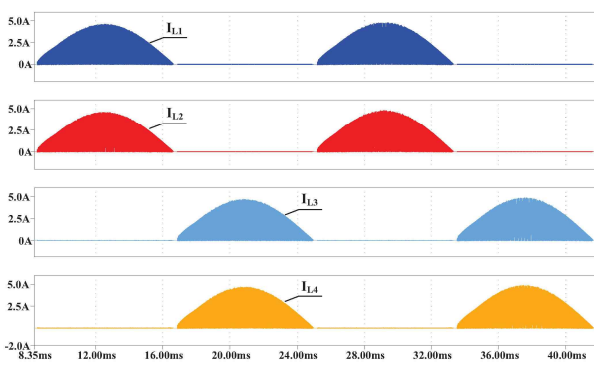


Fig. 15. Simulation inductor current waveforms of  $L_1$  to  $L_4$  in the proposed circuit

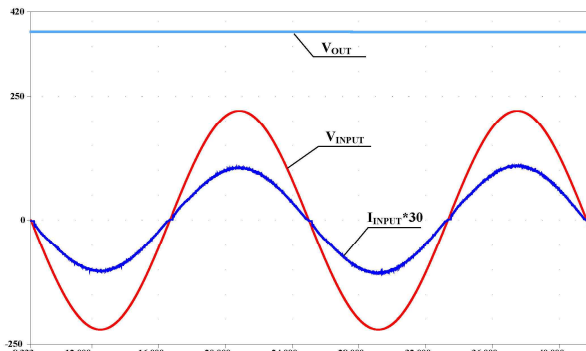


Fig. 16. Simulation waveforms of input voltage, input current, and output voltage

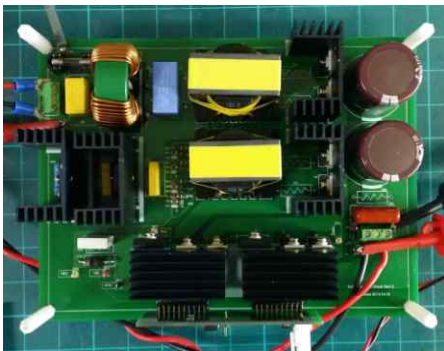


Fig. 17. Photograph of the prototype rectifier.

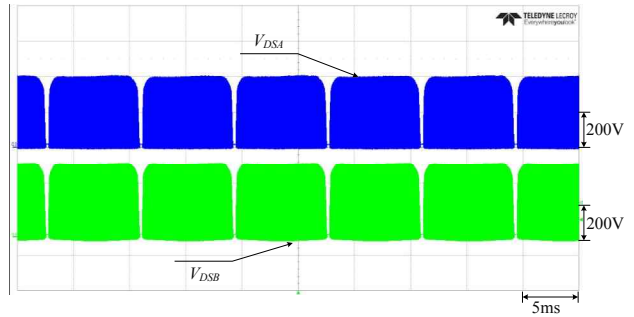


Fig. 18. Drain-to-source voltage waveforms of the switches.

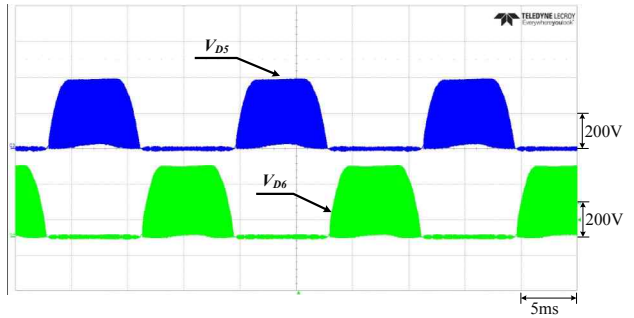


Fig. 19. Voltage waveforms across diodes  $D_5$  and  $D_6$

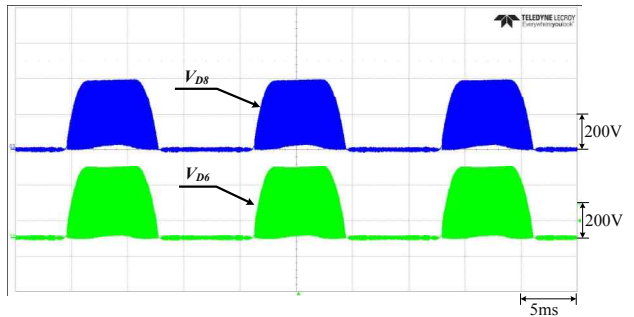


Fig. 20. Voltage waveforms across diodes  $D_6$  and  $D_8$

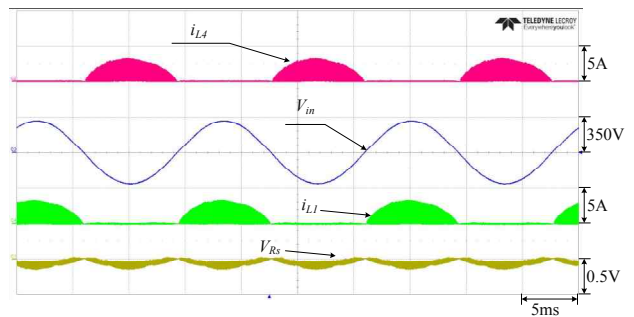


Fig. 21. Inductor current waveforms of  $L_1$  and  $L_4$  and the current-sensing signal.

interleaved cell, are shown in Fig. 20. Each diode operates in a half line period and blocks the current from other phases. Consequently, no undesired loop occurs during idle period. In addition, when operating in a half line period, the RMS current stresses of the diodes  $D_5 \sim D_8$  are low, and thus, less ideal devices can be used.

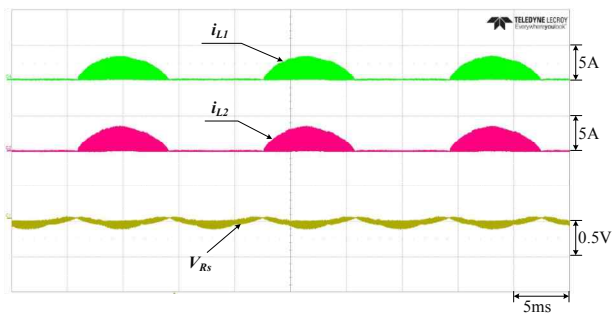


Fig. 22. Inductor current waveforms of  $L_1$  and  $L_2$  and the current-sensing signal.

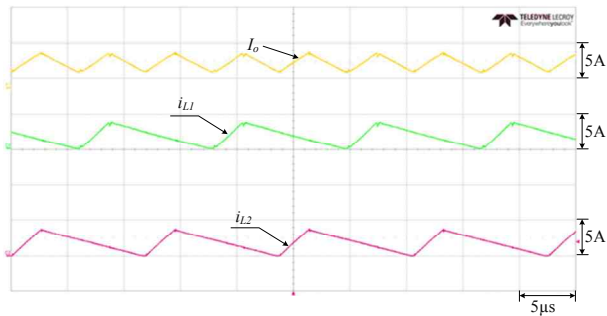


Fig. 23. Experimental current waveforms of  $L_1$  and  $L_2$ .

The current waveforms of  $L_1$  and  $L_4$  under full load and 220 V input voltage conditions are shown in Fig. 21. Although two inductors are coupled in a single magnetic core, the inductors are magnetically independent of each other, with  $L_1$  working in a positive half line cycle and  $L_4$  operating in a negative half line cycle. The sensing signal of system total current  $V_{RS}$  is also shown in the figure. Given the auxiliary blocking diodes, no undesired circulating current occurs in the inductor current loop. Therefore, the current-sensing signal can be more exact and stable than in the conventional circuit.

Fig. 22 shows the current waveforms of  $L_1$  and  $L_2$ . The two inductors operate in the same half line period in CrM. During the half line cycle, the two switches operate in interleaved mode, which is the same operation when using the conventional interleaved topology. However, the number of components in the current path is reduced by the bridgeless topology.

The sum inductor current and individual currents of  $L_1$  and  $L_2$  are shown in Fig. 23. Effective ripple frequency is increased twice, and peak-to-peak value input ripple current is significantly reduced compared with the two inductor current ripples because of the interleaved operation. Consequently, input filter size can be decreased. The boost phases also operate in CrM without reverse-recovery problems.

Fig. 24 shows the input current versus the input voltage at full load, as well as the output voltage. The input current is in phase with the input voltage and practically sinusoidal with

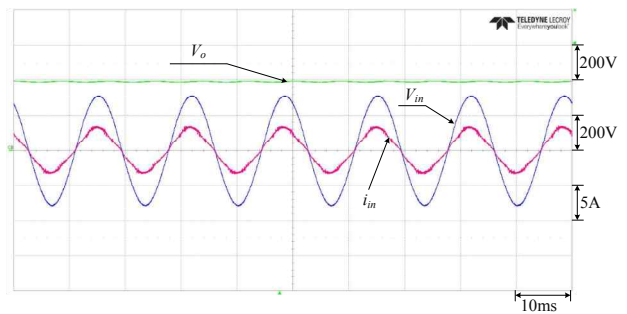


Fig. 24. Experimental results for the input voltage, input current, and output voltage at full load with 220 V input voltage.

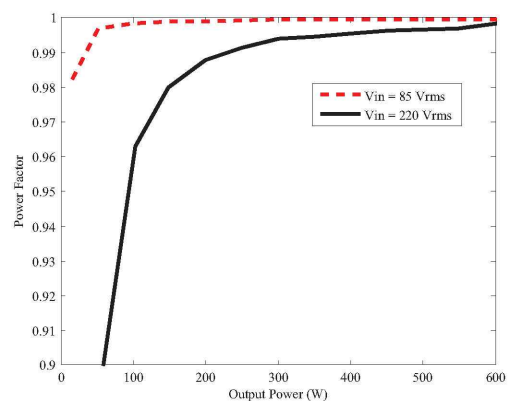


Fig. 25. Measured system power factor under different input voltages.

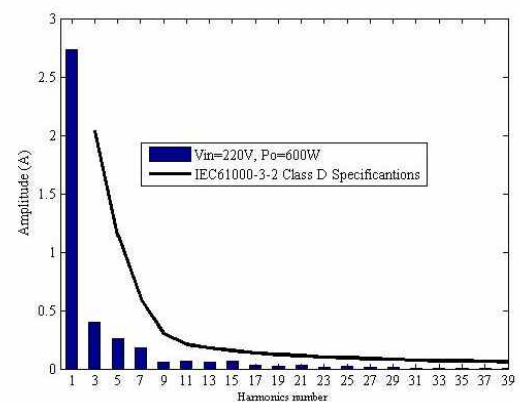


Fig. 26. Measured system THD under 220 V input voltage and full load conditions.

low THD and high PF. The output voltage is constant with low ripple.

The measured PFs of the proposed circuit under 85 V and 265 V input voltages are shown in Fig. 25. The proposed rectifier achieves high PF under 85 V, which is always higher than 99% from a 10% load to the full load. Under 265 V input voltage, the PF is higher than 99.6% under the rated load.

The measured THD of the proposed PFC under 220 V input voltage and full load is shown in Fig. 26. The proposed

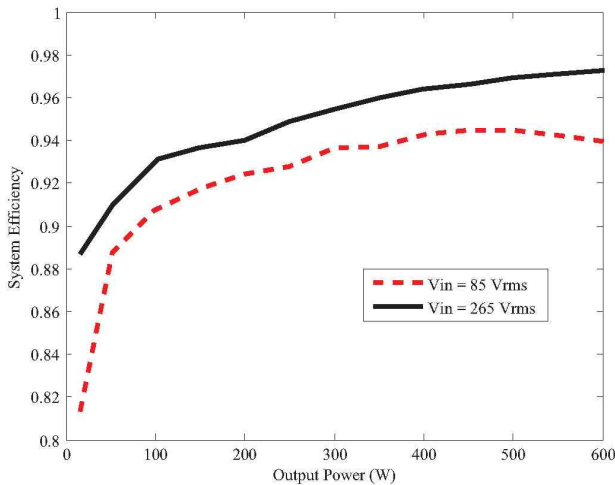


Fig. 27. Measured system efficiency under different input voltages.

rectifier achieves low THD, which can satisfy the IEC61000-3-2 Class D specifications.

Fig. 27 shows the measured efficiency curves of the proposed PFC converter. The efficiency at full load under 85 V is over 93%, and the maximum efficiency is 97.3%, which is achieved at full load and 265 Vac. Efficiency is improved at heavy load because the component number in the current flowing path is reduced.

## V. CONCLUSIONS

A novel bridgeless interleaved boost topology to overcome the serious drawbacks of conventional bridgeless PFC rectifiers is proposed in this study. The proposed circuit is compared with the conventional interleaved boost converter and bridgeless PFC topology that operate in CrM with soft switching. The proposed converter provides higher output power and lower current ripple than the other topologies. To verify the feasibility of the proposed converter, a 600 W prototype is designed and tested. The performance of the converter is also demonstrated by the simulation and experimental results. Nearly unity PF and low THD are achieved. Power efficiencies of 94.2% and 97.3% are obtained under 85 V and 265 V input voltages, respectively. Therefore, this implementation is a competitive candidate for high-power applications.

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