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Effect of Post Annealing in Oxygen Ambient on the Characteristics of Indium Gallium Zinc Oxide Thin Film Transistors

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Abstract: We have investigated the effect of electrical properties of amorphous InGaZnO thin film transistors (a-IGZO TFTs) by post thermal annealing in O_2 ambient.The post-annealed in O_2 ambient a-IGZOTFT is found to be more stable to be used for oxide-based TFT devices, and has better performance, such as the on/off current ratios, sub-threshold voltage gate swing, and, as well as reasonable threshold voltage, than others do. The interface trap density is controlled to achieve the optimum value of TFT transfer and output characteristics. The device performance is significantly affected by adjusting the annealing condition. This effect is closely related with the modulation annealing method by reducing the localized trapping carriers and defect centers at the interface or in the channel layer.

Keywords: a-IGZO, Oxide TFT, O_2 annealing, Interface trap density

1. INTRODUCTION

AOS (amorphous oxide-based semiconductor), TFTs (thin film transistors) are strong candidates for use in the active-matrix backplanes of next-generation displays because they overcome the limitations of amorphous and polycrystalline silicon TFTs. The a-IGZO has the excellent performances such as low temperature fabrication (R.T~), high mobility, visible region transparent, and reasonable on-off ratio. Furthermore, the low temperature process compared with other material makes TFT on flexible substrate (polymeric substrate) which allows applying the flexible active-matrix organic light emitting diode (AMOLED) [1-3]. Although the fabrication skills for oxide based TFTs great advanced, the insufficiency of explanation for their performance has made it difficult to fully understand their operation or degradation phenomena. For application to industrial products, electrical reliability as well as electrical properties, such as mobility, SS (sub-threshold swing), drain current on-off ratio ($I_{on/off}$), and so on, should be guaranteed to the required condition.

Thus, many studies have mainly focused on controlling the performance of the a-IGZO device, which is dependent on various susceptible parameters such as sputtering power and post-treatment [4-6]. The thickness of the channel layer can also be an important parameter to control device performance. Specifically, it can effectively enhance the switching behavior and threshold

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voltage (V_{th}) of TFTs through proper semiconductor resistance path adjustment [7,8]. The properties of a-IGZO TFTs are highly dependent on their oxygen content, but in an interactive way; this is because oxygen vacancies provide the needed free carriers for electrical conduction [9]. In fact, oxygen vacancy can be easily generated in the oxides. Therefore, the electrical properties cannot be controlled easily [10].

We have found that a post annealing in O_2 ambient on a-IGZO is described for the control of the threshold voltage parameter by varying annealing condition. This involves understanding how O_2 ratios influence the electronic properties and how the electronic behavior can be controlled.

2. EXPERIMENTAL

We have fabricated two type samples of the oxide-based TFT with IGZO channeal layer and heavily doped Si/SiO_2/IGZO capacitor of MOS structure, theelectrical properties are analyzed. The heavily doped Si/SiO_2/IGZO capacitor and a-IGZOTFT samples were fabricated by using the following process.

The gate insulator SiO_2 film was grown 20, 200 nm on heavily P-type(100) silicon wafers with 0.001 Ωcm resistivity by thermal oxidation method, respectively. Simultaneously, two types of substrates were loaded into a deposition sputter chamber, and then 50 nm IGZO films were directly deposited on the SiO_2/heavily doped Si wafers by rf-magnetron sputtering (SNTEK, Korea) from IGZO target (In : Ga : Zn = 2 : 2 : 1 mol%). The sputtering base pressure was under 5×10^{-6} torr.

The working pressure of sputtering chamber and rf-magnetron power was 3.5×10^{-3} torr and 50 W respectively. Then, the post annealing of the a-IGZO/SiO_2/heavily doping Si films was performed using a conventional furnace at 350 to 550℃ for 90 minutes with O_2 ambient, respectively. Finally, to fabricate a MOS capacitor, Al gate (dot size 2.3 × 10^{-4} cm^2) was thermally evaporated on the IGZO film using a shadow mask with circular dots.

Then, we deposited and patterned source and drain electrodes 100 nm Al metal on the a-IGZO channel layer using thermal evaporator for TFT. TEM (transmission electron microscopy) and AES (auger electron spectroscopy) were used to determine the thickness of the films and to investigate the interfacial layers formed between IGZO and SiO_2.

High frequency capacitance voltage (HF C-V) measurements were performed by using a Boonton 7,200 capacitance meter at 1 MHz. Current density voltage (J-V) curves were measured by stepping the voltage and measuring the current with a pico amper meter (pA meter, HP4145B, U.S.A).

3. RESULTS AND DISCUSSION

Figure 1 shows the variations in the AES depth profile curves obtained from the mixing of the In, Ga, Zn and oxygen atoms around the SiOx/IGZO interface region, after annealing at 350 and 450℃, respectively, with and without O_2 ambient.

The relevant elements in interfacial layer were investigated regarding their occurrence at various post annealing conditions, their bonding state and their behavior after post annealing process. This analysis indicated chemical compositions of the following relevant elements: In, Ga, Zn and oxygen. In the case of annealed in O_2 ambient clearly shows

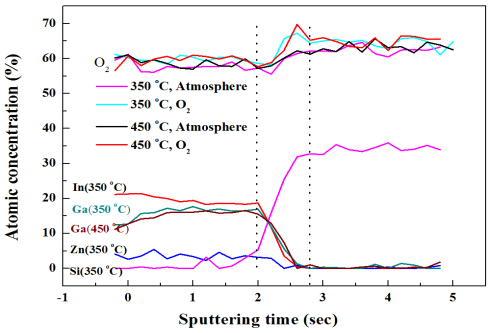

Fig. 1. AES depth profiles of a-IGZO/SiO_2 thin film with different post-annealing condition.

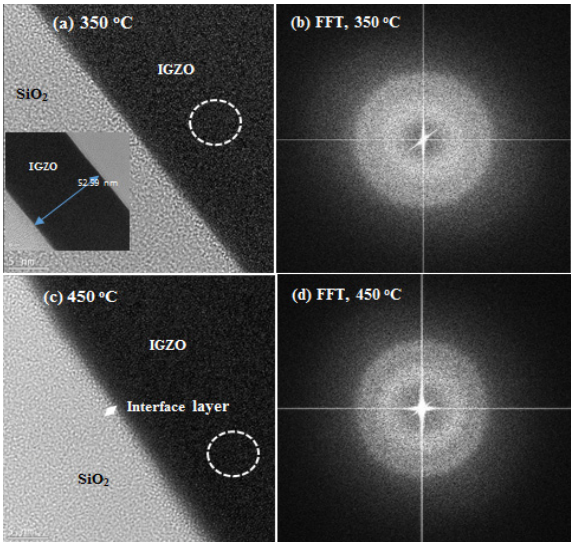

Fig. 2. Cross sectional High resolution TEM images and diffraction patterns of a FFT (fast fourier transform) images of IGZO thin films annealed at 350 and 450℃ in O_2 ambient, respectively.

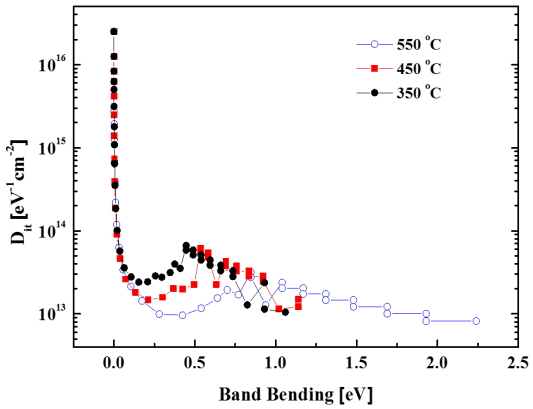

Fig. 3. The interface trap density with various post annealing condition extracted by Terman method.

that deep diffuses of oxygen atom in to the interfacial layer, and the concentration of Ga in the IGZO surface decreases with increasing post annealing temperature in O_2 ambient [11].

In addition, it can be noted that the annealed a-IGZO films are partially inter-diffused from IGZO bulk to the SiO_2 film. The diffusion of the a-IGZO films on SiO_2 interface is more easily when the film stacks are annealed at high temperatures. The AES depth profile also confirmed the concentration change of relevant elements, and the concentration of Ga atom in the IGZO bulk was decreased with the post annealing temperature is increasing. It should be noted that the relevant elements are diffused into the a-IGZO/SiO_2 interface. The thickness of a-IGZO/SiO_2 interface certainly increased with the increase of post annealing temperature. It can be assumed that the increase of the defect center by Ga-O bonding in the IGZO thin film with increasing of post annealing temperature is deteriorated of the electrical properties in the a-IGZO TFT [12].

Figure 2(a) and (c) high resolution TEM images of IGZO thin films annealed at 350 and 450℃ in O_2 ambient, respectively. (b) and (d) diffraction patterns of a fast Fourier transform (FFT) image of IGZO thin films annealed at 350 and 450℃, respectively.

As shown in the Fig. 2(a), the IGZO thin films have a thickness of about 52 nm and an amorphous-like phase. In the case of the sample annealed at 450℃, it is observed that a very small amount of crystallization occurs at the interface layer between SiO_2 gate insulator and IGZO thin film [13]. Thus the low density and small range of these crystals result in their producing diffraction peaks in the XRD measurements and diffraction pattern (notshowninthispaper). The weak crystalline growth by annealing condition is related to increases of free elections and oxygen vacancies at interface layer.

In addition, the growth of weak crystalline phase may be activated of oxygen radicals around the IGZO thin film by annealing temperature. As shown in the electrical results, the mobility of the IGZO thin films and the threshold voltage stability deteriorated by the annealing temperature increases. The AES results are in good agreement with the HRTEM (high-resolution TEM) images and diffraction patterns of the samples annealed at 450℃.

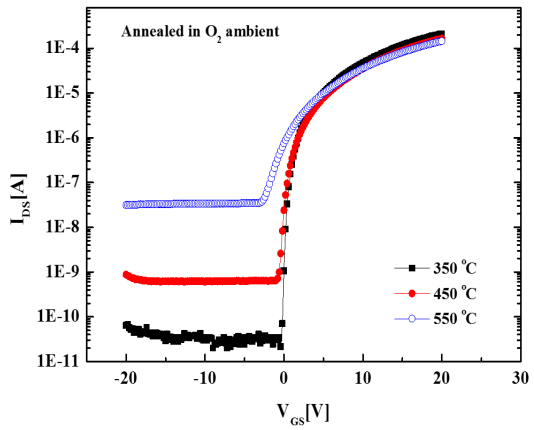

Fig. 4. The transfer curves of a-IGZO TFTs with different post-annealing conditions. The post annealing temperature for 350, 450, and 550℃, respectively, in O_2 ambient.

Figure 3 shows the interface trap density of IGZO/SiO_2 films with the various annealing conditions. The interface trap density in IGZO/SiO_2 films with annealing conditions (annealing temperature 350, 450, and 550℃ in O_2 ambient) was calculated by the Terman method [12], and the following values were found 6.5×10^{13}, 2.0×10^{13} and 1.0×10^{13} $cm^{-2}eV^{-1}\cdot cm^{-1}$ at 0.45 eV, respectively.

The distribution of interface trap density in the band gap for almost all samples is increased with the approaches to the shallow level. This is associated with the diffusion of the Ga and oxygen atoms during the post annealing process. Therefore, the change of interface trap density is due to the formation of the additional interface layer by the various annealing conditions.

This result indicates that the interface trap density in shallow level is strongly depending on temperature and controlled under O_2 ambient in thin film post annealing process. This clearly indicates that the temperature instability is more closely related with the variation of shallow trap density than deep level. Therefore, the interfacial properties of a-IGZO can result in a dominant effect on S.S and temperature stability, and, particularly,

Table 1. Electrical properties for various annealed conditions. The a-IGZO TFT shows the best electrical properties when annealed in O_2 ambient at 350℃.

Annealing condition (℃, O_2 ambient)	S.S ($V\cdot dec^{-1}$)	Mobility ($cm^2/V.s$)	On/off ratio	V_{th} (v)
350	0.15	4.5	8.0×10^6	0.1
450	0.26	3.4	3.8×10^6	-0.2
550	2.29	3.0	2.4×10^4	-2.1

$\triangle V_{th}$ can be controlled by the interface trap density in shallow level.

It could be explained that the effect of temperature treatment on the change of interfacial properties was caused by the difference of post annealing temperature and with O_2 ambient.

Figure 4 shows the transfer curves of a-IGZO TFTs with different post annealing conditions. Their electrical properties, such as V_{th}, μ_{FE}, $I_{on/off}$, and S.S were summarized in Table 1.

The sample annealed at 350℃ in O_2 ambient shows the highest on and off currents related to the high conductivity of the channel layer, leading to a high flow of electrons to pass through the source and drain. It is known that the off current is a function of the conductivity of the channel layer, according to the followed by the research [10]. Besides, the sample annealed at 350℃ with O_2 ambient also showed the best in S.S and $I_{on/off}$ (as presented in Table 1) compared to other samples. This meant that the interface trap density could be optimized the most compared to the other samples.

This may be due to compensated of oxygen vacancy between the IGZO bulk and the interfacial from table 1, The best S.S value of 0.15 $Vdec^{-1}$ was obtained for the sample annealed in 350℃ in O_2 ambient. We have known that all TFT parameters depend strongly on the trapped density at the insulator-semiconductor interface and inside the gate insulator. The μ_{FE} is reduced linearly, whereas off current increased with an increase of the annealing temperature [15].

The μ_{FE} value of the a-IGZO TFT after post annealing was significantly deteriorated compared to the best devices, which may be due to the extension of interfacial layer and the diffusion of In, Ga and oxygen atoms at interface layer.

4. CONCLUSIONS

The post annealing process is used to repair the interface traps on a-IGZO thin film and to reduce the channel bulk traps. The trap charge in the bulk compensated during the annealing process, which clearly shows that increasing the annealing temperature leads to a negatively shifted threshold voltage. The postannealed a-IGZO TFT in O_2 ambient at 350℃ is found to be more stable to be used for oxide-based TFT devices, and has better performance, such as the $I_{on/off}$, S.S, and, as well as reasonable V_{th}, than others do. The interface trap density is controlled to achieve the optimum value of TFT transfer and output characteristics. The mechanism to reduce the interface trap density by post annealing condition is explained by the decrease in carrier concentration due to the decrease in oxygen vacancies in the a-IGZO films.

Consequently, the annealing effect on a-IGZO TFT's electrical characteristics has been presented. This work is expected to be useful to further advance oxide-based TFT technology for future devices.

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