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Analysis of an Interleaved Resonant Converter for High Voltage and High Current Applications

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Abstract – This paper presents an interleaved resonant converter to reduce the voltage stress of power MOSFETs and achieve high circuit efficiency. Two half-bridge converters are connected in series at high voltage side to limit MOSFETs at $V_{in}/2$ voltage stress. Flying capacitor is used between two series half-bridge converters to balance two input capacitor voltages in each switching cycle. Variable switching frequency scheme is used to control the output voltage. The resonant circuit is operated at the inductive load. Thus, the input current of the resonant circuit is lagging to the fundamental input voltage. Power MOSFETs can be turn on under zero voltage switching. Two resonant circuits are connected in parallel to reduce the current stress of transformer windings and rectifier diodes at low voltage side. Interleaved pulse-width modulation is adopted to decrease the output ripple current. Finally, experiments are presented to demonstrate the performance of the proposed converter.

Keywords: Flying capacitor, DC converter.

1. Introduction

Power converters for medium or high power applications have been proposed and applied for many industry applications, such as fuel-cell power system [1], charge system [2] and ship power system [3]. For three-phase AC/DC power conversion systems, the front stage is a power factor corrector (PFC) and the second stage a DC/DC converter. The DC bus voltage of a three-phase PFC may be equal to 800V. In DC/DC converter, power MOSFETs with 900V voltage stress will result in high turn-on resistance. Three-level converters [4-9] with low voltage stress and high switching frequency have been presented in DC/DC converters for high voltage applications. Based on the neutral-point clamped diodes or flying capacitor, the voltage stress of active switches is clamped at $V_{in}/2$. However, two input split capacitor voltages maybe unbalanced and will increase the voltage stress of active switches beyond $V_{in}/2$. In [1] and [10], flying capacitor is adopted to the conventional three-level neutral point clamped converter to automatically balance two input capacitor voltages. Three-level zero voltage switching (ZVS) converters [11-17] have been presented to reduce the switching losses and increase the circuit efficiency. Pulse-width modulation (PWM) schemes are adopted to generate the PWM signals for active switches and to regulate output voltage. However, the ZVS condition of active switches is related to the load condition and input voltage so that it is difficult to implement ZVS turn-on for all switches over the entire load range. In order to extend the ZVS condition over the whole load range, resonant converters [18-22] have been proposed to achieve ZVS turn-on over the wide load range and input voltage variation. However, the ripple current at the output capacitor in resonant converter is higher than the output ripple current in the conventional half-bridge or full-bridge PWM converter. In order to limit the output ripple voltage in the desired ripple voltage specification, several capacitors are connected in parallel to reduce the resultant series equivalent resistance. Therefore, the large capacitance is normally adopted at the output side in the resonant converters. In order to reduce the output capacitance and output ripple current in the resonant converters, parallel resonant converter with interleaved PWM scheme has been presented in [23-25].

A new parallel resonant converter is presented for high input voltage and high load current applications. Two circuit modules connected in parallel in order to share load power and reduce the current stress of all passive and active power components. These two circuit modules are controlled with the phase shift of one-fourth switching period in order to reduce the ripple current at the output capacitor. Thus, the size of output capacitor can be reduced. In each circuit module, two half-bridge converters are connected in series at the primary side to reduce the voltage stress of each active switch at $V_{in}/2$. Flying capacitor is connected between two half-bridge converters such that two input capacitor voltages can be automatically balanced in each switching cycle. Series-parallel resonant tank is adopted in each half-bridge converter to achieve ZVS turn-on for all switches over the entire load range. Finally, experiments were provided to verify the performance of the proposed converter.

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2. Circuit Configuration

Fig. 1 gives the circuit configuration of the proposed converter for three-phase switching mode power supplies. The three-phase AC/DC converter with power factor correction is used in the front stage to reduce line current harmonics and provide a stable DC bus voltage for second stage DC/DC converter. The DC bus voltage is about 750V-800V for three-phase 480V utility input with power factor correction. The proposed parallel DC/DC converter with low voltage stress MOSFETs is adopted in the second stage for high load current applications. Two circuit modules are adopted in the proposed converter to share load current and reduce the current rating of active and passive components. The first circuit module includes $C_{in1}-C_{in2}$, C_{f1}, S_1-S_4, $C_{S1}-C_{S4}$, $C_{r1}-C_{r2}$, $L_{r1}-L_{r2}$, T_1-T_2, D_1-D_4 and C_o. In the same manner, the components of $C_{in1}-C_{in2}$, C_{f2}, S_5-S_8, $C_{S5}-C_{S8}$, $C_{r3}-C_{r4}$, $L_{r3}-L_{r4}$, T_3-T_4, D_5-D_5 and C_o are included in the circuit module 2. C_{in1} and C_{in2} are two input capacitances. $C_{r1}-C_{r4}$ are the series resonant capacitances. $L_{r1}-L_{r4}$ are the series resonant inductances. $L_{m1}-L_{m4}$ are the magnetizing inductances of transformers T_1-T_4, respectively. D_1-D_8 are the rectifier diodes and T_1-T_4 are the isolated transformers. C_{f1} and C_{f2} are the flying capacitances. Each circuit module includes two resonant converters with half-bridge converter leg. In circuit module 1, the first resonant converter includes the components of S_1, S_2, C_{r1}, L_{r1}, T_1, D_1, D_2 and C_o. The second resonant converter includes S_3, S_4, C_{r2}, L_{r2}, T_2, D_3, D_4 and C_o. C_o is the output capacitance. The primary sides of two resonant converters are connected in series in order to limit the voltage stress of each active switch at $V_{in}/2$. Active switches S_1 and S_3 have the same PWM waveforms. In the same manner, S_2 and S_4 have the same PWM signals. However, the PWM waveforms of S_1 and S_2 are complementary each other to avoid the short circuit in each half-bridge leg. In order to balance two input capacitor voltages v_{Cin1} and v_{Cin2}, C_{f1} is connected between the AC terminals b and c and C_{f2} is connected between the AC terminals f and g. If S_1 and S_3 are in the on-state and S_2 and S_4 are in the off-state, then $v_{Cf1}=v_{Cin1}$. On the other hand, $v_{Cf1}=v_{Cin2}$ if S_2 and S_4 are in the on-state. Since each active switch has the equal turn-on time, the flying capacitor voltage can be derived as $v_{Cf1}=v_{Cf2}=v_{Cin1}=v_{Cin2}=V_{in}/2$ and two capacitor voltages v_{Cin1} and v_{Cin2} are automatically balanced in each switching cycle. The frequency modulation scheme is used to regulate output voltage V_o. If the operated switching frequency is lower than the series resonant frequency, active switches S_1-S_8 are turned on at ZVS and rectifier diodes D_1-D_8 are turned off at ZCS. Thus, the switching losses of active switches are reduced and the reverse recovery problem of rectifier diodes is improved. In the proposed converter, each resonant converter supplies one-fourth of load

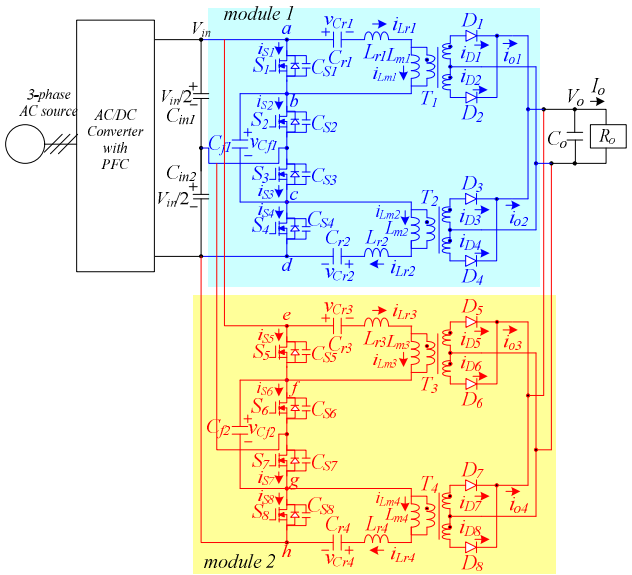


Fig. 1. Circuit configuration of the proposed converter with two circuit modules.

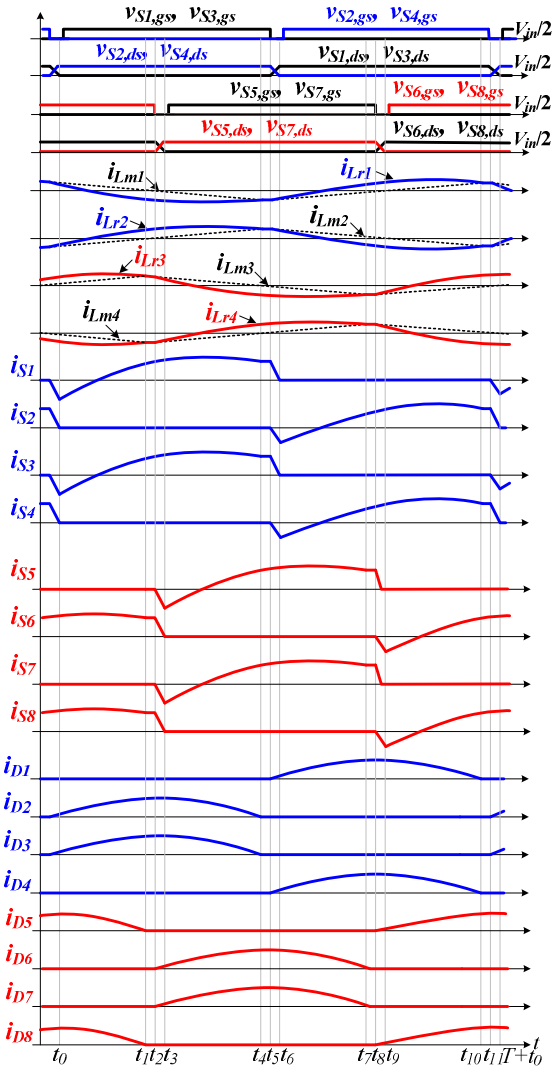


Fig. 2. Key waveforms of the proposed converter.

power to output load for the medium/high load current applications.

3. Operation Principle

The circuit operations of the proposed converter are discussed with the following assumptions to simplify the system analysis. (1) Transformers T_1-T_4 are identical with the same turns ratio $n=n_p/n_{s1}=n_p/n_{s2}$ and same magnetizing inductances $L_{m1}=L_{m2}=L_{m3}=L_{m4}=L_m$, (2) S_1-S_8 have the same output capacitance C_S, (3) $C_{in1}=C_{in2}$, (4) $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r$, and (5) $L_{r1}=L_{r2}=L_{r3}=L_{r4}=L_r$. The main PWM waveforms of the proposed converter during one switching cycle are given in Fig. 2. Due to the on/off conditions of switches S_1-S_8 and rectifier diodes D_1-D_8, the proposed converter has twelve operation modes in one switching period. The corresponding equivalent circuits of twelve operation modes are shown in Fig. 3. Before time t_0, S_1-S_4 are all turned off in circuit module 1. i_{Lr1} and i_{Lr2} are positive and negative, respectively. Therefore, C_{S1} and C_{S3} are discharged and C_{S2} and C_{S4} are charged. Since $i_{Lr1}<i_{Lm1}$ and $i_{Lr2}>i_{Lm2}$, diodes D_2 and D_3 are in the on-state. In circuit module 2, S_6 and S_8 are in the on-state and diodes D_5 and D_8 are conducting. L_{r3} and C_{r3} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr3}(t_0+T_s)$, and L_{r4} and C_{r4} are resonant with the applied voltage $nV_o-v_{Cr4}(t_0+T_s)$.

***Mode 1* [$t_0\le t<t_1$]:** At t_0, capacitances C_{S1} and C_{S3} are discharged to zero voltage in circuit module 1. Since i_{Lr1} and i_{Lr2} are positive and negative, respectively, the anti-parallel diodes of S_1 and S_3 are conducting. Therefore, S_1 and S_3 can be turned on at this moment to achieve ZVS. In this mode, $i_{Lr1}<i_{Lm1}$ and $i_{Lr2}>i_{Lm2}$. Thus, D_2 and D_3 are conducting and the magnetizing voltages $v_{Lm1}=-nV_o$ and $v_{Lm2}=nV_o$. The magnetizing current i_{Lm1} decreases with the slope of $-nV_o/L_m$ and i_{Lm2} increases with the slope of nV_o/L_m. In module 1, L_{r1} and C_{r1} are resonant with the applied voltage $nV_o-v_{Cr1}(t_0)$, L_{r2} and C_{r2} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr2}(t_0)$, and the flying capacitor voltage $v_{Cf1}=v_{Cin1}$. In module 2, S_6 and S_8 are turned on and D_5 and D_8 are in the on-state. L_{r3} and C_{r3} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr3}(t_0)$, L_{r4} and C_{r4} are resonant with the applied voltage $nV_o-v_{Cr4}(t_0)$, and the flying capacitor voltage $v_{Cf2}=v_{Cin2}$. The inductor currents $i_{Lr1}-i_{Lr4}$ and capacitor voltages $v_{Cr1}-v_{Cr4}$ in this mode are given as:

$$i_{Lr1}(t)=\frac{nV_o-v_{Cr1}(t_0)}{Z_r}\sin\omega_r(t-t_0)+i_{Lr1}(t_0)\cos\omega_r(t-t_0) \quad (1)$$

$$i_{Lr2}(t)=\frac{V_{in}/2-nV_o-v_{Cr2}(t_0)}{Z_r}\sin\omega_r(t-t_0)+i_{Lr2}(t_0)\cos\omega_r(t-t_0) \quad (2)$$

$$i_{Lr3}(t)=\frac{V_{in}/2-nV_o-v_{Cr3}(t_0)}{Z_r}\sin\omega_r(t-t_0)+i_{Lr3}(t_0)\cos\omega_r(t-t_0) \quad (3)$$

$$i_{Lr4}(t)=\frac{nV_o-v_{Cr4}(t_0)}{Z_r}\sin\omega_r(t-t_0)+i_{Lr4}(t_0)\cos\omega_r(t-t_0) \quad (4)$$

$$v_{Cr1}(t)=nV_o-[nV_o-v_{Cr1}(t_0)]\cos\omega_r(t-t_0)+i_{Lr1}(t_0)Z_r\sin\omega_r(t-t_0) \quad (5)$$

$$v_{Cr2}(t)=V_{in}/2-nV_o-[V_{in}/2-nV_o-v_{Cr2}(t_0)]\cos\omega_r(t-t_0)+i_{Lr2}(t_0)Z_r\sin\omega_r(t-t_0) \quad (6)$$

$$v_{Cr3}(t)=V_{in}/2-nV_o-[V_{in}/2-nV_o-v_{Cr3}(t_0)]\cos\omega_r(t-t_0)+i_{Lr3}(t_0)Z_r\sin\omega_r(t-t_0) \quad (7)$$

$$v_{Cr4}(t)=nV_o-[nV_o-v_{Cr4}(t_0)]\cos\omega_r(t-t_0)+i_{Lr4}(t_0)Z_r\sin\omega_r(t-t_0) \quad (8)$$

where $\omega_r=1/\sqrt{L_rC_r}$ and $Z_r=\sqrt{L_r/C_r}$. The inductor currents i_{Lr1} and i_{Lr4} decrease and i_{Lr2} and i_{Lr3} increase in this mode.

***Mode 2* [$t_1\le t<t_2$]:** At t_1, $i_{Lr3}=i_{Lm3}$ and $i_{Lr4}=i_{Lm4}$. Thus, D_5-D_8 are in the off-state. Since S_6 and S_8 are still in the on-state, C_{r3}, L_{r3} and L_{m3} are resonant with the applied voltage $V_{in}/2-v_{Cr3}(t_1)$ and C_{r4}, L_{r4} and L_{m4} are resonant with the applied voltage $-v_{Cr4}(t_1)$ in circuit module 2. The inductor currents $i_{Lr3}-i_{Lr4}$ and capacitor voltages v_{Cr3}-v_{Cr4} are expressed as:

$$i_{Lr3}(t)=\frac{V_{in}/2-v_{Cr3}(t_1)}{Z_p}\sin\omega_p(t-t_1)+i_{Lr3}(t_1)\cos\omega_p(t-t_1) \quad (9)$$

$$i_{Lr4}(t)=\frac{-v_{Cr4}(t_1)}{Z_p}\sin\omega_p(t-t_1)+i_{Lr4}(t_1)\cos\omega_p(t-t_1) \quad (10)$$

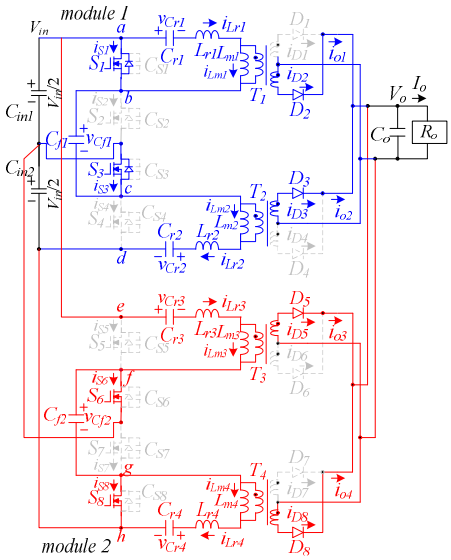
$$v_{Cr3}(t)=V_{in}/2-[V_{in}/2-v_{Cr3}(t_1)]\cos\omega_p(t-t_1)+i_{Lr3}(t_1)Z_p\sin\omega_p(t-t_1) \quad (11)$$

$$v_{Cr4}(t)=v_{Cr4}(t_1)\cos\omega_p(t-t_1)+i_{Lr4}(t_1)Z_p\sin\omega_p(t-t_1) \quad (12)$$

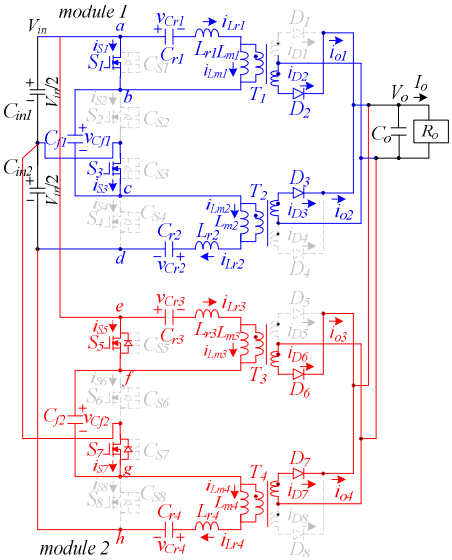
where $\omega_p=1/\sqrt{(L_r+L_m)C_r}$ and $Z_p=\sqrt{(L_r+L_m)/C_r}$. The operations of circuit module 1 in this mode are the same as the operation in mode 1.

***Mode 3* [$t_2\le t<t_3$]:** At t_2, S_6 and S_8 are turned off. Since $i_{Lr3}(t_2)$ and $i_{Lr4}(t_2)$ are positive and negative, respectively, C_{S6} and C_{S8} are charged and C_{S5} and C_{S7} are discharged in this mode. Diodes D_6 and D_7 are conducting. Thus, the magnetizing voltages $v_{Lm3}=-nV_o$ and $v_{Lm4}=nV_o$, and i_{Lm3} decreases and i_{Lm4} increases in this mode. If the energy stored in L_{r3} and L_{r4} is greater than the energy stored in $C_{S5}-C_{S8}$, then C_{S5} and C_{S7} can be discharged to zero voltage.

***Mode 4* [$t_3\le t<t_4$]:** At t_3, C_{S5} and C_{S7} are discharged to zero voltage. Since $i_{Lr3}(t_3)>0$ and $i_{Lr4}(t_3)<0$, the anti-parallel diodes of S_5 and S_7 are conducting. Therefore, S_5 and S_7


module 1
module 2

(a)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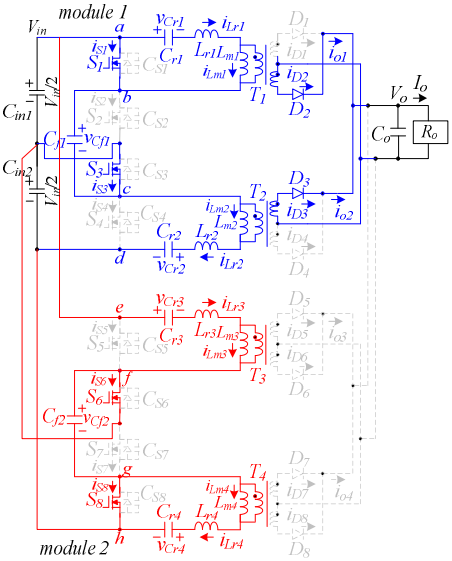
(d)


module 1
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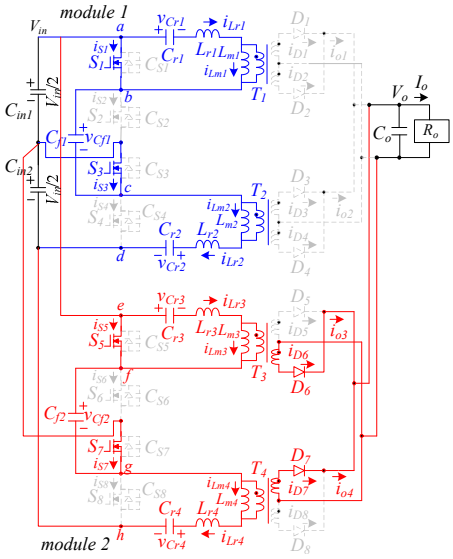
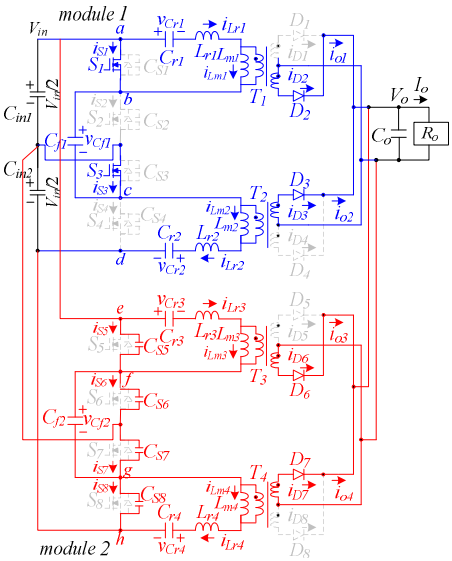
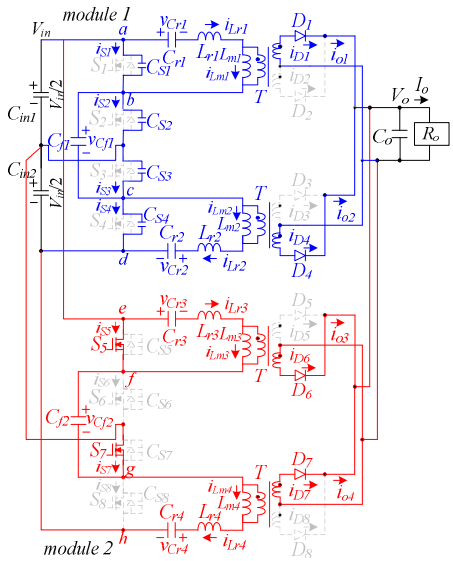
(b)


module 1
module 2

(e)


module 1
module 2

(c)


module 1
module 2

(f)

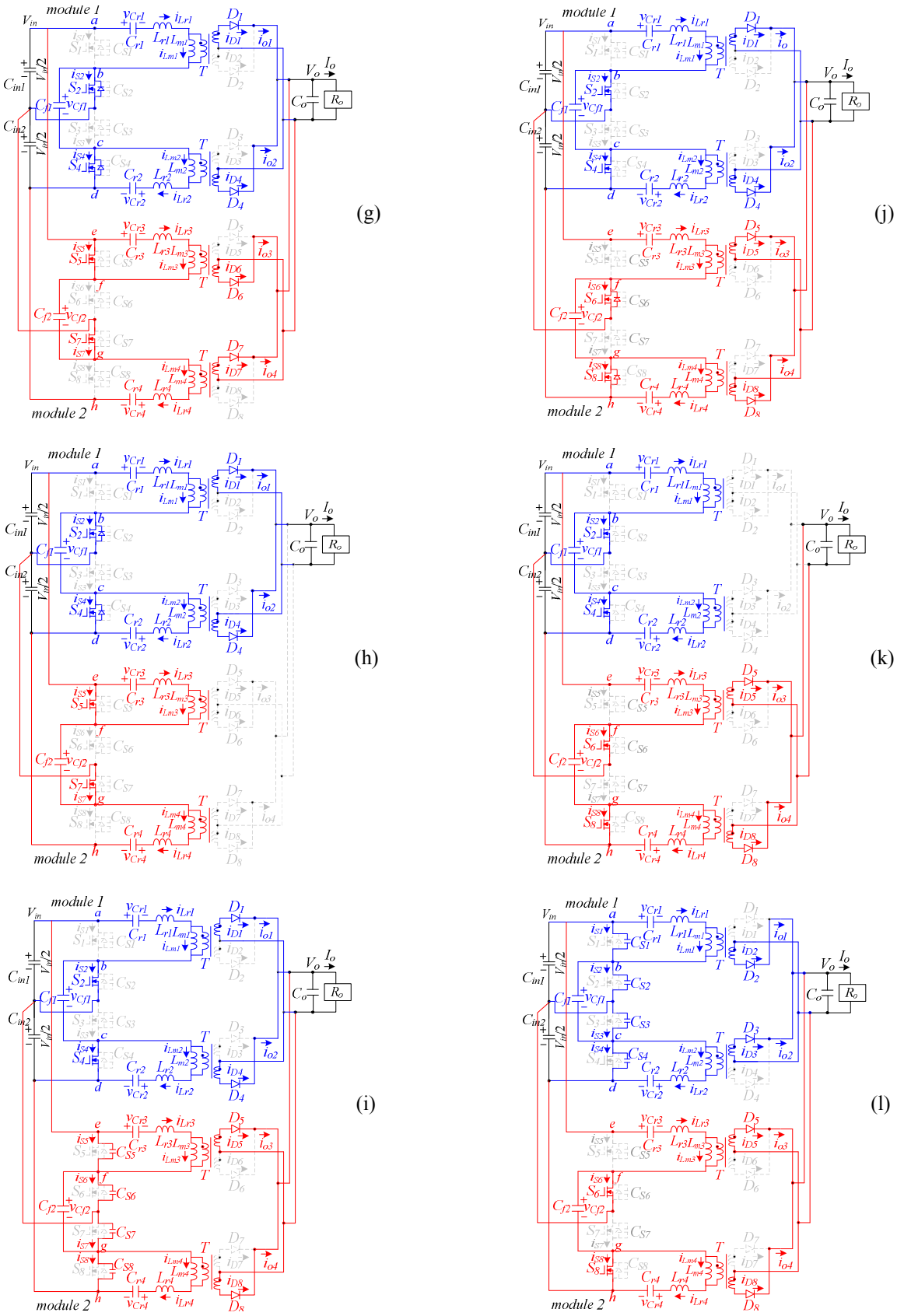


Fig. 3. Operation modes of the proposed converter during one switching cycle: (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10 (k) mode 11 (l) mode 12.

can be turned on at this moment to achieve ZVS. Diodes D_6 and D_7 are conducting so that $v_{Lm3}=-nV_o$ and $v_{Lm4}=nV_o$. In circuit module 2, L_{r3} and C_{r3} are resonant with the applied voltage $nV_o-v_{Cr3}(t_3)$ and L_{r4} and C_{r4} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr4}(t_3)$. The inductor currents i_{Lr3} and i_{Lr4} and the capacitor voltages v_{Cr3} and v_{Cr4} are expressed as:

$$i_{Lr3}(t)=\frac{nV_o-v_{Cr3}(t_3)}{Z_r}\sin\omega_r(t-t_3)+i_{Lr3}(t_3)\cos\omega_r(t-t_3) \quad (13)$$

$$i_{Lr4}(t)=\frac{V_{in}/2-nV_o-v_{Cr4}(t_3)}{Z_r}\sin\omega_r(t-t_3)+i_{Lr4}(t_3)\cos\omega_r(t-t_3) \quad (14)$$

$$v_{Cr3}(t)=nV_o-[nV_o-v_{Cr3}(t_3)]\cos\omega_r(t-t_3)+i_{Lr3}(t_3)Z_r\sin\omega_r(t-t_3) \quad (15)$$

$$v_{Cr4}(t)=V_{in}/2-nV_o-[V_{in}/2-nV_o-v_{Cr4}(t_3)]\cdot\cos\omega_r(t-t_3)+i_{Lr4}(t_3)Z_r\sin\omega_r(t-t_3) \quad (16)$$

***Mode 5* [$t_4\le t< t_5$]:** At t_5, $i_{Lm1}=i_{Lr1}$ and $i_{Lm2}=i_{Lr2}$. Thus, D_1-D_4 are all turned off. Components C_{r1}, L_{r1} and L_{m1} are resonant with the applied voltage $-v_{Cr1}(t_4)$ and C_{r2}, L_{r2} and L_{m2} are resonant with the applied voltage $V_{in}/2-v_{Cr2}(t_4)$. The inductor currents i_{Lr1} and i_{Lr2} and capacitor voltages v_{Cr1} and v_{Cr2} are given as:

$$i_{Lr1}(t)=\frac{-v_{Cr1}(t_4)}{Z_p}\sin\omega_p(t-t_4)+i_{Lr1}(t_4)\cos\omega_p(t-t_4) \quad (17)$$

$$i_{Lr2}(t)=\frac{V_{in}/2-v_{Cr2}(t_4)}{Z_p}\sin\omega_p(t-t_4)+i_{Lr2}(t_4)\cos\omega_p(t-t_4) \quad (18)$$

$$v_{Cr1}(t)=v_{Cr1}(t_4)\cos\omega_p(t-t_4)+i_{Lr1}(t_4)Z_p\sin\omega_p(t-t_4) \quad (19)$$

$$v_{Cr2}(t)=V_{in}/2-[V_{in}/2-v_{Cr2}(t_4)]\cos\omega_p(t-t_4)+i_{Lr2}(t_4)Z_p\sin\omega_p(t-t_4) \quad (20)$$

***Mode 6* [$t_5\le t<t_6$]:** At t_5, S_1 and S_3 are turned off and D_1 and D_4 are conducting. The magnetizing voltages $v_{Lm1}=nV_o$ and $v_{Lm2}=-nV_o$. Since $i_{Lr1}(t_5)<0$ and $i_{Lr2}(t_5)>0$, C_{S1} and C_{S3} are charged and C_{S2} and C_{S4} are discharged. C_{S2} and C_{S4} can be discharged to zero voltage if the energy stored in L_{r1} and L_{r2} is greater than the energy stored in $C_{S1}-C_{S4}$. At t_6, $v_{CS2}=v_{CS4}=0$. The anti-parallel diodes of S_2 and S_4 are conducting.

***Mode 7* [$t_6\le t<t_7$]:** At t_6, C_{S2} and C_{S4} are discharged to zero voltage in circuit module 1. Since $i_{Lr1}(t_6)<0$ and $i_{Lr2}(t_6)>0$, the anti-parallel diodes of S_2 and S_4 are conducting. Thus, S_2 and S_4 can be turned on at this moment to achieve ZVS. In module 1, L_{r1} and C_{r1} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr1}(t_6)$, L_{r2} and C_{r2} are resonant with the applied voltage $nV_o-v_{Cr2}(t_6)$, and the flying capacitor voltage $v_{Cf1}=v_{Cin2}$. The operation of circuit module 2 in this mode is the same as the operation in the previous mode.

***Mode 8* [$t_7\le t<t_8$]:** At t_7, $i_{Lr3}=i_{Lm3}$ and $i_{Lr4}=i_{Lm4}$. Thus, D_5-D_8 are all turned off. In circuit module 2, C_{r3}, L_{r3} and L_{m3} are resonant with the applied voltage $-v_{Cr3}(t_7)$ and C_{r4}, L_{r4} and L_{m4} are resonant with the applied voltage $V_{in}/2-v_{Cr4}(t_7)$. The operations of circuit module 1 in this mode are the same as the operation in the previous mode.

***Mode 9* [$t_8\le t<t_9$]:** At t_8, S_5 and S_7 are turned off. Since $i_{Lr3}(t_8)<0$ and $i_{Lr4}(t_6)>0$, C_{S6} and C_{S8} are discharged and C_{S5} and C_{S7} are charged in this mode. Diodes D_5 and D_8 are conducting. C_{S6} and C_{S8} can be discharged to zero voltage if the energy stored in L_{r3} and L_{r4} is greater than the energy stored in $C_{S5}-C_{S8}$.

***Mode 10* [$t_9\le t<t_{10}$]:** At t_9, C_{S6} and C_{S8} are discharged to zero voltage. Since $i_{Lr3}(t_9)<0$ and $i_{Lr4}(t_9)>0$, the anti-parallel diodes of S_6 and S_8 are conducting. Thus, S_6 and S_8 can be turned on under ZVS. In circuit module 2, L_{r3} and C_{r3} are resonant with the applied voltage $V_{in}/2-nV_o-v_{Cr3}(t_9)$ and L_{r4} and C_{r4} are resonant with the applied voltage $nV_o-v_{Cr4}(t_9)$.

***Mode 11* [$t_{10}\le t< t_{11}$]:** At t_{10}, $i_{Lm1}=i_{Lr1}$ and $i_{Lm2}=i_{Lr2}$. Thus, D_1-D_4 are all turned off. In circuit module 1, C_{r1}, L_{r1} and L_{m1} are resonant with the applied voltage $V_{in}/2-v_{Cr1}(t_{10})$ and C_{r2}, L_{r2} and L_{m2} are resonant with the applied voltage $-v_{Cr2}(t_{10})$. The operation of circuit module 2 is the same as the operation in the previous mode.

***Mode 12* [$t_{11}\le t<T_s+t_0$]:** At t_{11}, S_2 and S_4 are turned off and D_2 and D_3 are conducting. The magnetizing voltages $v_{Lm1}=-nV_o$ and $v_{Lm2}=nV_o$. Since $i_{Lr1}(t_{11})>0$ and $i_{Lr2}(t_{11})<0$, C_{S1} and C_{S3} are discharged and C_{S2} and C_{S4} are charged. C_{S1} and C_{S3} can be discharged to zero voltage if the energy stored in L_{r1} and L_{r2} is greater than the energy stored in $C_{S1}-C_{S4}$. At T_s+t_0, $v_{CS1}=v_{CS3}=0$. The anti-parallel diodes of S_1 and S_3 are conducting. Then, the operations of the proposed converter in a switching period are completed.

4. System Analysis

In this section, the system analysis of the proposed converter is presented. The duty cycle of each active switch is equal to 0.5. The pulse frequency modulation is adopted to regulate output voltage. The analysis of the proposed converter is based on the fundamental harmonic approach. The fundamental switching frequency is adopted to derive the system transfer function for each resonant converter. All harmonics of the switching frequency are neglected in the following discussion. The PWM signals of two circuit modules are interleaved by one-fourth of switching period. Each resonant circuit supplies one-fourth of load power to output load. Since the duty ratio of S_1-S_8 is equal to 0.5, the AC terminal voltages v_{ab}, v_{cd}, v_{ef} and v_{gh} are the square waveforms between 0 and $V_{in}/2$. The capacitor voltage $v_{Cf1}=v_{Cin1}$ in modes 1-5 and $v_{Cf1}=v_{Cin2}$ in

modes 7-11. The time periods in these two intervals are the same. Thus, the input capacitor voltages can be compensated and identical each other v_{Cin1}=v_{Cf1}=v_{Cin2}. Based on the Fourier series analysis, the AC terminal voltage v_{ab} can be expressed as:

$$\begin{aligned} v_{ab} &= \frac{V_{in}}{4} + \frac{V_{in}}{\pi}\sin(2\pi f_s t) + \sum_{n=3,5\ldots}\frac{V_{in}}{n\pi}\sin(2\pi n f_s t) \\ &= v_{ab,dc} + v_{ab,f} + v_{ab,h} \end{aligned} \quad (21)$$

where $v_{ab,dc}$, $v_{ab,f}$ and $v_{ab,h}$ are the dc component, fundamental frequency component and harmonic components of v_{ab}, respectively. The secondary side of resonant converter is driven by a quasi-sinusoidal current. If i_{Lr1}>i_{Lm1}, D_1 is conducting and the magnetizing voltage v_{Lm1}=nV_o. On the other hand, v_{Lm1}=$-nV_o$ if i_{Lr1}<i_{Lm1} and D_2 is conducting. The transformer primary voltage v_{Lm1} can be considered as a quasi-square waveform with $\pm nV_o$. The peak voltage of v_{Lm1} at the fundamental frequency is expressed as $\hat{v}_{Lm1,f} = 4nV_o/\pi$. The average output current of each center-tapped rectifier is equal to I_o/4 and the peak value of diode currents is given as $\hat{i}_{D1} = \hat{i}_{D2} = \pi I_o/8$. The load resistance reflected to the primary side of T_1 is given as $R_{ac,T1} = \hat{v}_{Lm1,f}/(\hat{i}_{D1}/n) = 32n^2R_o/\pi^2$. Therefore, the resonant tank by L_{r1}, C_{r1} and L_{m1} is excited by an effectively sinusoidal input voltage $V_{ab,f}$ and drives the effective AC resistive road $R_{ac,T1}$. Thus, the AC voltage gain of the resonant tank by L_{r1}, C_{r1} and L_{m1} at fundament frequency can be obtained as:

$$|G_{AC}(f)| = \frac{V_{Lm1,f}}{V_{ab,f}} = 1/\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2 + Q^2(\frac{f_s}{f_r}-\frac{f_r}{f_s})^2} \quad (22)$$

where $Q = \sqrt{L_{r1}/C_{r1}}/R_{ac,T1}$, $f_r = 1/2\pi\sqrt{L_{r1}C_{r1}}$, k=L_{r1}/L_{m1} and f_s is the switching frequency. At no-load condition (Q=0) and f_s=∞ condition, the AC voltage gain of each resonant converter is expressed as $|G_{AC}(f)|_{Q=0,f_s=\infty} \approx 1/(1+k)$. If the minimum DC voltage gain of the resonant converter is greater than $|G_{AC}(f)|_{Q=0,f_s=\infty}$, then the output voltage can be controlled from no load to full load condition.

5. Design Example and Experimental Results

A laboratory prototype was implemented with the following specifications: V_{in}=$750V-800V$, V_o=$24V$, I_o=$60A$, and resonant frequency f_r=120kHz. Transformers T_1-T_4 were implemented with TDK EER-42 magnertic core with A_e=194mm^2. The primary and secondary winding turns of T_1-T_4 are 48 turns and 6 turns, respectively. The minimum and maximum voltage gains of resonant converter are given as:

$$G_{DC,\min} = \frac{4n(V_o+V_f)}{V_{in,\max}} = \frac{4\times(48/6)\times(24+0.8)}{800} \approx 0.992 \quad (23)$$

$$G_{DC,\max} = \frac{4n(V_o+V_f)}{V_{in,\min}} = \frac{4\times(48/6)\times(24+0.8)}{750} = 1.058 \quad (24)$$

where V_f is the voltage drop on diodes D_1-D_8. At full load, the AC equivalent resistances $R_{ac,T1}-R_{ac,T4}$ are given as:

$$\begin{aligned} R_{ac,T1} &= R_{ac,T2} = R_{ac,T3} = R_{ac,T4} \\ &= 32\times(48/6)^2\times(24/60)/3.1416^2 \approx 83\Omega \end{aligned} \quad (25)$$

In this prototype, the inductance ratio k=L_{r1}/L_{m1} is selected as 1/8 and the quality factor Q at full load is selected as 0.3. Thus, the AC voltage gain of the proposed converter at no load condition (Q=0) is obtained as $|G_{AC}(f)|_{Q=0,f_s=\infty} \approx 0.889$. In (23), the minimum DC voltage gain $G_{DC,min}$ of the proposed converter is 0.992 and greater than the AC voltage gain at no load condition. Thus, the output voltage at no load condition can be controlled. From the given series resonant frequency f_r, the selected quality factor Q, the inductance ratio k and the AC equivalent resistance $R_{ac,T1}$, the series resonant inductances $L_{r1}-L_{r4}$, the magnetizing inductances $L_{m1}-L_{m4}$ and the resonant capacitances $C_{r1}-C_{r4}$ can be obtained as:

$$L_{r1} = L_{r2} = L_{r3} = L_{r4} = \frac{QR_{ac,T1}}{2\pi f_r} = \frac{0.3\times 83}{2\pi\times 120\times 10^3} \approx 33\mu H \quad (26)$$

$$L_{m1} = L_{m2} = L_{m3} = L_{m4} = L_{r1}/k = \frac{33\mu H}{1/8} \approx 264\mu H \quad (27)$$

$$C_{r1} = C_{r2} = C_{r3} = C_{r4} = \frac{1}{4\pi^2 L_{r1} f_r^2} \approx 53nF \quad (28)$$

Since two flying capacitors C_{f1} and C_{f2} are used to balance two input capacitor voltages V_{Cin1} and V_{Cin2}, the voltage stresses of S_1-S_8 can be limited at $V_{in,max}$/2.

$$v_{S1,stress} = V_{in,\max}/2 = 400V \quad (29)$$

The MOSFETs IRFP460 with 500V voltage stress and 20A current stress are adopted for active switches S_1-S_8. The voltage stress and average current of rectifier diodes D_1-D_8 are obtained as:

$$v_{D1,stress} = 2(V_o+V_f) = 2\times(24+0.8) = 49.6V \quad (30)$$

$$i_{D1,av} = I_{o,\max}/8 = 60/8 = 7.5A \quad (31)$$

The fast recovery diodes 30CPQ150 with 150V voltage stress, 30A current stress and 0.8V voltage drop are used for diodes D_1-D_8. The input capacitances C_{in1} and C_{in2} are 680nF/450V, the flying capacitances C_{f1} and C_{f2} are 680nF/630V, and the output capacitance C_o is 2820μF/100V ($6\times 470\mu F/100V$).

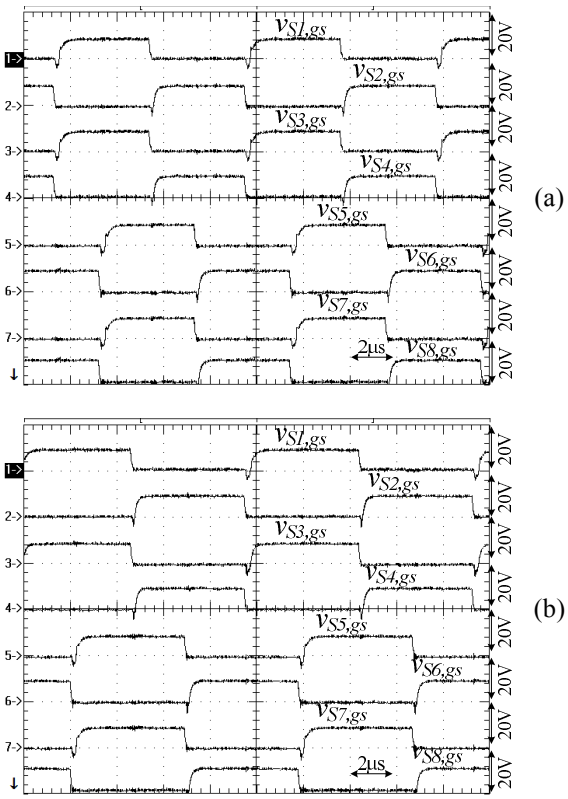


Fig. 4. Measured waveforms of the gate voltages $v_{S1,gs}$ − $v_{S8,gs}$ with V_{in}=800V and (a) 25% load (b) full load.

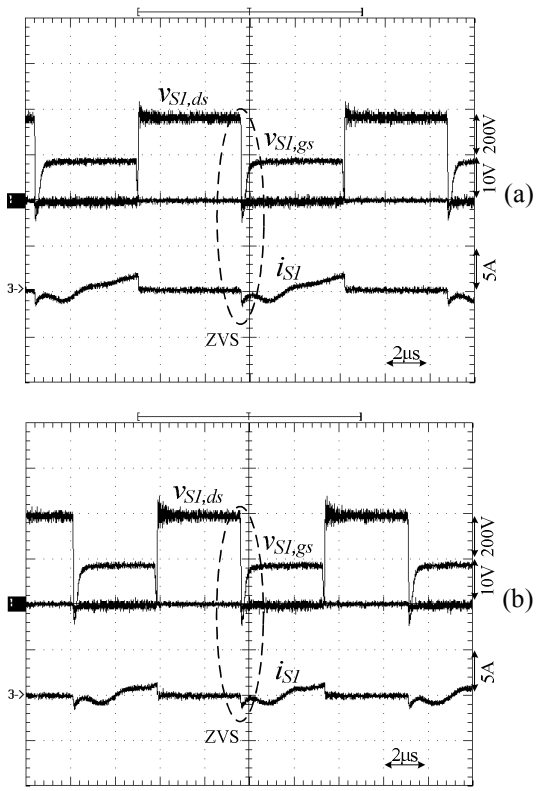


Fig. 5. Experimental results of gate voltage, drain voltage and drain current of switch S_1 at 5% load with (a) V_{in}=750V (b) V_{in}=800V.

A laboratory prototype with the circuit parameters derived in the previous section was implemented and tested to verify the effectiveness of the proposed converter. The measured gate voltages of $S_1 - S_8$ with input voltage V_{in}=800V and 25% load and full load are shown in Fig. 4. The PWM signals of $S_5 - S_8$ are phase-shifted one-fourth of switching period with respectively to PWM signals of $S_1 - S_4$, respectively. Fig. 5 gives the measured results of gate voltage, drain voltage and drain current of switch S_1 at 5% load with different input voltage cases. Before switch S_1 is turned on, the drain current is negative to discharge the drain-to-source capacitor. Thus, switch S_1 can be turned

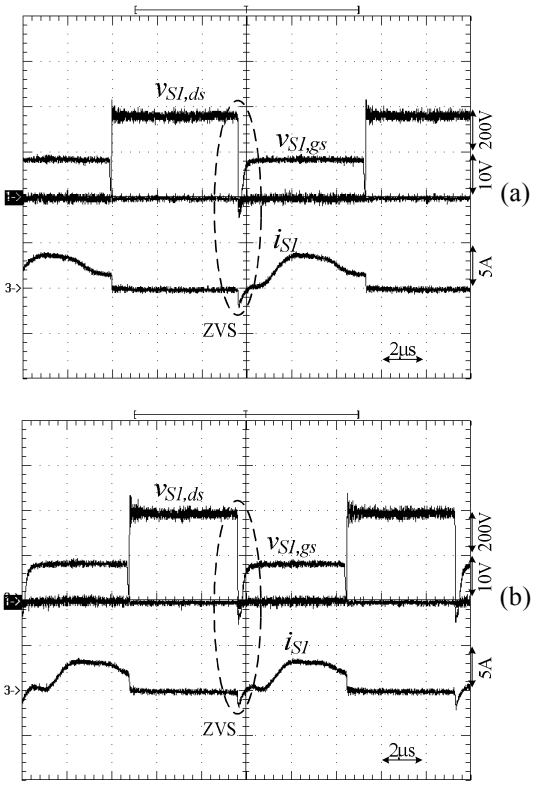


Fig. 6. Experimental results of gate voltage, drain voltage and drain current of switch S_1 at full load with (a) V_{in}=750V (b) V_{in}=800V.

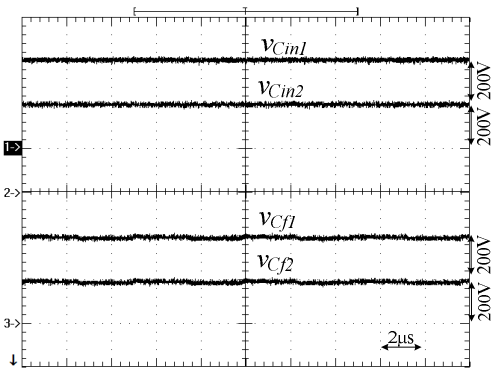


Fig. 7. Measured waveforms of two input capacitor voltages and two flying capacitor voltages at full load and V_{in}=800V.

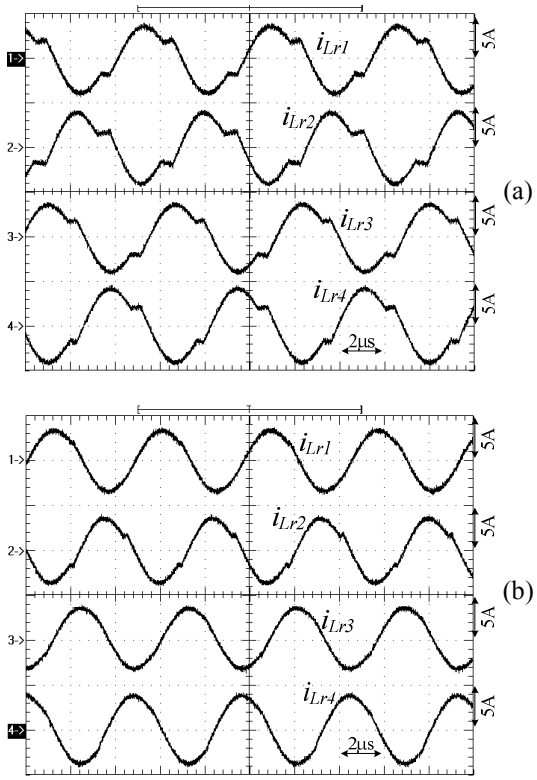


Fig. 8. Measured waveforms of inductor currents i_{Lr1} −i_{Lr4} at full load with (a) V_{in}=750V (b) V_{in}=800V.

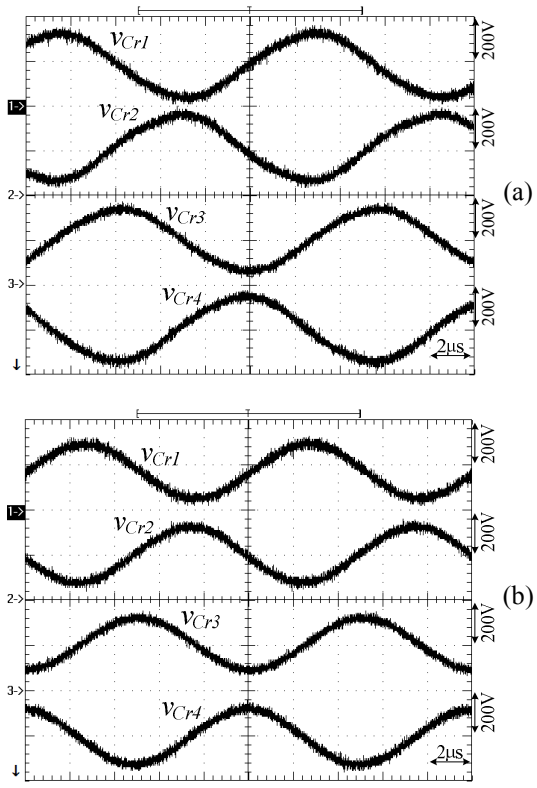


Fig. 9. Measured waveforms of resonant capacitor voltages v_{Cr1} −v_{Cr4} at full load with (a) V_{in}=750V (b) V_{in}= 800V.

on under ZVS when drain voltage is decreased to zero voltage. In the same manner, Fig. 6 shows the measured gate voltage, drain voltage and drain current of S_1 at full load and different input voltage conditions. From measured results shown in Figs. 5 and 6, S_1 is turned on at ZVS from 5% load to full load. Similarly, S_2 −S_8 can also be turned on under ZVS from 5% load to full load. Fig. 7 illustrates the measured waveforms of two input capacitor voltages and two flying capacitor voltages at full load and V_{in}=800V. Two input capacitor voltages and two flying capacitor voltages are all balanced at 400V. Fig. 8 gives the measured waveforms of inductor currents i_{Lr1} −i_{Lr4} at full load. Four inductor currents i_{Lr1} −i_{Lr4} are balanced. Fig. 9

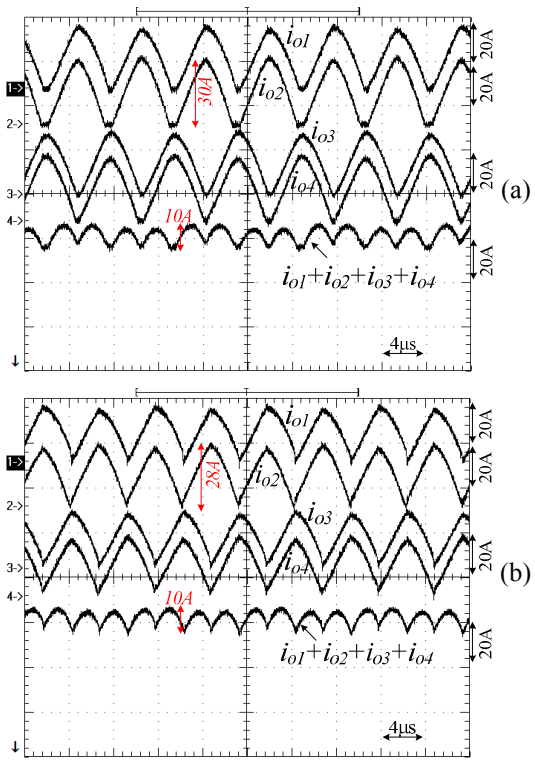


Fig. 10. Measured waveforms of the center-tapped rectifier output currents i_{o1}–i_{o4} at full load with (a) V_{in}= 750V (b) V_{in}=800V.

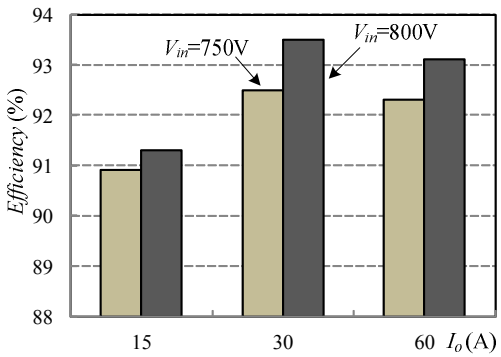


Fig. 11. Measured efficiencies of the proposed converter at different input voltage and load current conditions.

shows the measured waveforms of four resonant capacitor voltages $v_{Cr1}-v_{Cr4}$ at full load condition. Fig. 10 gives the test results of the rectifier output currents $i_{o1}-i_{o4}$ at full load condition. The rectifier output currents $i_{o1}-i_{o4}$ are almost balanced. It is clear that output currents i_{o3} and i_{o4} are phase-shifted one-half of switching cycle with respectively to i_{o1} and i_{o2}. The ripple current of i_{o2} is about 30A. However, the ripple current of the resultant output current $i_{o1}+i_{o2}+i_{o3}+i_{o4}$ is about 10A. The measured output ripple voltage is 2.1V at full load. Fig. 11 shows the measured circuit efficiencies of the proposed converter at different input voltage and load current conditions.

6. Conclusion

A new parallel resonant converter is presented for high input voltage and high load current applications. The main functions of the proposed converter are low voltage stress of MOSFETs, ZVS turn-on for all MOSFETs, no reverse recovery loss on rectifier diodes, low current rating of transformer windings and less ripple current on output capacitor. Two resonant circuit modules with interleaved PWM scheme are adopted in the proposed converter to reduce the current stress of active and passive components and reduce the ripple current at output side. In each circuit module, one flying capacitor is added between two half-bridge legs to balance two input capacitor voltages. Two resonant converters are connected in series in order to reduce the voltage stress of each MOSFET at $V_{in}/2$. The pulse frequency modulation scheme is used to regulate output voltage. The switching frequency is controlled to be less than the series resonant frequency so that MOSFETs can be turned on at ZVS and rectifier diodes can be turned off at ZCS. The switching loss of MOSFETs is reduced and the reverse recovery loss of rectifier diodes is overcome. Finally, experiments based on a laboratory prototype are provided to verify the effectiveness of the proposed converter.

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