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A Novel Single Phase Soft Switched PFC Converter

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Abstract – In this study, a novel single phase soft switched power factor correction (PFC) converter is developed with active snubber cell. The active snubber cell provides boost switch both to turn on with zero voltage transition (ZVT) and to turn off with zero current transition (ZCT). As the switching losses in the proposed converter are too low, L and C size can be reduced by increasing the operating frequency. Also, all the semiconductor devices operate with soft switching. There is no additional voltage stress in the boost switch and diode. The proposed converter has a simple structure, low cost and ease of control as well. It has a simple control loop to achieve near unity power factor with the aid of the UC3854. In this study, detailed steady state analysis of the proposed converter is presented and this theoretical analysis is verified by a prototype of 100 kHz and 500 W converter. The measured power factor and efficiency are 0.99 and 97.9% at full load.

Keywords: Power factor correction, AC-DC converter, Zero current transition, Zero voltage transion

Nomenclature

C_F	Output capacitor
C_p	Parasitic capacitor
C_s	Snubber capacitor
D_F	Boost diode
D_1	Body diode of the boost switch
D_2	Body diode of the auxiliary switch
$D_{3,4}$	Auxiliary diode
$D_{r1,r2,r3,r4}$	Rectifier diode
f_s	Switching frequency
i_{ac}	Line current
i_{DF}	Boost diode current
I_i	Input current
I_o	Output current
i_{Lsa}, i_{Lsb}	Snubber inductor current
i_{S1}	Boost switch current
L_F	Boost inductance
L_{sa}, L_{sb}	Snubber inductor
R_L	Load
S_1	Boost switch
S_2	Auxiliary switch
t_{f1}	Current fall time of boost switch
t_{r2}	Current rise time of auxiliary switch
t_{ZVT}	ZVT interval
t_{ZCT}	ZCT interval
v_{ac}	Line voltage
v_{Cp}	Parasitic capacitor voltage
v_{Cs}	Snubber capacitor voltage
V_{Csmax}	Maximum snubber capacitor voltage
v_{D3}	Auxiliary diode voltage
v_{S1}	Boost switch voltage
v_{S2}	Auxiliary switch voltage
V_i	Rectified input voltage
V_o	Output voltage
$Z_{1,2}$	Resonant impedance
$\omega_{1,2,3}$	Radial resonant frequency

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1. Introduction

AC-DC converters have been used in the power electronic systems and introduce harmonic currents from the ac mains. These harmonic currents cause some problems such as voltage distortion, poor power factor at input ac mains and noise. Single-phase power factor correction (PFC) topologies have been used in the power electronic systems to meet harmonic current limits defined by IEC 61000-3-2 [1-3].

The boost converter is the most popular topology for PFC applications because of their high power density, low-distorted input current, fast transient response and ease of control [4]. The boost PFC converter is operated in continuous conduction mode (CCM) at medium power level application [5].

A higher power density and faster transient response can be achieved by increasing switching frequency. However, as the switching frequency rises, switching losses and electromagnetic interference (EMI) noises increase. This aim can be realized by using the soft switching (SS) techniques implemented with snubber cells instead of hard switching (HS) techniques [6, 7]. SS techniques are based on Zero Voltage Switching (ZVS), Zero Current Switching (ZCS), Zero Voltage Transition (ZVT), and Zero Current Transition (ZCT) methods [8-20].

Recently, a lot of papers have been proposed to realize soft switching for the boost PFC converter. In the basic ZVT converter [8], the main switch turns on with ZVT perfectly with the help of a snubber cell. In the basic ZCT

converter [9], the main switch turns off under ZCS and ZVS with the help of a snubber cell. A lot of papers are developed to solve the problems in basic ZVT and ZCT converters [10-17]. In these methods, there are still some problems along with significant switching losses. In order to solve these problems, ZVT and ZCT converters which are formed by combining the ZVT and ZCT methods, are suggested in [18-20]. The main switch is turned on and off with exactly at zero voltage and zero current. Also, the auxiliary switch operates under by soft switching.

In this study, a novel single phase soft switched power factor correction (PFC) converter is developed with active snubber cell. The active snubber cell provides boost switch both to turn on with zero voltage transition (ZVT) and to turn off with zero current transition (ZCT). It has a simple control loop to achieve near unity power factor with the aid of the UC3854. The detailed steady state analysis of the proposed converter is presented and this theoretical analysis is verified by a prototype of 100 kHz and 500 W converter.

2. Operation Modes and Analysis

2.1 Definitions and assumptions

The proposed new single phase soft switched PFC converter circuit is shown in Fig. 1. In this circuit, v_{ac} is line voltage, i_{ac} is line current, D_{r1}-D_{r4} are rectifier diodes,

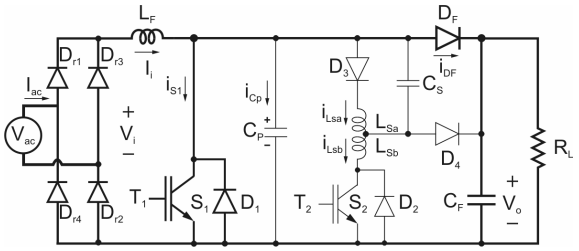

Fig. 1. Circuit scheme of the proposed converter

V_i is input voltage source, V_o is output voltage, L_F is boost inductor, C_F is output filter capacitor, S_1 is boost switch and D_F is boost diode. The boost switch consists of a boost transistor T_1 and its body diode D_1. In the soft switching circuit, S_2 is auxiliary switch, L_{sa} and L_{sb} are snubber inductors, C_s is snubber capacitor, D_3 and D_4 are auxiliary diodes. The snubber capacitor C_p is assumed to be the sum of the parasitic capacitor of S_1 and D_F.

In the steady-state analysis of the circuit, V_o and I_i are assumed constant for one switching cycle. Besides semiconductor devices and resonant circuits are assumed ideal. Also, the reverse recovery times of all diodes are not taken into account.

2.2 Operation stages

One switching period of the proposed new converter consist of 12 stages. The equivalent circuit diagrams of the operation stages are given in Fig. 2. The key waveforms

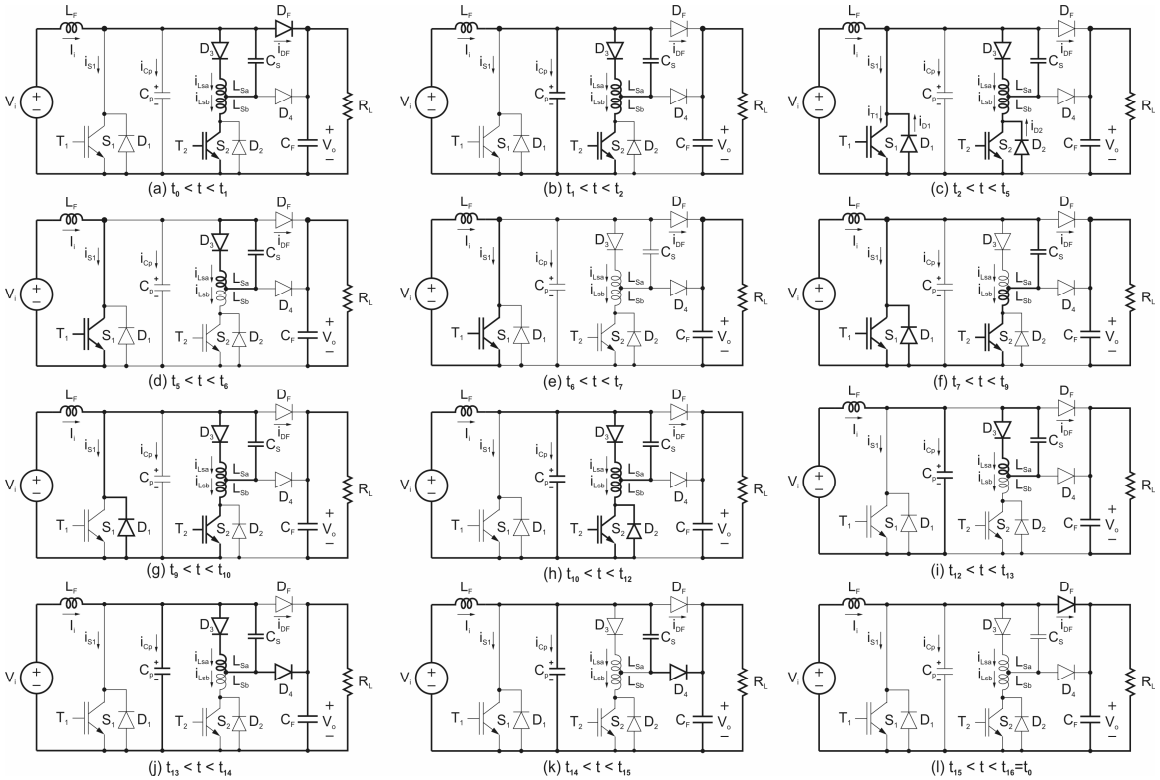

Fig. 2. Equivalent circuit schemes of the operation stages in the proposed converter

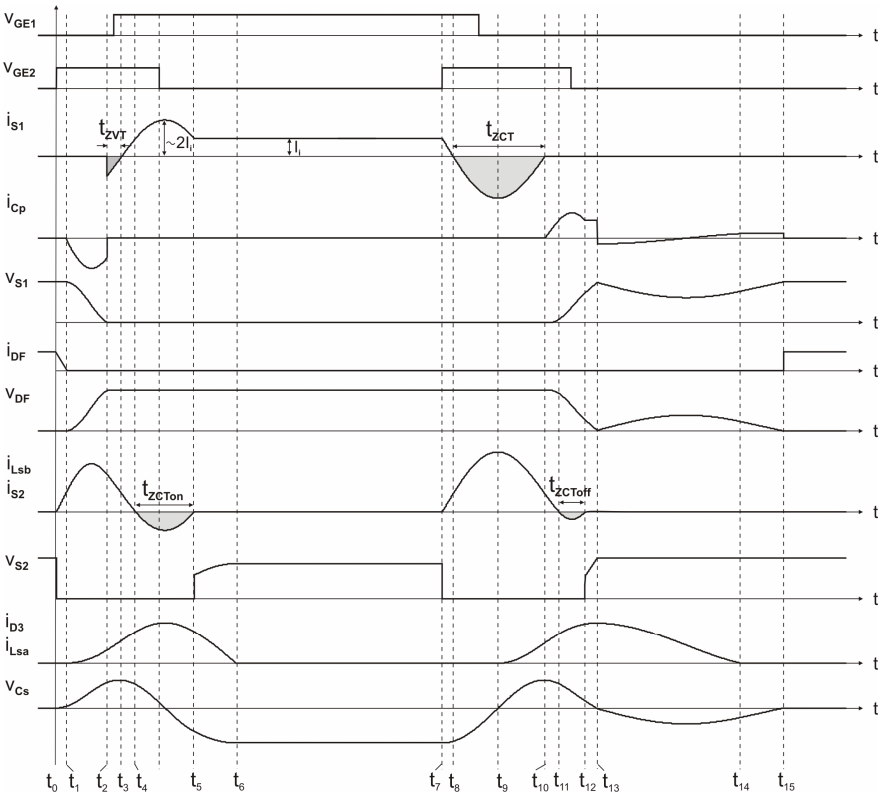

Fig. 3. The key waveforms of the proposed converter

concerning these stages are shown in Fig. 3. The detailed analysis of every stage of the proposed converter is presented below.

Stage 1 [$t_0<t<t_1$: *Fig. 2(a)*]: At $t=t_0$, $i_{T1}=0$, $i_{T2}=0$, $i_{DF}=I_i$, $i_{Lsa}=0$, $i_{Lsb}=0$ and $v_{Cs}=0$ are valid. At the beginning of this stage, D_F is in the on state and conducts the input current. S_1 and S_2 are in the off state. At $t=t_0$, when the control signal is applied to the gate of S_2, a resonance starts between L_{sa}, L_{sb} and C_s. Due to the resonance, C_s capacitor charges, S_2 current rises and D_F current falls simultaneously. For this stage, the following state equations can be written generally as,

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \tag{1}$$

$$L_{sb}\frac{di_{Lsb}}{dt}=V_o-v_{Cs} \tag{2}$$

$$C_s\frac{dv_{Cs}}{dt}=i_{Lsb}-i_{Lsa} \tag{3}$$

At $t = t_1$, i_{S2} reaches I_i and i_{DF} falls to zero and this stage is finished. Due to the series connected snubber inductance, S_2 and D_3 are turned on with ZCS. The boost diode D_F is turned off with nearly ZCS and ZVS. At the end of this mode,

$$i_{Lsa}=I_{Lsa1} \tag{4}$$

$$i_{Lsb}=I_{Lsb1}=I_i \tag{5}$$

$$v_{Cs}=V_{Cs1} \tag{6}$$

can be written.

Stage 2 [$t_1<t<t_2$: *Fig. 2(b)*]: At $t=t_1$, $i_{T1}=0$, $i_{T2}=I_i$, $i_{DF}=0$, $i_{Lsa}=I_{Lsa1}$, $i_{Lsb}=I_i$, $v_{Cs}=V_{Cs1}$ and $v_{Cp}=V_o$ are valid. S_1 and D_F are in the off state. S_2 is in the on state and conducts input current I_i.

At $t = t_1$, a resonance starts between C_p, L_{sa}, L_{sb} and C_s. i_{Lsa} and i_{Lsb} current rises and the capacitor voltage of v_{Cp} decreases by the resonance. For this stage, the following state equations can be written generally as,

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \tag{7}$$

$$L_{sb}\frac{di_{Lsb}}{dt}=v_{Cp}-v_{Cs} \tag{8}$$

$$C_s\frac{dv_{Cs}}{dt}=i_{Lsb}-i_{Lsa} \tag{9}$$

$$C_p\frac{dv_{Cp}}{dt}=I_i-i_{Lsb} \tag{10}$$

At $t = t_2$, v_{Cp} becomes 0 and the energy which is stored in the C_p, is transferred from capacitor to resonant circuit. At the same time, D_1 turns on with ZVS and this stage ends. At the end of this mode,

$$i_{Lsa}=I_{Lsa2} \tag{11}$$

$$i_{Lsb}=I_{Lsb2} \quad (12)$$

$$v_{Cs}=V_{Cs2} \quad (13)$$

can be written.

Stage 3 [$t_2<t<t_5$: *Fig. 2(c)*]: At the beginning of this stage, $i_{T1}=0$, $i_{T2}=I_{Lsb2}$, $i_{DF}=0$, $i_{Lsa}=I_{Lsa2}$, $i_{Lsb}=I_{Lsb2}$, $v_{Cs}=V_{Cs2}$ and $v_{Cp}=0$ are existent. In this mode, the resonant which is between L_{sa}, L_{sb} and C_s is still continued. For this stage,

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \quad (14)$$

$$L_{sb}\frac{di_{Lsb}}{dt}=-v_{Cs} \quad (15)$$

$$C_s\frac{dv_{Cs}}{dt}=i_{Lsb}-i_{Lsa} \quad (16)$$

are written. In this stage three different operation modes are occurred. At $t=t_2$, D_1 is turned on and conducts the excess of i_{Lsb} current from I_i. The interval of this mode is time for the boost switch S_1 to turn on with ZVT. It should be noted that the gate signal of S_1 must be applied during this time. As a result, S_1 will be turn on perfectly under ZVS and ZCS provided by ZVT. At $t=t_3$, i_{Lsb} drops to input current level and D_1 is turned off under ZCS. Just before D_1 is turned off, S_1 is turned on with ZVT. The boost switch current starts to rise and when it reaches to I_i, the current of S_2 becomes 0 at $t=t_4$. Just after $t=t_4$, D_2 is turned on. In the on state of D_2, the gate signal of S_2 is removed, so that S_2 is perfectly turned off under ZCT. This stage ends when i_{D2} is equal to zero at the instant t_5. At the end of this stage,

$$i_{Lsa}=I_{Lsa5} \quad (17)$$

$$v_{Cs}=V_{Cs5} \quad (18)$$

can be written.

Stage 4 [$t_5<t<t_6$: *Fig. 2(d)*]: This stage begins when D_2 turns off. At $t=t_5$, $i_{T1}=I_i$, $i_{T2}=0$, $i_{DF}=0$, $i_{Lsa}=I_{Lsa5}$, $i_{Lsb}=0$, $v_{Cs}=V_{Cs5}$ and $v_{Cp}=0$. While S_1 conducts input current, The current through the main transistor is equal to input current. At the same time, a resonance occurs through L_{sa}-C_s-D_3. For this resonance,

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \quad (19)$$

$$C_s\frac{dv_{Cs}}{dt}=-i_{Lsa} \quad (20)$$

are achieved. The energy in L_{sa} is transferred to C_s with this resonance. At $t=t_6$, L_{sa} current is equal to zero and the current direction change is blocked by D_3. v_{Cs} reaches its maximum level and this stage is finished. At the end of this mode,

$$v_{Cs}=V_{Cs6}=V_{Csmax}=\sqrt{{V_{Cs5}}^2+(Z_1 I_{Lsa5})^2} \quad (21)$$

can be written. Where

$$Z_1=\sqrt{\frac{L_{sa}}{C_s}} \quad (22)$$

Stage 5 [$t_6<t<t_7$: *Fig. 2(e)*]: In this stage, the boost switch S_1 conducts I_i and the auxiliary circuit is not active. This stage is the on state of the standard PWM boost converter. For this mode,

$$i_{S1}=I_i \quad (23)$$

can be written.

Stage 6 [$t_7<t<t_9$: *Fig. 2(f)*]: At the beginning of this stage, $i_{T1}=I_i$, $i_{T2}=0$, $i_{DF}=0$, $i_{Lsa}=0$, $i_{Lsb}=0$, $v_{Cs}=V_{Csmax}$ and $v_{Cp}=0$ are valid. At $t=t_7$, when the gate signal is applied to the S_2, a resonance starts between L_{sb} and C_s by the way of C_s-L_{sb}-S_2-S_1. For this stage, the following state equations can be written generally as,

$$L_{sb}\frac{di_{Lsb}}{dt}=-v_{Cs} \quad (24)$$

$$C_s\frac{dv_{Cs}}{dt}=i_{Lsb} \quad (25)$$

S_2 is turned on with ZCS through L_{sb}. The L_{sb} current rises and the boost switch current falls due to the resonance. At $t=t_8$, when i_{S2} reaches input current level, i_{S1} becomes zero. Just after this time, D_1 is turned on with ZCS and the current trough the boost switch is negative. If the gate signal of S_1 is removed, S_1 will turn off perfectly under ZVS and ZCS provided by ZCT. A new resonance occurs through the way of C_s-L_{sb}-T_2-D_1. D_1 conducts the excess of i_{Lsb} from I_i. At $t=t_9$, v_{Cs} voltage falls to zero and i_{Lsb} reaches its maximum value and this stage finishes. At the end of this mode,

$$i_{Lsb}=I_{Lsb9}=I_{Lsb\max}=\frac{V_{Cs\max}}{Z_2} \quad (26)$$

is valid. Here,

$$Z_2=\sqrt{\frac{L_{sb}}{C_s}} \quad (27)$$

Stage 7 [$t_9<t<t_{10}$: *Fig. 2(g)*]: At the beginning of this stage, $i_{T1}=0$, $i_{T2}=I_{Lsbmax}$, $i_{DF}=0$, $i_{Lsa}=0$, $i_{Lsb}=I_{Lsbmax}$, $v_{Cs}=0$ and $v_{Cp}=0$ are valid. At $t=t_9$, while v_{Cs} starts to be positive, the diode D_3 is turned on with ZCS. A new resonance is occurred between L_{sb}, L_{sa} and C_s. For this state,

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \quad (28)$$

$$L_{sb}\frac{di_{Lsb}}{dt}=V_o-v_{Cs} \quad (29)$$

$$C_s\frac{dv_{Cs}}{dt}=i_{Lsb}-i_{Lsa} \quad (30)$$

can be written. D_1 current becomes zero when i_{Lsb} falls again to I_i. At $t=t_{10}$, D_1 is turned off under ZCS and this stage ends. At the end of this mode,

$$i_{Lsa}=I_{Lsa10} \quad (31)$$
$$i_{Lsb}=I_{Lsb10}=I_i \quad (32)$$
$$v_{Cs}=V_{Cs10} \quad (33)$$

are valid. t_8-t_{10} is the on state time interval of D_1 and it is also equal to the ZCT time of the converter. The control signal of S_1 must be removed during this time and so the boost switch is turned off perfectly under ZCS and ZVS provided by ZCT.

Stage 8 [$t_{10}<t<t_{11}$: *Fig. 2(h)*]: At $t=t_{10}$, $i_{T1}=0$, $i_{T2}=I_i$, $i_{DF}=0$, $i_{Lsa}=I_{Lsa10}$, $i_{Lsb}=I_i$, $v_{Cs}=V_{Cs10}$ and $v_{Cp}=0$ are valid. Just after this time, a resonance occurs between C_p, L_{sa}, L_{sb} and C_s with the input current. The state equations are formed for this mode as follows.

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \quad (34)$$

$$L_{sb}\frac{di_{Lsb}}{dt}=v_{Cp}-v_{Cs} \quad (35)$$

$$C_s\frac{dv_{Cs}}{dt}=i_{Lsb}-i_{Lsa} \quad (36)$$

$$C_p\frac{dv_{Cp}}{dt}=I_i-i_{Lsb} \quad (37)$$

i_{Lsb} continues to decrease due to the resonance and becomes zero at $t=t_{11}$. The auxiliary switch current becomes negative. The control signal of S_2 must be removed during this interval, in which D_2 is in the on state. The auxiliary switch S_2 is turned off perfectly under ZCS and ZVS provided by ZCT. i_{S2} becomes zero at $t=t_{12}$ and this stage ends. At the end of this mode,

$$i_{Lsa}=I_{Lsa12} \quad (38)$$
$$v_{Cs}=V_{Cs12} \quad (39)$$
$$v_{Cp}=V_{Cp12} \quad (40)$$

are valid.

Stage 9 [$t_{12}<t<t_{13}$: *Fig. 2(i)*]: At the beginning of this stage, $i_{T1}=0$, $i_{T2}=0$, $i_{DF}=0$, $i_{Lsa}=I_{Lsa12}$, $i_{Lsb}=0$, $v_{Cs}=V_{Cs12}$ and $v_{Cp}=V_{Cp12}$ are valid. There are two different closed circuits for this interval. For the first one, C_p is charged linearly with I_i and the second one, a resonance occurs between L_{sa} and C_s via the path L_{sa}-C_s-D_3. For this mode,

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cs} \quad (41)$$

$$C_s\frac{dv_{Cs}}{dt}=-i_{Lsa} \quad (42)$$

$$C_p\frac{dv_{Cp}}{dt}=I_i \quad (43)$$

can be written. The sum of the v_{Cp} and v_{Cs} voltages becomes equal to output voltage at $t=t_{13}$. D_4 is turned on with ZVS and this mode is finished. At the end of this mode,

$$i_{Lsa}=I_{Lsa13} \quad (44)$$
$$v_{Cs}=V_{Cs13} \quad (45)$$
$$v_{Cp}=V_{Cp13} \quad (46)$$

are valid.

Stage 10 [$t_{13}<t<t_{14}$: *Fig. 2(j)*]: At $t=t_{13}$, $i_{T1}=0$, $i_{T2}=0$, $i_{DF}=0$, $i_{Lsa}=I_{Lsa13}$, $i_{Lsb}=0$, $v_{Cs}=V_{Cs13}$ and $v_{Cp}=V_o$-V_{Cs13} are existent. In this stage, a resonance between L_{sa}, C_s and C_p starts under the input current. At $t=t_{14}$, i_{Lsa} current becomes zero. This mode is finished. The energy stored in the L_{sa} is transferred to the capacitors and to the load. For this mode, the following equations are derived.

$$L_{sa}\frac{di_{Lsa}}{dt}=v_{Cp}-V_o \quad (47)$$

$$C_p\frac{dv_{Cp}}{dt}=I_i-i_{Lsa}-C_s\frac{d(v_{Cp}-V_o)}{dt} \quad (48)$$

Stage 11 [$t_{14}<t<t_{15}$: *Fig. 2(k)*]: At $t=t_{14}$, $i_{T1}=0$, $i_{T2}=0$, $i_{DF}=0$, $i_{Lsa}=0$, $i_{Lsb}=0$, $v_{Cs}=V_{Cs14}$ and $v_{Cp}=V_o$-V_{Cs14} are valid. C_p is charged linearly with I_i and C_s is discharged. For this mode,

$$C_p\frac{dv_{Cp}}{dt}=I_i-C_s\frac{dv_{Cs}}{dt} \quad (49)$$

$$v_{Cp}+v_{Cs}=V_o \quad (50)$$

can be written. v_{Cp} reaches V_o and v_{Cs} falls to 0 simultaneously at t_{15}. D_F is turned on with ZVS and D_{3} is turned off with ZVS, and this mode finishes.

Stage 12 [$t_{15}<t<t_{16}$: *Fig. 2(l)*]: At $t=t_{15}$, $i_{T1}=0$, $i_{T2}=0$, $i_{DF}=I_i$, $i_{Lsa}=0$, $i_{Lsb}=0$, $v_{Cs}=0$ and $v_{Cp}=V_o$ are valid. In this stage, the boost diode continues conducting the input current and the auxiliary circuit is not active. This stage is the off state of the PWM boost converter. For this mode,

$$i_{DF}=I_i \quad (51)$$

can be written.

At $t=t_{16}=t_0$, one switching period is completed by applying the control signal to boost switch again, and new switching period is started.

3. Converter Features

3.1 Main futures

The proposed converter is endowed with the active snubber cell which overcomes most of the drawbacks of the conventional PFC converter. Also, it has achieved nearly unity power factor at overall load range.

1) The boost switch is turned on with ZVT and turn off with ZCT, perfectly. The auxiliary switch is turned on with ZCS and turned off with ZCT
2) The boost switch is not subjected to any additional voltage stress. The current stress of main switch is at acceptable levels but this is the disadvantage of this converter.
3) The main diode is not subjected to any additional voltage and current stresses.
4) The soft switching operation of the new converter is maintained for the overall line and load ranges.
5) The converter can operate at considerably high frequencies and acts as a normal PWM converter. Also the circulating energy is quite small.
6) The sum of transient intervals is a very little part of the switching cycle.
7) Nearly unity power factor is achieved at full load condition and even light load condition.

3.2 Comparison of the proposed PFC converter and the PFC converter in [20]

In the proposed PFC converter, all semiconductor devices in the circuit are switched under soft switching. The boost switch is perfectly turned on and off with ZVT and ZCT, respectively. The auxiliary switch is turned on with ZCS and turned off with ZCT. But the PFC converter in [20], the boost switch and auxiliary switch are turned off with near ZVS. So that, the turn off switching losses are occurred in this case. As a result of this, the switching frequency can be selected higher than [20] and the efficiency of the proposed converter will be higher than [20]. The soft switching capabilities of the proposed converter and the PFC converter of [20] are summarized in the Table 1.

Table 1. Switching states

	Proposed PFC converter		PFC converter in [20]	
Device	Turn on	Turn off	Turn on	Turn off
Boost Switch	ZVT	ZCT	ZVT	near ZVS
Auxiliary Switch	ZCS	ZCT	ZCS	near ZVS
Boost Diode	ZVS	ZCS, ZVS	ZVS	ZVS

4. Design Procedure

A procedure for the design of the proposed converter is presented in this section. The design of the main power circuit can be found in any standard power electronics textbook so that only the design of the snubber circuit components is presented. In this study, the average control technique is used in the control circuit.

1) C_p is assumed to be the sum of parasitic capacitor of the main switch and the other parasitic capacitors incorporating it.
2) The t_{ZCT} interval must be chosen at least as fall time of the boost switch (t_{fl}).

$$t_{ZCT} \geq t_{fl} \tag{52}$$

3) In order to turn off the auxiliary switch with ZCT, the value of L_{sa} must be at least 2 times of L_{sb} value.

$$L_{sa} \geq 2L_{sb} \tag{53}$$

4) L_{sb} is selected to allow a current rise rate to be the maximum input current at most, within the auxiliary switch turn-on process and its current rise time.

$$\frac{V_o}{L_{sb}} t_{r2} \leq I_{i\max} \tag{54}$$

5) The value of C_s depends on the values of C_p, L_{sa} and L_{sb}. Also, the resonance current maximum value should be higher than the input current, the t_{ZCT} operation should be provided and the total resonance

Table 2. Some values of the components used in experimental circuit witching states

Component	Parameter	Value
Capacitors	C_s	WIMA MKP, 4.7nF/630V
	C_F	EPCOS, 440µF/450V
Inductors	L_F	500µH
	L_{sa}	4µH
	L_{sb}	2µH
Semiconductors	S_1	IXGR50N60C2D1 (600V-40A)
	S_2	IXGP16N60C2D1 (600V-16A)
	D_F, D_3, D_4	DSEI8-06 (600V-8A)

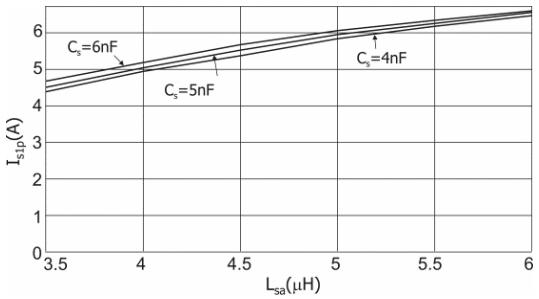

Fig. 4. Variation of maximum current through the main switch with snubber inductance L_{sa} for different snubber capacitor C_s

interval should not affect the PWM operation.

In order to give an idea about the selection of the components of the snubber cell, a design example is given below. Some values of the components used in experimental circuit are given in Table 2. According to design procedure and Table 2, snubber circuit components are determined. The capacitor C_p is assumed to be the sum of the parasitic capacitor of main switch and the other parasitic capacitors incorporating it. In the experimental circuit, C_p is approximately 1 nF. The L_{sb} value is selected as 2 µH from (54). L_{sa} is selected as 4 µH from (53). If the maximum value of the main switch current is assumed to be twice the input current, by using the characteristic curves shown in Fig. 4, the value of C_s is selected as 4.7 nF.

5. Experimental Results

The experimental circuit scheme of the converter is shown in Fig. 5.

The converter is to be designed according to the following specifications: output voltage V_o = 400 V, input voltage V_{ac}=85-265 V, output power P_o= 500 W, switching frequency f_s = 100 kHz. L_F boost inductance is designed to provide PFC and to operate in CCM. C_F output capacitor is selected to have constant voltage. The control circuit associated with the UC3854 integrated circuit is designed

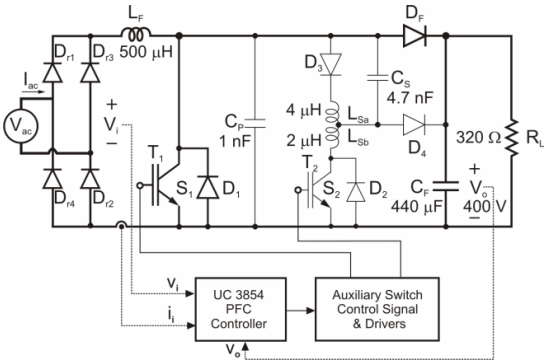

Fig. 5. Experimental circuit scheme of the proposed converter

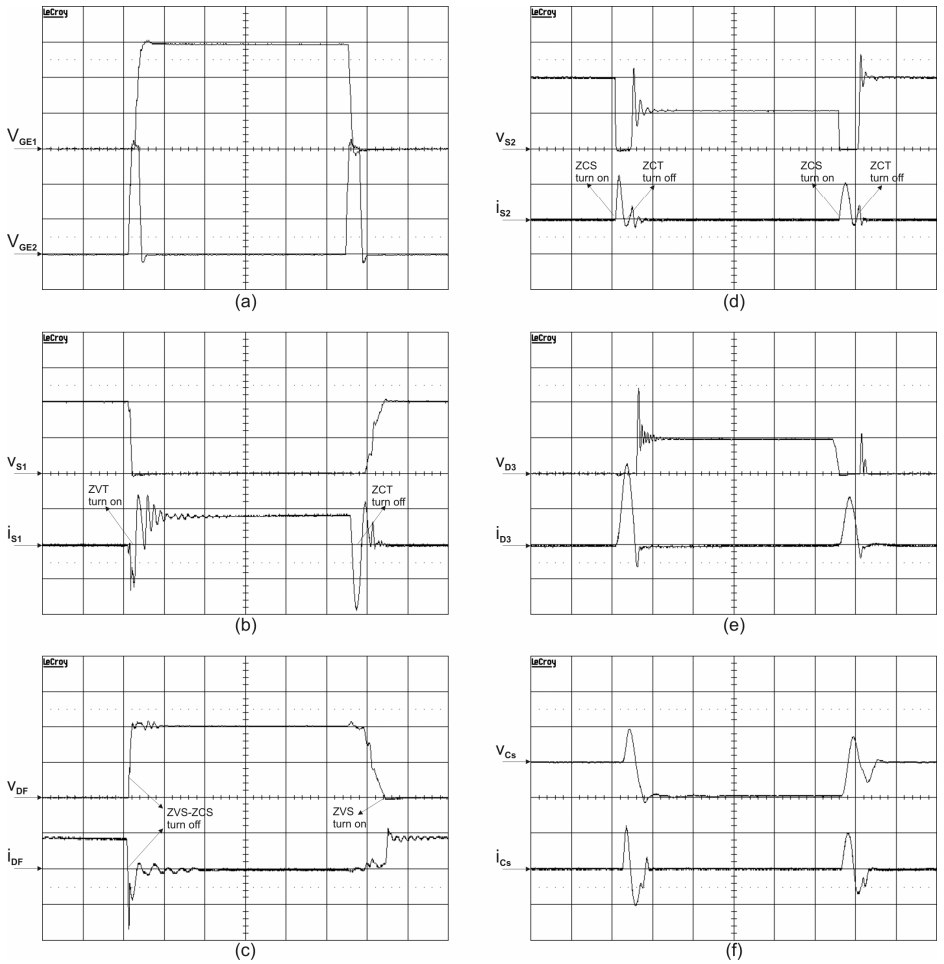

Fig. 6. Some oscillograms with the scales of 5 V/div, 1 µs/div for only (a), 200 V/div, 2 A/div, 1 µs/div for (b)-(g): (a) Control signals of S_1 and S_2; (b) Voltage and current of S_1; (c) Voltage and current of D_F; (d) Voltage and current of S_2; (e) Voltage and current of D_3; (f) Voltage and current of C_s.

as suggested in [21]. Due to the well-known, the control circuit design procedure is not given here. UC3854A integrated circuit generates the control signal of the boost switch. The auxiliary switch control signal is produced by using the control signal of the boost switch with the help of the analog card.

In the Fig. 6(a), the control signals of the main and auxiliary switches are shown. The auxiliary switch operates twice in a one switching period of the main switch.

The voltage and current waveforms of the boost switch S_1 are shown in the Fig. 6(b). It can be seen that turn on and turn off process of the S_1 is realized with soft switching. There is no overlap between current and voltage waveforms of S_1. From the S_1 current waveform, the body diode is turned on firstly and then the control signals of the S_1 is removed during the turn on and turn off process of the switch. So, ZVT turn on and ZCT turn off processes is perfectly realized. Also, there is no any additional voltage stress on the main switch and it has got an acceptable current stress.

The boost diode is turned on under ZVS and turned off under ZCS and ZVS. It can be seen in Fig. 6(c), there is no any additional voltage and current stresses on the boost diode.

The auxiliary switch voltage and current waveforms are shown in Fig. 6(d). The auxiliary switch is operated in both ZVT and ZCT processes of the boost switch. It means that the operating frequency of the auxiliary switch is two times of the boost switch operating frequency. Also, the auxiliary switch conduction time is very short. The auxiliary switch is turned on under near ZCS due to the serial connected inductance and is turned off with ZCT perfectly due to the removal of drive signal while the body diode is conducting. By the way, there are no additional voltage stresses on the auxiliary switch while its operate under soft switching.

Fig. 6(e) shows the voltage and current waveforms of D_3. Reverse recovery current of the diode and a discharge current of the capacitor are shown in that figure.

The voltage and current waveforms of the snubber capacitor are shown in Fig. 6(f). The voltage across the snubber capacitor starts to increase when the resonance is started with the auxiliary transistor turn on in the ZVT interval of the boost switch. It becomes zero nearly half of the output voltage at the end of the ZVT interval. At the end of the ZCT interval, the capacitor voltage is equal to zero.

The input voltage and current waveforms are given in Fig. 7. The power factor of the proposed converter is near unity with 0.99. Also, it is seen that the proposed PFC converter operates in CCM. Fig. 8 presents the response of the power factor for universal input line voltage for full load condition. It can be observed that the proposed converter will exhibit a power factor of near 0.99 at any power line voltage between 85 and 260 V_{rms}. The proposed converter is tested at universal input line voltage and very wide load ranges. It is observed that it keeps operating

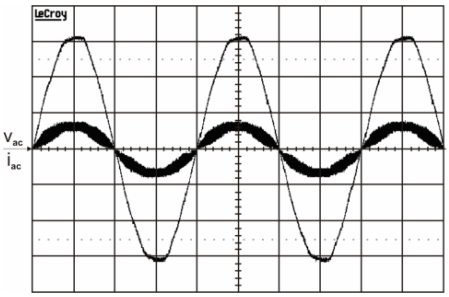

Fig. 7. The input voltage and current waveforms with the scales of 100 V/div, 5 A/div and 5 ms/div.

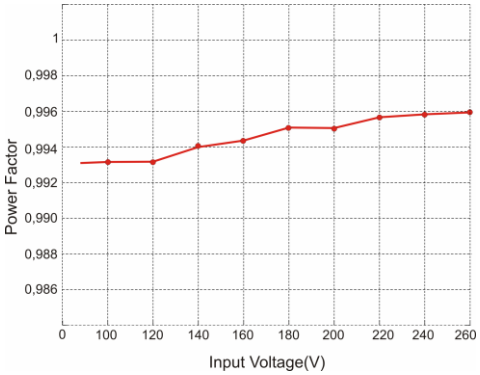

Fig. 8. The input voltage and current waveforms with the scales of 100 V/div, 5 A/div and 5 ms/div.

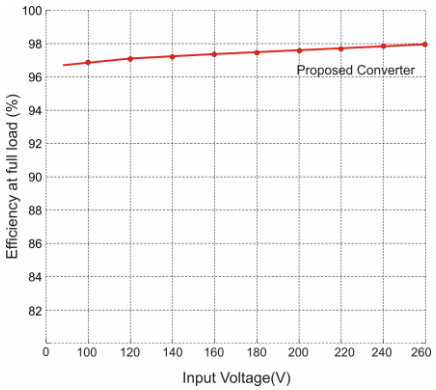

Fig. 9. Converter efficiency at full load and varying line voltage.

under soft switching conditions successfully for the whole line and load ranges.

In the Fig. 9, efficiency waveform of the proposed converter is given for the range of universal input line voltage at full load. The efficiency value is increasing along with the line voltage. Basically, losses depend on current in the converters. In order to obtain the same output power, the input current decreases when the input line voltage increases.

In the Fig. 10, efficiency variations of the proposed converter and the converter in [20] are given for 220 V_{rms} input voltages. It can be seen that the efficiency values of the proposed converter which operates at 100 kHz are

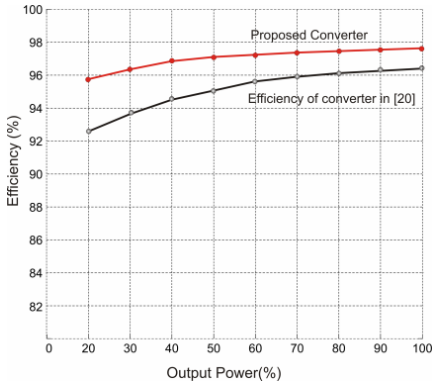

Fig. 10. Efficiency curves of the proposed converter and the converter in [20].

higher than the converter in [20] which operates at 50 kHz. The main reason of the efficiency improvement is all switches operate under exact soft switching in the proposed converter. The overall efficiency of the proposed converter is measured about 97.9% at the nominal output power.

6. Conclusion

In this study, a novel snubber circuit is used in the PFC converter. This snubber circuit provides ZVT turn on and ZCT turn off together for the boost switch of the converter. Also, it is implemented by using only one quasi resonant circuit without an important increase in cost and complexity. The proposed converter solves many drawbacks of the PFC converters presented earlier. All semiconductor devices in the circuit are switched under soft switching. The boost switch is not subjected to any additional voltage stress. The boost diode is not subjected to any additional voltage and current stresses. A detailed steady-state analysis of the proposed converter is presented. The theoretical analysis of the proposed converter is exactly verified by 500 W and 100 kHz prototype. The average current mode control method is used in the proposed converter. The power factor of the proposed converter is measured nearly 0.99. Additionally, at nominal output power, the converter efficiency is reach approximately 97.9%.

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