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I/O 트랜지스터의 핫 캐리어 주입 개선에 관한 연구

문성열* · 강성준* · 정양희**

A study on the Hot Carrier Injection Improvement of I/O Transistor

Seong-Yeol Mun* · Seong-Jun Kang** · Yang-Hee Joung**

요 약

반도체 소자 제조에서 비용 절감을 위한 공정기술의 스케일링 가속화 경향에 따라 축소기술에 대한 요구가 증가되고 있다. 축소에 따른 또 다른 가장 큰 문제점의 하나는 Hot Carrier Injection (HCI) 특성의 열화이다. 이는 축소 과정에서 생기는 불가피한 가장 큰 이슈중의 하나이며, 특히 입출력 소자에 있어 극복하기 어려운 부분이다. 이의 개선을 위해 유효 채널 길이를 늘이고자 LDD 임플란트 공정 이전에 산화막이 추가되었고, 또한 I/O LDD 임플란트 공정의 이온 입사 각도를 최적화함으로써, LDD 영역에서 E-field 열화 없이 HCI 규격을 만족할 수 있었다.

ABSTRACT

As the scaling trend becomes accelerated in process technology for cost reduction in semiconductor chip manufacturing, the requirement for shrink technology has increased. Hot Carrier Injection (HCI) degradation for I/O transistors is most concerning part when shrink. To solve this, the effective channel length (Leff) was increased using liner oxide before Light Doped Drain (LDD) implants and optimized the tilt angle to increase Leff without E-field degradation in LDD region, satisfying the HCI specification.

키워드

LDD Implant, Ion Tilt Angle, Linear Oxide Films, Hot Carrier Injection, Effective Channel
LDD 임플란트, 이온 입사각, 산화막, 핫 캐리어 주입, 유효채널

Ⅰ. Introduction

As the requirement for cost down by increasing the number of semiconductor chips within wafer, the scaling trend becomes accelerated in process technology. The shrink technologies have been related to core transistors only excluding input & output (I/O) transistors, because the I/O shrink is much more challenging. The one of major challenging item is hot carrier injection (HCI) lifetime degradation for I/O circuit which operation voltage is 3.3 V.

Hot Carrier Injection (HCI) degradation for I/O transistors is the most concerning part when

* 전남대학교 전기및반도체공학과(msyc1103@hanmail.net)
** 교신저자(corresponding author) : 전남대학교 전기및반도체공학과(jyanghee@jnu.ac.kr)
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shrink. Actually, the previous shrink technologies avoided the I/O shrink because of this HCI issue. The I/O transistors are very sensitive to HCI due to the thicker gate oxide (higher impact by drain voltage) and higher drain voltage. More than worse, the HCI performance for pre-shrink has narrow margin already because of the punch through implant step for both n-MOS and p-MOS. The punch implant in I/O transistors can be used to increase R_{out} by reducing I_{off}[1-4], but, degrades the HCI performance due to the increased electric field (E-field) in light doped drain (LDD) region. Generally, the HCI is the most sensitives to the channel length in fixed operation voltage and gate oxide. However, the channel length can't be increased due to size limitation. There is no choice but to increase effective channel length (L_{eff}) to solve this problem[5-6]. In this paper, New liner oxide was added before LDD implant to increase the L_{eff}[7-8]. The increased L_{eff} was clear by TCAD simulation results. LDD implant tilt-angle was also optimized to increase the L_{eff}. Generally, tilt- angle is applied to reduce the channeling issue, resulting in shallow implant. However, too big tilt-angle can reduce the channel length and increase gate overlap capacitance. In reverse, too low tilt-angle can cause the sharp corner of LDD doping profile, which can increase E-field crowding on the corner. This study optimized the tilt-angle to increase L_{eff} without E-field degradation in LDD region, satisfying the HCI specification[6].

II. Experimental

A (100)-oriented p-type 8-inch Si wafer with a resistivity of 8~12ohm-㎝. The gate oxidation is a NO oxynitride process using rapid thermal oxidation (RTO), in which wet oxidation at 800℃ and NO anneal at 850℃ are consecutively performed. After gate oxide formation, poly was deposited by 1150Å and litho and etching process were performed. And, spacer liner oxide 100Å using TEOS and spacer liner nitride 220Å using CVD and oxide using TEOS were carried out followed by TEOS and nitride etching.

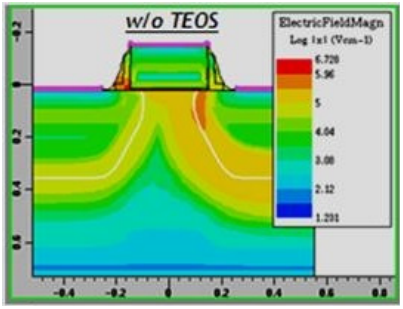
To improve HCI lifetime, increase of effective channel length (L_{eff}) was tried using liner TEOS oxide of 680℃ CVD process before LDD implant and LDD implant tilt-angle reduction for IO transistors. By adding 100Å TEOS right before the LDD implant, the L_{eff} can be increases by that thickness for thick n-, p-MOS transistor. The TEOS deposition temperature 680℃, thermal budget, doesn't affect the device performance. However, L_{eff} for p-MOS should be increased more, because the HCI lifetime margin is more narrower than n-MOS. For this, LDD implant tilt-angle, processed to minimize the channeling, was tried to reduce and optimum angle was determined considering E-field and L_{eff} by TCAD simulation. If the tilt-angle is too small, that can cause sharp corner of LDD profile, causing E-field crowding in the sharp corner profile.

III. Results and Discussion

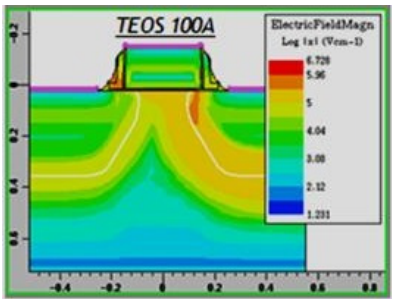
HCI lifetime using additional linear oxide before LDD implant and the optimization of LDD implant is improved. Fig. 1 shows the gate structure profile for 100Å TEOS before LDD implant process.

For 3.3V n-MOS, L_{eff} was found to increase 10nm by adding the 100Å TEOS as shown in Fig. 1, because the TEOS step coverage is 50%. E-field simulation showed reduced E-field as exhibited in Fig. 2. Eventually, by using TEOS side wall, TEOS thickness increases, we confirmed that the LDD junction E-field is decreased.

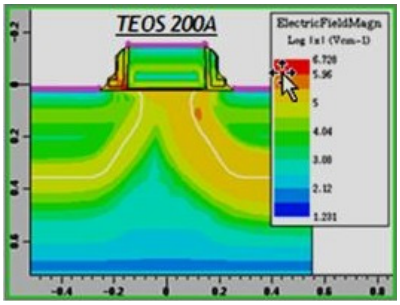
Fig. 1 Gate structure profile for 100Å TEOS before LDD implant process



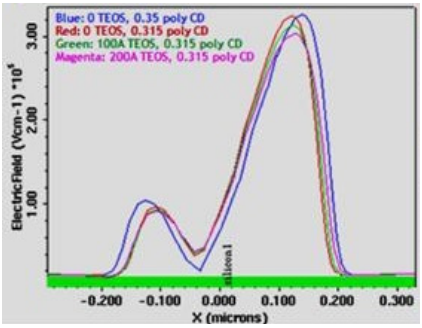
(a)



(b)



(c)



(d)

Fig. 2 E-field profile with different TEOS thickness and without TEOS before LDD implant for I/O (3.3V) n-MOS (a) without TEOS (b) TEOS 100Å (c) TEOS 200Å (d) E-field distribution with TEOS thickness

The reduced E-field in LDD Junction by TEOS is due to more graded profile of phosphorous implant, used for LDD implant [5-6].

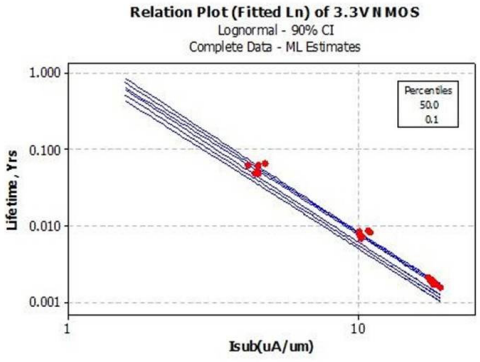


Fig. 3 HCI lifetime for I/O (3.3V) n-MOS after improvement

The TEOS 100Å before the 3.3V n-MOS LDD implant reduced I_{submax} from 2.9 to 2.4㎂/㎛ by 17%, passing the HCI lifetime specification, 0.2years, with 0.52, 0.54, 0.46years for each 3 Lots, respectively as shown in Fig. 3.

For 3.3V p-MOS, which has narrower margin in HCI lifetime due to the punch through preventive implant, additional improvement item was applied except the 100Å TEOS deposition which reduces the E-field in p-MOS also as shown in simulation

results of Fig. 4. [7-8].

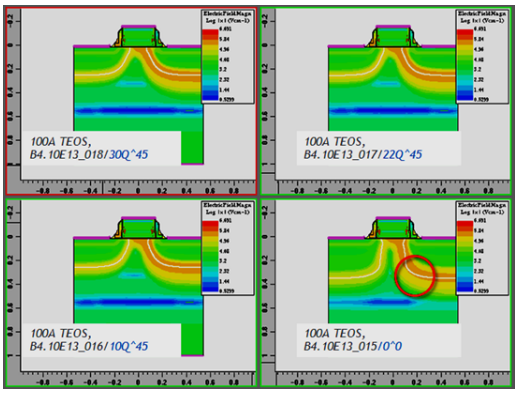


Fig. 4 E-field profile with different tilt angle of LDD implant for I/O (3.3V) p-MOS

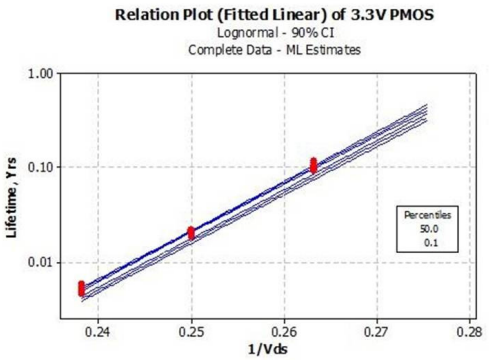


Fig. 5 HCI lifetime for I/O (3.3V) p-MOS after improvement

Tilt-angle of LDD implant was reduced for additional L_{eff} increase by changing from B3.0E13, 17KeV, 30° tilt-angle and 45° twist-angle, with quadrupole to B3.0E13, 17keV, 22° tilt-angle and 45° twist-angle, with quadrupole, resulting in 15nm increase of L_{eff}. But, If the tilt-angle is too small, that can cause sharp corner of LDD profile, causing E-field crowding in the sharp corner profile. As a result, passed HCI spec, 0.2years, with 0.34, 0.33, 0.3years for each 3 Lots, respectively as shown in Fig. 5.

As an additional analysis, the E-field according to the punch preventive implant is investigated in the pre-shrink and post-shrink. The I/O n-MOS has punch-preventive implant step in case of pre-shrink process and that enables wider space between source and drain as shown in Fig. 6. However, the punch-preventive implant step increases the E-field in LDD region as shown in TCAD simulation Fig. 6, increasing I_{sub} and resulting in HCI lifetime failure. They are trade-off relations [9-11]. Designer need to be careful for the trade-off.

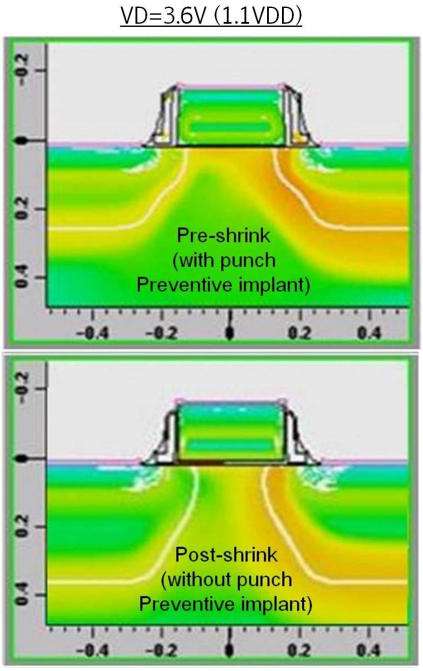


Fig. 6 E-field TCAD simulation profile comparison for I/O (3.3V) n-MOS between pre-shrink and post-shrink process

Ⅵ. Conclusions

The barriers for process reliability of shrink process are also big issue. The most concerning part when shrink even the I/O transistor is HCI

lifetime issue due to the smaller channel length that is the most critical parameter for HCI. By optimizing the implant conditions(22° tilt-angle and 45° twist-angle) and increasing the effective channel length using additional liner oxide(100Å TEOS) before LDD implant, resulting in 15nm increase of L_{eff}. we confirmed that HCI lifetime can be recovered to pre-shrink level.

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저자 소개

문성열(Seong-Yeol Mun)

1994년 경기대학교 물리학과졸업(공학사)
2006년 전남대학교 대학원 전기및 반도체공학과 졸업(공학석사)
2011년 전남대학교 전기및반도체공학과(공학박사)
현재 Globalfoundries Ltd., USA, manager
※ 관심분야 : 소자 공정 개발

강성준(Seong-Jun Kang)

1989년 인하대학교 응용물리학과 졸업(공학사)
1994년 인하대학교 대학원 전자재료공학과 졸업(공학석사)
1999년 인하대학교 대학원 전자재료공학과 졸업(공학박사)
현재 전남대학교 전기및반도체공학과 교수
※ 관심분야 : 기능성박막, 반도체공정 및 재료

정양희(Yang-Hee Joung)

1983년 단국대학교 응용물리학과 졸업(공학사)
1985년 인하대학교 대학원 응용물리학과 졸업(공학석사)
1993년 인하대학교 대학원 전자재료공학과 졸업(공학박사)
1995년~현재 전남대학교 전기및반도체공학과 교수
※ 관심분야 : 반도체 공정 및 물성