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Investigation of Buffer Traps in AlGaN/GaN Heterostructure Field-Effect Transistors Using a Simple Test Structure

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Abstract—**We propose a new method which can extract the information about the electronic traps in the semi-insulating GaN buffer of AlGaN/GaN heterostructure field-effect transistors (HFETs) using a simple test structure. The proposed method has a merit in the easiness of fabricating the test structure. Moreover, the electric fields inside the test structure are very similar to those inside the actual transistor, so that we can extract the information of bulk traps which directly affect the current collapse behaviors of AlGaN/GaN HEFTs. By applying the proposed method to the GaN buffer structures with various unintentionally doped GaN channel thicknesses, we conclude that the incorporated carbon into the GaN back barrier layer is the dominant origin of the bulk trap which affects the current collapse behaviors of AlGaN/GaN HEFTs.**

Index Terms—**AlGaN/GaN HFET, semi-insulating GaN buffer, bulk trap, carbon-doped GaN back barrier**

I. INTRODUCTION

Recently, AlGaN/GaN heterostructure field-effect transistors (HFETs) fabricated on a silicon substrate are attracting considerable attention as promising candidates for next generation microwave and power electronic devices [1]. However, there still remain some issues, including dynamic on-resistance degradation and current collapse which seriously limits the switching performance of devices [2]. In previous works, the formation of a front-side virtual gate associated with surface traps has been considered as the dominant mechanism causing the current collapse in AlGaN/GaN HFETs [2]. However, recent reports show that the bulk traps in the semi-insulating GaN buffer also can cause the serious current collapse in AlGaN/GaN HFETs [3]. Previously, the bulk traps in the semi-insulating GaN buffer have been mainly investigated using the capacitance-mode deep level transient spectroscopy (C-DLTS) [4], the backgating current transient spectroscopy [5, 6], and the drain current transient method [7-9]. C-DLTS is a powerful and well-established technique for the extraction of bulk traps in semiconductor devices. However, since it generally requires large area Schottky diodes, C-DLTS is difficult to apply to actual transistors due to their small gate capacitance. Considering that the distribution of the electric field is quite different in diodes and in actual transistors, the obtained results from C-DLTS cannot give clear information about the location of electronic traps in HFET structures. The backgating current transient spectroscopy is the method which has been used to investigate the bulk trap in the metal-semiconductor field effect transistors and HFETs. For HFETs, the backgating depletion region and therefore the influence of the substrate voltage is limited below the

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two dimensional electron gas (2DEG), therefore, all related effects have their origin in the bulk without contribution of surface effects. This method has a merit that it does not require a large area device. However, electronic trap extracted from this method can be different from the one which affects the current collapse behavior of the device, because the electric field distribution within the device during the application of the substrate bias is different from that during the operation of the transistor. As a more effective method to extract the bulk trap in AlGaN/GaN HFETs, the drain current transient method was suggested by Joh et al. [7]. They expose the AlGaN/GaN HFETs to the on-state stress (high I_D and relatively high V_{DS}, V_{GS} = 0 V and V_{DS} = 10 V in [7]) for a while, and observe the subsequent drain current transient in the linear regime (V_{GS} = 1 V and V_{DS} = 0.5 V in [7]). In this method, the information about the trap can be obtained from the recovery characteristics of I_D due to the detrapping of electrons which were captured by the traps during the on-state stress. Although this method can extract the information about the electronic traps directly from the actual transistors, it has a drawback of discerning the location of the extracted traps between the surface and the bulk, because the electrons are trapped not only by the bulk trap but by the surface trap during the on-state stress due to the relatively high V_{DG}. In this letter, we propose a new method which can selectively extract the information about the electronic traps in the semi-insulating GaN buffer of AlGaN/GaN HFETs using a simple test structure, and investigate the bulk traps in the GaN buffer structures with various unintentionally doped (UID) GaN channel thicknesses based on the proposed method.

II. TEST STRUCTURE FABRICATION & MEASUREMENT SCHEME

Fig. 1(a) shows the cross sectional view of the proposed test structure to investigate the electronic traps in the semi-insulating GaN buffer of AlGaN/GaN HFETs. The samples were grown by metal-organic chemical vapor deposition (MOCVD) on 6-in Si substrates, and carbon doping of GaN buffer is achieved without an additional carbon source. UID GaN channel layers with various thicknesses (200 – 1000 nm) were followed by a

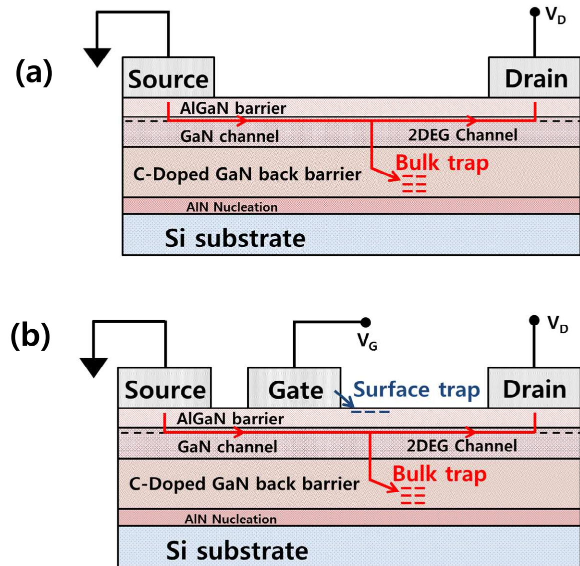

Fig. 1. Cross sectional view of the (a) proposed test structure, (b) AlGaN/GaN HFET. Arrows indicate the electron flow. Because there is no gate electrode in the proposed test structure, the electrons are not captured by the surface traps in the gate-drain access region during the on-state stress, and the recovery characteristics of I_D can be attributed solely to the detrapping of electrons from the traps located in the GaN buffer.

GaN:C buffer structure (2 μm, [C] ~ 10^{19} cm^{-3}). A 25 nm-thick $Al_{0.25}Ga_{0.75}N$ layer was then grown on a UID GaN channel layer to form the 2DEG, and Ti/Al/Pd/Au metal stacks were deposited and annealed at 800 °C in N_2 atmosphere for source and drain electrodes. The width (W) and length (L) of the test structure were designed to be 200 μm and 30 μm, respectively.

In the proposed method, the information about electronic trap in the GaN buffer can be extracted by monitoring the time transient of I_D right after reducing the magnitude of V_{DS}. When V_{DS} is high, relatively large I_D flows between source and drain electrodes through the channel and bulk of the test structure because the AlGaN/GaN HFET exhibits the normally-on characteristics, and electrons are captured by the bulk trap during this operation. After lowering V_{DS}, the trapped electrons in the GaN buffer are detrapping from the bulk trap, and I_D continuously increases with a time.

By observing these recovery characteristics of I_D at various temperatures, we can extract the information of GaN bulk trap. As commented in the introduction part, electrons are captured by the traps located not only in the GaN buffer but in the surface when the AlGaN/GaN HEFTs are exposed to the on-state stress in the

conventional drain current transient method (Fig. 1(b)). However, because there is no gate electrode in the proposed test structure, the electrons are not captured by the surface traps in the gate-drain access region during the on-state stress (Fig. 1(a)), and we can attribute the recovery characteristics of I_D solely to the detrapping of electrons from the traps located in the GaN buffer. The suggested method has a merit that it is very simple to fabricate the test structure and easy to apply. Moreover, the electric fields inside the test structure are very similar to those inside the actual transistor, so we can extract the information of bulk traps which directly affect the electrical behaviors of AlGaN/GaN HEFTs.

III. RESULTS AND DISCUSSION

Fig. 2(a) depicts the time transients of I_D measured at V_{DS} = 0.5 V right after exposing the test structure (UID GaN channel thickness : 200 nm) to the on-state stress (V_{DS} = 10 V) for 10 s. Measurements were made at various temperatures ranging from RT to 80 °C using the Agilent 4156 C semiconductor parameter analyzer. The test structure was illuminated by microscope light for 30 s before each measurement to recover the initial condition of the device. Fig. 2(a) shows that I_D increases with a time during the measurement at RT, and it is accelerated as the temperature increases. This phenomenon can be attributed to the accelerated detrapping process of captured electrons at higher temperatures. Fig. 2(b) shows the Arrhenius plot depicted using the extracted time constants from the results in Fig. 2(a). The multiple-exponential fitting method was used to extract the time constants from I_D transients at each temperature [7], and the activation energy (E_a) is determined to be ~ 0.25 eV from the Arrhenius plot in Fig. 2(b). Previously in theoretical studies, the formation of donor states with an energy level of ~ 0.2 eV below the conduction band edge was expected when C substitutes Ga (C_{Ga}) in carbon doped GaN (GaN:C) [10, 11]. The calculated E_a from Fig. 2(b) is consistent with this result, and it implies that the incorporated carbon into GaN to prevent punchthrough currents at high electric field is the possible origin of the bulk trap which affecting the electrical behaviors of AlGaN/GaN HEFTs even though the carbon-doped GaN back barrier is located 200-nm below 2DEG channel. Fig. 2(a) also

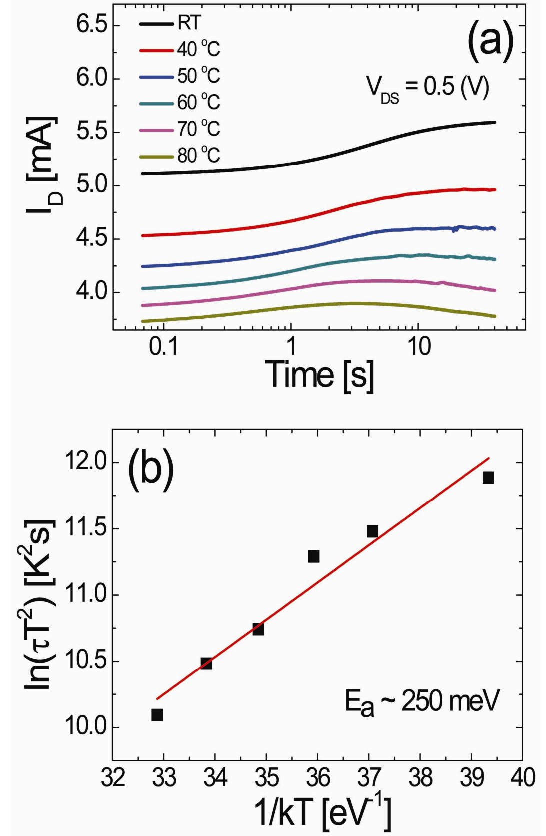

Fig. 2. (a) Time transients of I_D measured at V_{DS} = 0.5 V right after exposing the test structure (UID GaN channel thickness: 200 nm) to the on-state stress (V_{DS} = 10 V) for 10 s at various temperatures ranging from RT to 80 °C, (b) Arrhenius plot depicted using the extracted time constants from the results in Fig. 2(a). Time constants are extracted as 3.82, 2.35, 2.16, 1.16, 0.87, and 0.66 s at RT, 40, 50, 60, 70, and 80 °C, respectively.

shows the slight decrease of I_D with a time at high temperatures, it may be attributed to the re-trapping of electrons during the current transient measurements.

Fig. 3 depicts the time transients of normalized I_D measured for test structures with different UID GaN channel thicknesses at RT. Measurements were made at a same condition with that in Fig. 2(a). Fig. 3 shows that the magnitude of detrapping current is much reduced when UID GaN channel thickness increases. Moreover, the detrapping current becomes negligible in test structures without a carbon-doped GaN back barrier. This result confirms the conclusion of Fig. 2 that the carbon-doped GaN back barrier is the dominant source of bulk trap in fabricated AlGaN/GaN test structures, and shows that the current collapse behavior caused from the carbon doping cannot be perfectly eliminated even when the vertical spacing between the 2DEG channel and the

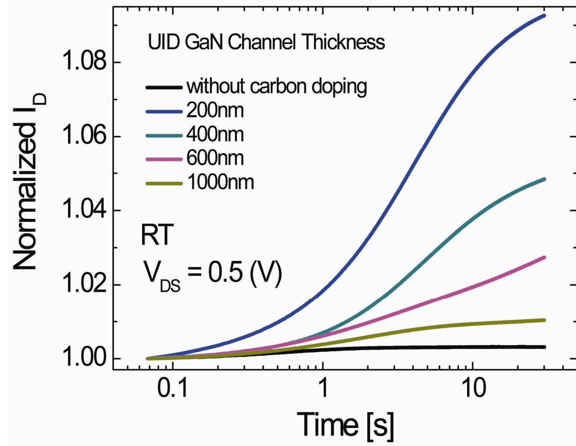

Fig. 3. Time transients of normalized I_D measured for test structures with different UID GaN channel thicknesses at RT. Measurements were made at a same condition with that in Fig. 2(a).

carbon-doped GaN back barrier is 1 μm.

Fig. 4 compares the time transients of normalized I_D measured for AlGaN/GaN HFETs (Fig. 4(a)) and test structures (Fig. 4(b)) with a UID GaN channel thickness of 200 and 400 nm at RT. The AlGaN/GaN HFETs are fabricated by forming the p-GaN gate on the AlGaN/GaN heterostructure. The HFET and test structure with a same UID GaN channel thickness were fabricated on the same wafer and source-to-drain distance of the HFET was designed to be same with that of the test structure. Fig. 4(c) depicts the transfer curves measured from the fabricated AlGaN/GaN HFETs. In AlGaN/GaN HFETs, the time transient measurements were made after changing the bias point (V_{GS}, V_{DS}) from (2 V, 10 V) to (2 V, 0.5 V). From the results of Fig. 4(a) and (b), we can observe that the detrapping transient of normalized I_D exhibit a similar shape in the HFET and test structure when a UID GaN channel thickness is same, which implies that the relatively slow current transient phenomenon (time constant (τ) > 0.1 s) in fabricated AlGaN/GaN HFET is mainly due to the electron detrapping from the bulk trap located in the carbon-doped GaN back barrier.

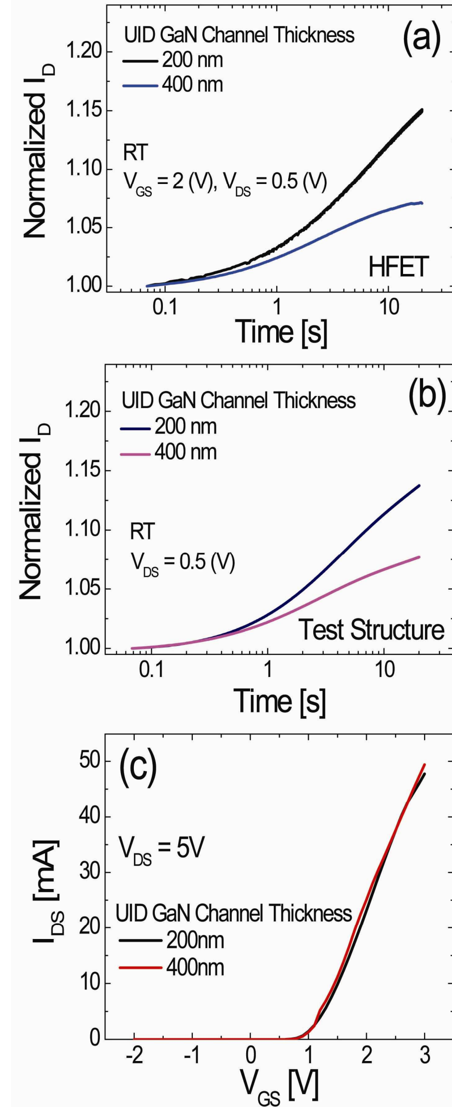

Fig. 4. Time transients of normalized I_D measured for (a) AlGaN/GaN HFETs, (b) test structures with a UID GaN channel thickness of 200 and 400 nm at RT. (c) Transfer curves measured from the fabricated AlGaN/GaN HFETs with a UID GaN channel thickness of 200 and 400 nm.

IV. Conclusions

In this letter, we propose the new method which can investigate the buffer traps in the AlGaN/GaN HFETs using a simple test structure. The operation principle of the proposed method is similar with that of the conventional drain current transient method, but we can selectively extract the information about bulk trap using the proposed method. The electric fields inside the test structure are very similar to those inside the actual HFET, so we can extract the information of bulk traps which directly affect the current collapse behaviors of AlGaN/GaN HEFTs. From the application of the proposed method to GaN buffer structures with various UID GaN channel thicknesses, carbon-doped GaN back barrier is concluded as the dominant source of the bulk

trap in fabricated AlGaN/GaN test structures even when the vertical spacing between the 2DEG channel and the carbon-doped GaN back barrier is 1 μm.

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REFERENCES

[1] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, “GaN on Si technologies for power switching devices,” IEEE Trans. Electron Devices, vol. 60, no. 10, pp. 3053–3059, Oct. 2013.

[2] S. Arulkumaran, G. I. Ng, and Z. H. Liu, “Effect of gate–source and gate–drain Si3N4 passivation on current collapse in AlGaN/GaN high-electron-mobility transistors on silicon,” Appl. Phys. Lett., vol. 90, no. 17, pp. 173504-1-173504-3, Apr. 2007.

[3] M. J. Uren, J. Möreke, and M. Kuball, “Buffer design to minimize current collapse in GaN/AlGaN HFETs,” IEEE Trans. Electron Devices, vol. 59, no. 12, pp. 3327–3333, Dec. 2012.

[4] Z. Q. Fang, B. Claflin, D. C. Look, D. S. Green, R. Vetury, “Deep traps in AlGaN/GaN heterostructures studied by deep level transient spectroscopy: Effect of carbon concentration in GaN buffer layers,” J. Appl. Phys., vol. 108, no. 6, pp. 063706-1-063706-6, Sep. 2010.

[5] M. Marso, M. Wolter, P. Javorka, P. kordos, and H. Luth, “Investigation of buffer traps in an AlGaN/GaN/Si high electron mobility transistor by backgating current deep level transient spectroscopy,” Appl. Phys. Lett., vol. 82, no. 4, pp. 633-635, Jan. 2003.

[6] M. J. Uren, M. Silverstri, M. Casar, G. A. M. Hurkx, J. A. Croon, J. Sonsky, and M. Kuball, “Intentionally carbon-doped AlGaN/GaN HEMTs: Necessaty for vertical leakage paths,” IEEE Electron Device Lett., vol. 35, no. 3, pp. 327–329, Mar. 2014.

[7] J. Joh and J. del Alamo, “Impact of electrical degradation on trapping characteristics of GaN high electron mobility transistors,” in IEDM Tech. Dig., 2008, pp. 461-464.

[8] J. Joh and J. del Alamo, “A current-transient methodology for trap analysis for GaN high electron mobility transistors,” IEEE Trans. Electron Devices, vol. 58, no. 1, pp. 132–140, Jan. 2011.

[9] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Bruckner, M. Mikulla, G. Meneghesso, and E. Zanoni, “Deep-level characterization in GaN HEMTs-Part I: Advantages and limitations of drain current transient measurements,” IEEE Trans. Electron Devices, vol. 60, no. 10, pp. 3166–3175, Oct. 2013.

[10] P. Boguslawski and J. Bernholc, “Doping properties of C, Si, Ge impurities in GaN and AlN,” Phys. Rev. B, vol. 56, no. 15, pp. 9496-9505, Jul. 1997.

[11] A. F. Wright, “Substitutional and interstitial carbon in wurtzite GaN,” J. Appl. Phys., vol. 92, no. 5, pp. 2575-2585, Sep. 2002.

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