A Low-Jitter DLL-Based Clock Generator with Two Negative Feedback Loops

Young-Shig Choi and Jong-Yoon Park

Abstract—**This letter proposes a low-jitter DLL-based clock generator with two negative feedback loops. The main negative feedback loops suppress the jitter of DLL. The additional negative feedback loops suppress the delay-time variance of each delay stages. Both two negative feedback loops in a DLL results in suppressing the jitter of clock signal further. Measurement results of the DLL-based clock generator with two negative feedback loops fabricated in a one-poly six-metal 0.18 μm CMOS process show 5.127-ps rms jitter and 47.6-ps peak-to-peak jitter at 1 GHz.**

Index Terms—**clock generator, delay locked loop, delay-time variance voltage converter**

I. INTRODUCTION

As the speed performance of recent chips rapidly increases, more emphasis is placed on suppressing jitter in high frequency clock signal. Phase locked loops (PLL's) and delay locked loops (DLL's) have been widely used in microprocessors and memory chips to generate on-chip clock signals. While the phase noise of PLL's is accumulated, that of DLL's is not accumulated, and thus, the clock signal generated from DLL's has lower jitter. For the clock multiplication, DLL requires evenly spaced edges from delay stages in voltage controlled delay line (VCDL). They span one period of reference signal. These evenly spaced edges are combined to form a pattern of higher frequency transition and eventually generate the desired high frequency clock signal. Timing uncertainty of edges due to PVT variations among the delay stages in VCDL causes a larger jitter.

An edge combiner is used to generate a higher frequency signal [1]. To suppress the timing uncertainty, novel techniques have been published. The self-calibrated technique by using shift averaging VCDL reduces the timing uncertainty of delay stages in VCDL but it has a difficulty of suppressing the timing uncertainty accurately [2]. The phase averaging and interpolation by using resistor arrays has been proposed to suppress the delay mismatch of delay stages but it requires a large area for resistor arrays [3]. The closet edge selection method digital DLL has been proposed to suppress the timing uncertainty [4]. The delay mismatches among delay stages are compared by using multiple phase detectors to suppress delay mismatch [5]. The multiple phase detectors which are sensitive to process variations may generate variation among their output. The self-calibration method that consists of a delay calibration buffer and a timing error comparator is used to reduce the delay mismatch [6]. The current mismatch of the timing error comparator can cause the systematic timing uncertainty.

In this letter, additional negative feedback loops for each delay cells in VCDL are introduced to suppress timing uncertainty (delay mismatches) of every delay stage. It has been implemented in 0.18μm CMOS process and shown the low measured jitter of the proposed DLL.

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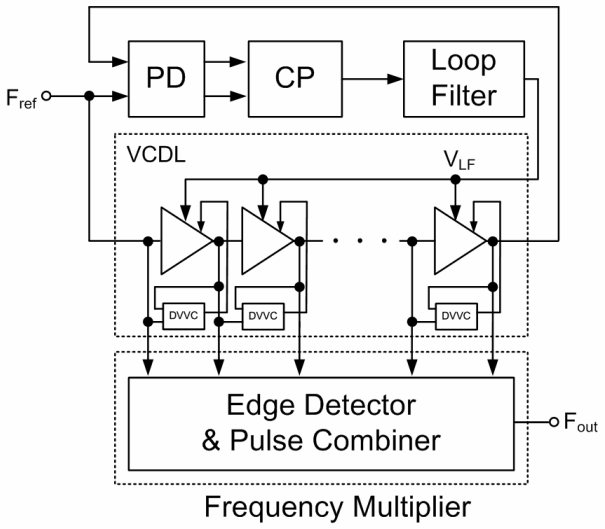

Fig. 1. Block diagram of the proposed clock generator with two negative feedback loops.

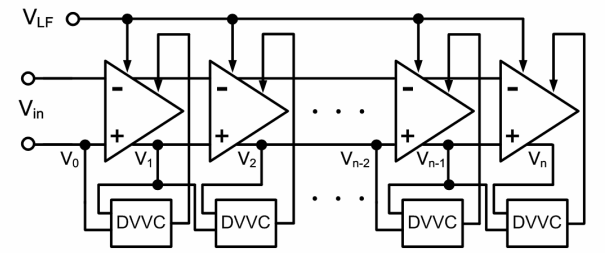

Fig. 2. Block diagram of the VCDL with DVVC. The VCDL is negative feedback looped with DVVC.

II. ARCHITECTURE OF DLL WITH TWO NEGATIVE FEEDBACK LOOPS

The entire architecture of the proposed DLL-based clock generator with two negative feedback loops is shown in Fig. 1. It consists of phase detector (PD), charge pump (CP), loop filter (LF), VCDL with multiple delay-time variance voltage converters (DVVC) and frequency multiplier (FM) consisted of edge detector and pulse combiner. The VCDL in Fig. 2 is made of differential delay stages and each delay stage is negative feedback looped with DVVC. Each delay stage has two input signals from LF and DVVC.

The main negative feedback loop consists of PD, CP, LF and VCDL. In the main negative feedback loop, the output voltage of LF is used to control the delay time of the whole VCDL. The additional negative feedback loop consists of one delay stage in VCDL and one DVVC. The DVVC senses the delay-time variance of each delay stages and generates voltage to suppress the delay-time variance of each delay stage in VCDL.

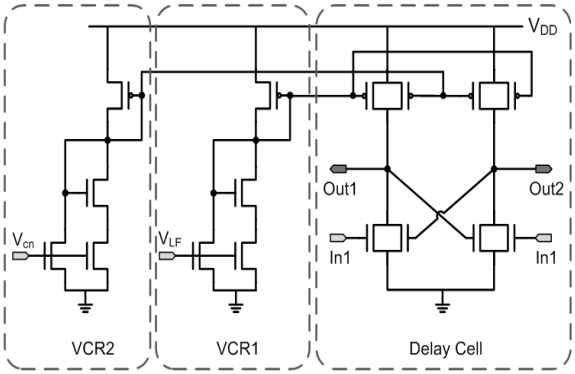

Fig. 3. Circuit of VCR & delay stage in VCDL.

When there is delay-time difference between F_{ref} and the output of VCDL, the output voltage of the loop filter (V_{LF}) changes to reduce the delay-time difference in the main negative feedback loop. When there is delay-time variance on the output of each delay stage in VCDL, the output voltage of the DVVC changes to suppress the delay-time variance of each delay stage in the additional negative feedback loop. Both negative feedback loops works simultaneously to suppress the jitter of DLL further.

$$T_{ref} = (t_1 + \Delta t_1) + (t_2 + \Delta t_2) + \cdots + (t_{n-1} + \Delta t_{n-1}) + (t_n + \Delta t_n) \quad (1)$$

where T_{ref} and t_n represent the period of reference signal and the delay-time of the delay stage in VCDL, respectively. Δt_n is the delay-time variance of the delay stage in VCDL. The main negative feedback loop works to reduce Δt_n of each delay stages at the same amount simultaneously. The additional negative feedback loop works to reduce Δt_n of each delay stages at the different amount and at different time. The operation of two negative feedback loops in a DLL results in suppressing the jitter of clock signal generated by the proposed DLL.

III. CIRCUIT DESCRIPTION

Fig. 3 shows the delay stage used in VCDL. Each delay stage has two voltage controlled resistors (VCR) which convert the output voltage from LF (V_{LF}) and DVVC (V_{cn}) into current to control the delay time of each delay stage.

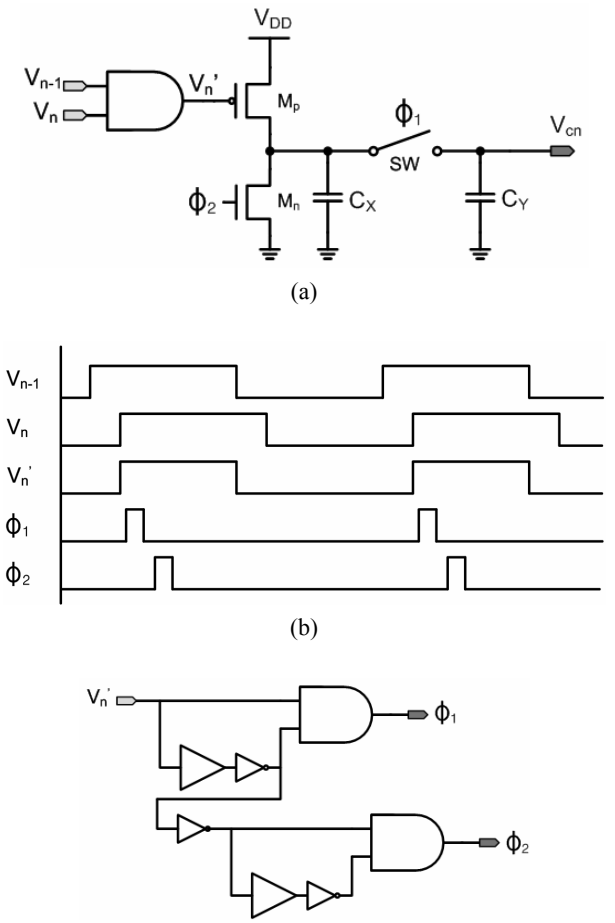

Fig. 4. (a) Circuit of DVVC, (b) Input, output and control signal timing, (c) Control signal block.

The circuit of DVVC, a modified FVC in [7], is shown in Fig. 4. The input signal (V_{n-1}) and the delayed signal, the output signal (V_n), of the n_{th} delay stage are AND gated and generated its output signal depending delay time of the n_{th} delay stage as shown in Figs. 4(a) and (b). The control signals of ϕ_1 and ϕ_2 are non-overlapped. When the V_n` is at its low level, the transistor M_p in Fig. 4(a) is turned on and C_x is charged. While ϕ_1 is high, switch SW is turned on and the charge is transferred from C_x to C_y. While ϕ_2 is high, the transistor M_n is turned on and the remaining charge of C_x is discharged to ground. The output voltage of DVVC depends on the period of low level of the signal, V_n`. The period of low level of the signal, $V_n$`, is determined by the rising time of the signal, V_n`. When there is no PVT variations among the delay stages in VCDL, the delay time of each delay stage is same and the period of low level of the signal, $V_n$`, is constant and the output voltage of DVVC is also constant.

When the delay time of n_{th} delay stage is longer than

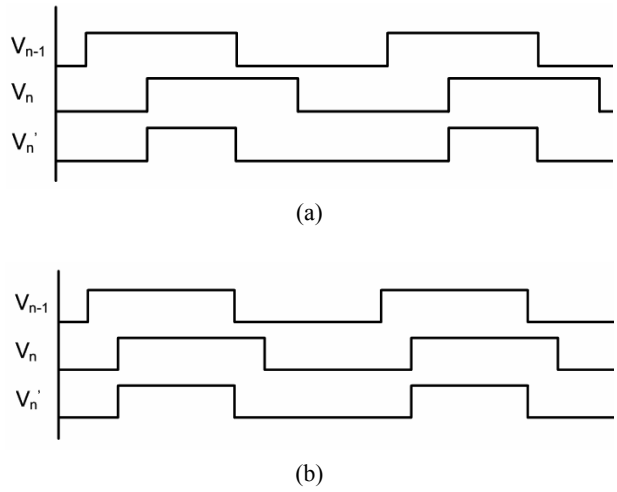

Fig. 5. Signal, V_n`, depending on the delay-time of delay stage in VCDL. (a) Long delay time, (b) Short delay time.

that of other delay stage, the period of low level of the signal, V_n` becomes large as shown in Fig. 5(a). Therefore, the output voltage of DVVC goes high and it shortens the delay time. When the delay time of $n_{th}$ delay stage is shorter than that of other delay stage, the period of low level of the signal, $V_n$` becomes small as shown in Fig. 5(b). Therefore, the output voltage of DVVC goes low and it lengthens the delay time. Whenever the delay time of delay stages in VCDL varies, the DVVC in a negative feedback loop with delay stages works as a compensator and it results in jitter reduction of the proposed DLL.

Fig. 6 shows frequency multiplier which is consisted of edge detector and pulse combiner. The edge detector consisted of an inverter and AND gate generates pulse signal at rising time of its input signal. The pulse combiner combines those pulses to generate high frequency output signal.

IV. MEASUREMENT RESULTS

The proposed DLL is implemented in a one-poly six-metal 0.18 μm CMOS process. The chip photograph is shown in Fig. 7(a). The lower layers of transistors and capacitors are not seen because of the thick multi-inter-metal layers. The die area is 1070 μm *350 μm without the LF capacitor.

Fig. 8 shows measured jitter characteristic. The multiplied output clock signal of 1GHz with a 100 MHz reference clock has 5.127-ps rms jitter and 47.6-ps peak-

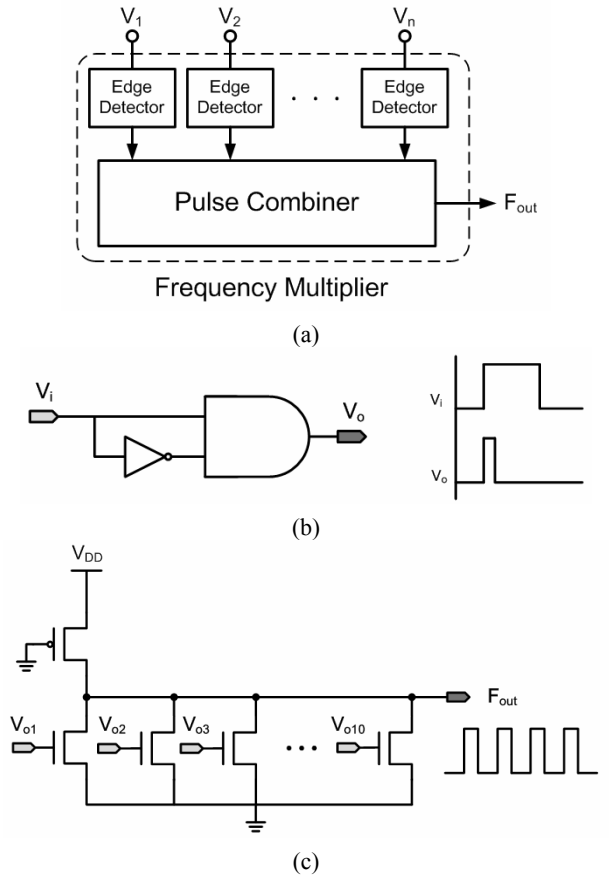

Fig. 6. (a) Frequency multiplier, (b) Edge detector, (c) Pulse combiner.

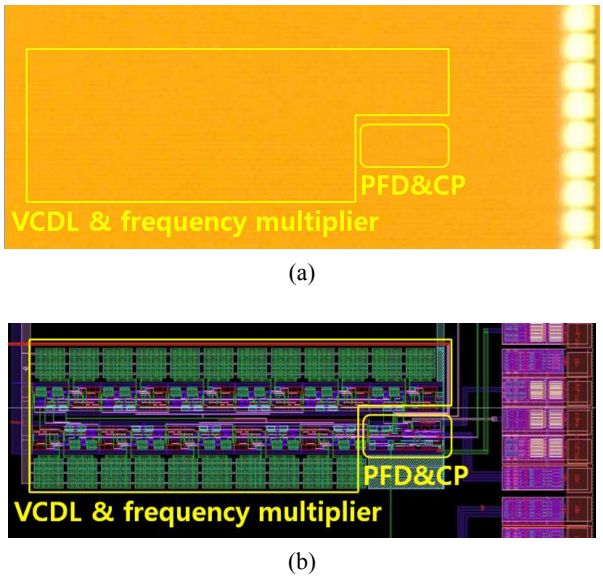

Fig. 7. (a) Chip photograph, (b) Layout of DLL with DVVC.

to-peak jitter. The jitter performance will probably be improved further by using a less current mismatched CP and a more careful layout of DVVC including the size of

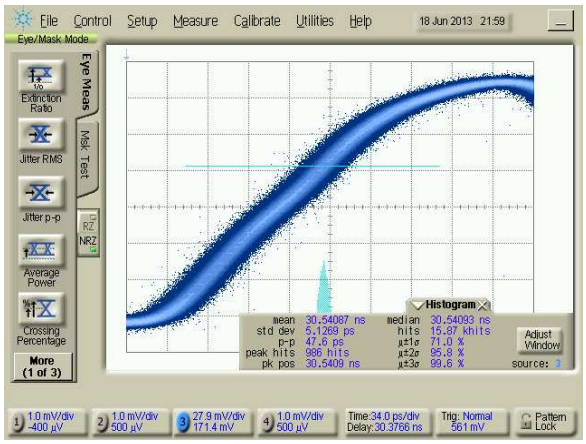

Fig. 8. Measured jitter characteristic at 1 GHz.

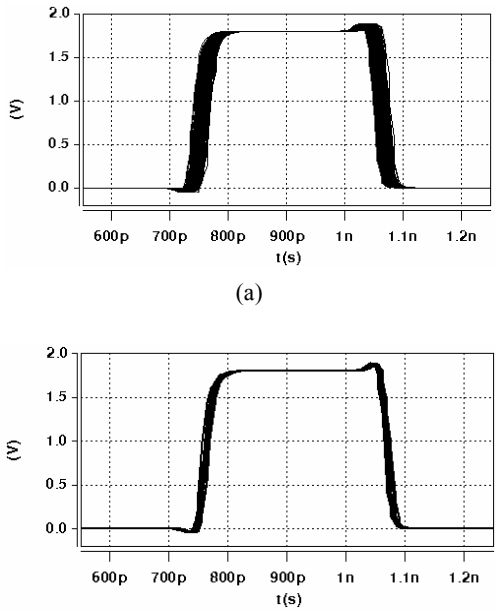

Fig. 9. Eye-diagram simulation results of the proposed DLL (a) without DVVC, (b) with DVVC.

capacitors. The proposed DLL dissipates 38.5mW including 6.5 mW of DVVC at 1 GHz.

It is impossible to partly turn off DVVC blocks because those are located in the inner VCDL. Therefore, the simulation results are shown in Fig. 9 to validate effectiveness of the DVVC function. In the simulation results, the jitters of DLL without and with DVVC are approximately 30 ps and 5 ps, respectively.

The jitter of 30 ps without DVVC can be caused by lots of reasons such as charge pump current mismatch and thermal noise of transistors, etc. It shows that the jitter performance of a DLL can be improved by the DVVC.

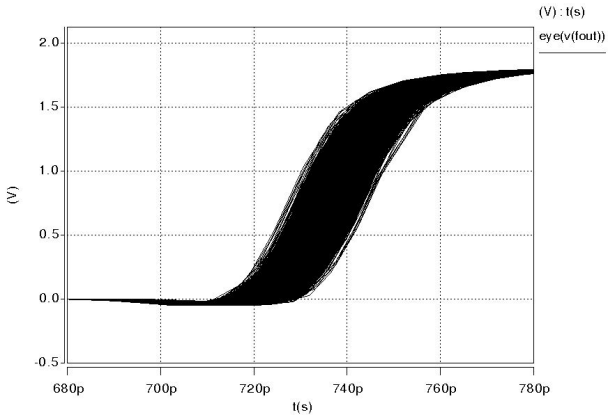

Fig. 10. Jitter characteristic caused by the mismatches among DVVCs.

In the proposed DLL, mismatches which are occurred by process variation among DVVCs can cause the increase of jitter. Monte Carlo simulation shows that the maximum jitter characteristic deteriorated by the mismatches among DVVCs is 17.5 ps. The variations of M_p (width) and C_x (capacitance) in the DVVC are 0.4% and 1.5%, respectively. The process variations are given by a manufacture. The measurement results of 5.127-ps rms jitter and 47.6-ps peak-to-peak jitter shows that the process variation is not as much as expected by Monte Carlo simulation.

V. CONCLUSIONS

This letter proposes a DLL-based clock generator with two negative feedback loops to suppress jitter. The main negative feedback loop works to reduce delay-time variance of each delay stages in VCDL at the same amount simultaneously. The additional negative feedback loop senses the delay-time variance of each delay stages in VCDL and generates different voltages to suppress delay-time variance of each delay stages in VCDL. Measurement results of the DLL-based clock generator with two negative feedback loops fabricated in a one-poly six-metal 0.18 μm CMOS process show 5.127-ps rms jitter and 47.6-ps peak-to-peak jitter at 1 GHz.

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