

A 45 nm 9-bit 1 GS/s High Precision CMOS Folding A/D Converter with an Odd Number of Folding Blocks

Seongjoo Lee, Jangwoo Lee, and Minkyu Song

Abstract—In this paper, a 9-bit 1GS/s high precision folding A/D converter with a 45 nm CMOS technology is proposed. In order to improve the asymmetrical boundary condition error of a conventional folding ADC, a novel scheme with an odd number of folding blocks is proposed. Further, a new digital encoding technique is described to implement the odd number of folding technique. The proposed ADC employs a digital error correction circuit to minimize device mismatch and external noise. The chip has been fabricated with 1.1V 45nm Samsung CMOS technology. The effective chip area is 2.99 mm² and the power dissipation is about 120 mW. The measured result of SNDR is 45.35 dB, when the input frequency is 150 MHz at the sampling frequency of 1 GHz. The measured INL is within +7 LSB/-3 LSB and DNL is within +1.5 LSB/-1 LSB.

Index Terms—Folding ADC, high precision ADC, odd number of folding blocks, SNDR, INL, DNL

I. INTRODUCTION

With the development of wireless communication and digital broadcasting markets in recent years, the demands for high speed Analog-to-Digital Converters(ADC) are rapidly increased in the field of satellite set-top box(S-STB), near field communication(NFC), military radar

system, and so on. Until now, a high-speed ADC beyond 1 GHz sampling clock is typically fabricated with BiCMOS or BJT technology. However, the technologies have to use high supply voltage, consume a lot of power. Furthermore, they don't conform to the recent trends of System-On-Chip(SOC) with a CMOS technology. Thus a high speed ADC with a 45 nm CMOS technology is described in this paper.

Conventionally, high conversion speed ADCs have been primarily designed with a flash type. However, flash ADCs cause a difficulty in realizing the high resolution beyond 8-bit, due to an increase of the number of preprocessing amplifiers by 2ⁿ times [1-3]. Thus it is a great constraint of high resolution ADCs because of its huge power consumption and chip area. To overcome those problems, folding structure has been continuously studied [4-16]. However, folding ADCs have an asymmetry error at the boundary conditions, since there is even number of folding blocks [5]. Further, the folding structure has a severe linearity error due to the undesired operation of the comparators. Even though a few calibration techniques have been published to improve the linearity errors, it is not enough to satisfy the required specifications [5, 6]. Hence, in this paper, an ADC satisfying 9-bit resolution and 1GHz conversion speed is proposed. It has a folding structure to satisfy high conversion speed and mid-range resolution. A novel scheme with an odd number of folding blocks is proposed to improve the asymmetrical boundary condition error of conventional folding structure. Further, a new digital encoding technique is described to implement the proposed folding technique. The proposed ADC employs a digital error correction circuit to minimize device mismatch and external noise

Manuscript received Jan. 30, 2014; accepted May. 8, 2014
A part of this work was presented in International SoC Design Conference (ISOCC), Busan in Korea, November 2013.
Seongjoo Lee, Jangwoo Lee, and Minkyu Song are with the Department of Semiconductor Science, Dongguk Univ.
E-mail : mksong@dongguk.edu

Table 1. Structure comparison among a few folding types

Structure (Coarse + Fine)	FR (Folding Rate)	IR (Interpolation Rate)	NFB (Number of Folding Blocks)	ΔRef (0.8Vpp diff.)	# of Preamplifiers	# of Comparators
Flash	-	-	-	0.781 mV	511	511
2+7	4	3, 4	even (32)	9.375 mV	96	4+128
3+6	8	3, 4	even (16)	9.375 mV	48	8+64
3+6	7.53	3, 4	odd (17)	9.375 mV	51	8+68
3+6	6.73	3, 4	odd (19)	9.375 mV	57	8+76
3+6	8.13	3, 3	odd (21)	9.375 mV	63	9+63
4+5	16	3, 3, 4	even (8)	28.125 mV	24	16+32
4+5	14.22	3, 3, 4	odd (9)	28.125 mV	27	16+36
4+5	11.63	3, 3, 4	odd (11)	28.125 mV	33	16+44

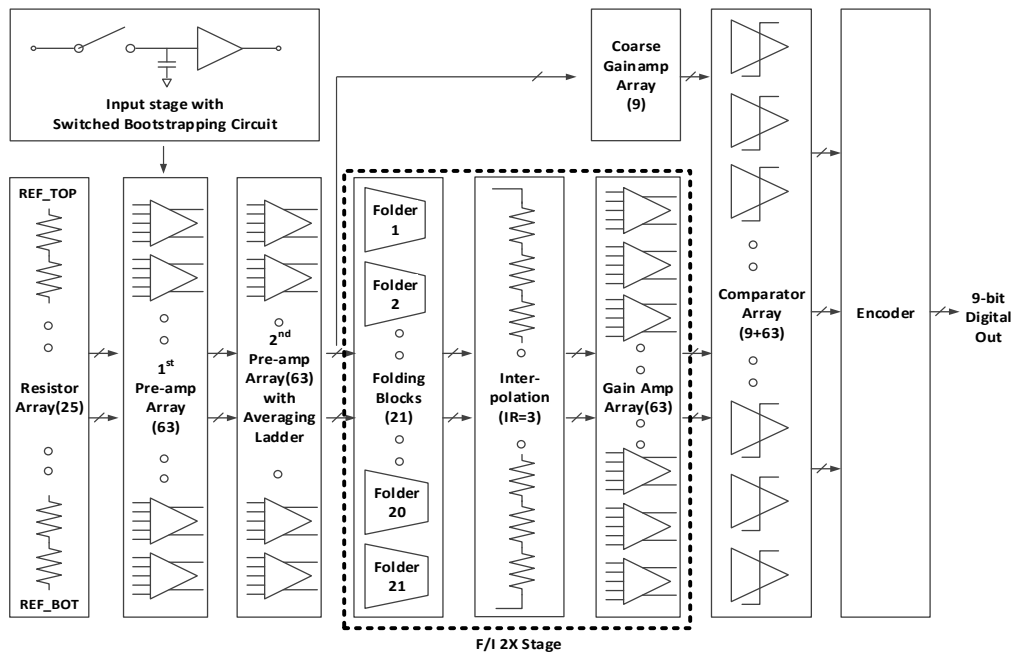


Fig. 1. Block diagram for the proposed 9-bit folding ADC.

The contents of this paper are as follows. In Section II and III, the architecture and the circuit technique for the proposed folding ADC are discussed, respectively. Measured results are described in Section IV. Finally, the conclusions are summarized in Section V.

II. ARCHITECTURE

Typically, in case of 9-bit folding ADC, it is designed with a split structure such as 2+7, 3+6, or 4+5 coarse and fine ADC. Table 1 shows the comparison of each structure in terms of the number of pre-amplifiers and comparators. The 2+7 structure has an advantage that it takes wider input bandwidth relatively. However, the 7-bit fine ADC has some problems of large chip area and

huge power consumption, because there are many comparators. In contrast, in case of 4+5 structure, small chip area and low power consumption are expected. But it causes very high folding rate (FR), and it is difficult to raise the frequency of input signal. Hence, the proposed ADC adopts the split structure of 3+6, considering the folding rate, power consumption, and chip area. Fig. 1 shows the block diagram of the proposed ADC which consists of an analog signal processing stage, a digital error correction circuit, a novel encoder, and so on.

In order to satisfy the folding rate, a cascaded folding structure is discussed as shown in Fig. 1. A resistive averaging technique is also adopted to improve the average offset errors of the pre-amps and folding blocks [7]. Normally, most of the conventional folding ADCs

have an even number folding blocks and preamp. It causes an asymmetric error at the boundary region. Thus a folding structure using an odd number of folding blocks and the preamp is discussed to solve the asymmetric error. Conventionally, the 2nd folding-interpolation stage is based on the even number of interpolation rate(IR=4) in [17]. However, it has a drawback that the zero-crossing cannot generate the perfect symmetrical codes of ADC. In order to solve this problem, the proposed 9-bit ADC is based on the odd number of interpolation rate(IR=3). Through this work, the symmetry of zero-crossing composition can be improved. However, it causes some problems of a complicated encoding process and a lot of switching arrays [10]. In order to solve that problem, the proposed ADC applies a novel digital encoder. It can minimize the switching problem, the chip area, and power consumption. In section III, the circuit technique and the role of each block are explained one by one.

III. CIRCUIT DESCRIPTION

1. Odd Number of Folding Blocks

A high conversion rate ADC typically has a parallel processing method to raise the speed. However, the parallel processing method has a nonlinearity problem because of the offset error at the amplifier stage. Further, conventional folding structures using even number of folding blocks have an asymmetric error at the boundary regions and it causes zero-crossing errors. Fig. 2(a) shows the asymmetric error of the even number of folding blocks. It has the inevitable zero-crossing error at the right boundary region. To solve those problems, dummy circuits, calibration engine, and other methods have been published [10-16]. However, they have a few drawbacks of huge power consumption, large chip area.

Hence, in this paper, an odd number of folding blocks to improve the linearity and symmetry is described. The proposed folding structure adopts a resistive averaging technique to improve the linearity when the signal of pre-amplifier stage is processed. Fig. 2(b) shows the circuit diagram and the analog signal diagram. If there is odd number of folding blocks, it is able to maintain the symmetric conditions at the left and right boundary region. Thus the linearity error can be reduced drastically.

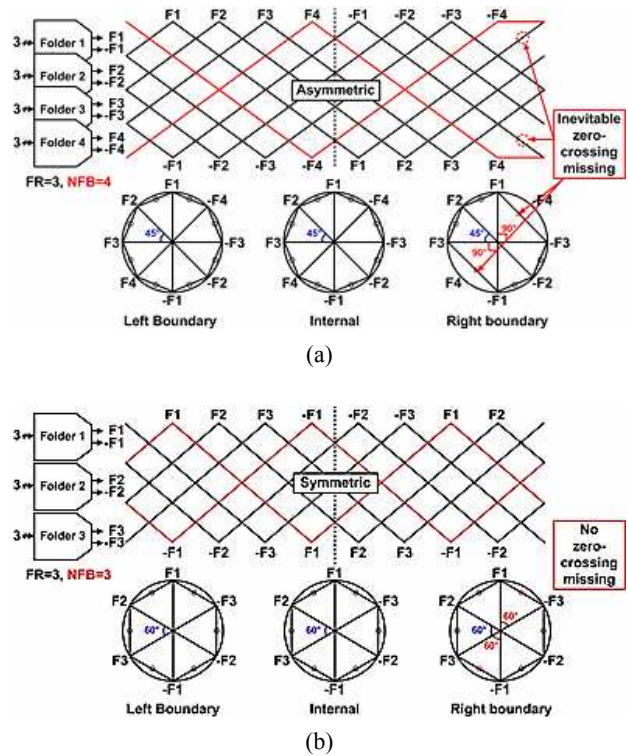


Fig. 2. Block diagram and analog signal diagram (a) conventional even number of folding blocks, (b) odd number of folding blocks.

2. A Digital Encoding Technique

Unlike the conventional ADCs based on even number of folding blocks, the proposed structure with an odd number of folding blocks has a problem that encoding process is complicated. When we choose a conventional encoding process, we have to use many ROMs and switching processors [11]. However, there are many complicated circuits, and the switching delay may cause a malfunction. Thus, a novel encoder using adder logic to minimize the switching process is proposed. Fig. 3 shows the encoding process of the coarse ADC and the fine ADC.

Since the folding rate is 8.13 at the proposed 3+6 structure, the folding structure has a digital signal value of $\log_2(8.13)$ ($N1=3.02$ -bit) at the coarse ADC block, and a digital signal value of $\log_2(63)$ ($N2=5.98$ -bit) at the fine ADC block. In order to generate the normal coarse digital bit ($N1=3$ -bit) and the fine digital bit ($N2=6$ -bit), the fractional digital bit must be converted into normal digital bit. The deficient 0.02-bit at the fine ADC block can be added by the addition of ROM1 digital output at

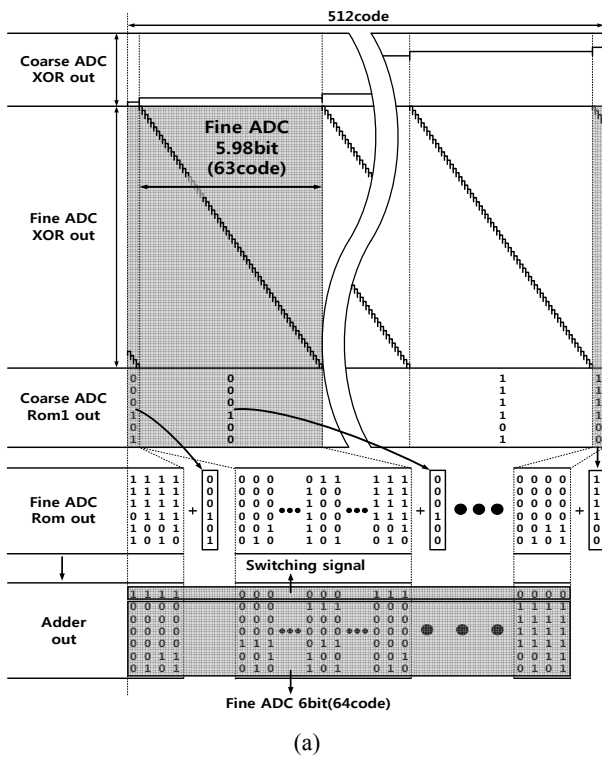


Fig. 3. Encoding process (a) encoding process of fine ADC, (b) encoding process of coarse ADC.

the coarse ADC block. Then, the switching signal of the adder block at the fine ADC selects the ROM2 or ROM3 at the coarse ADC block. Thus the results of coarse ADC are synchronized by the output of fine ADC, and the final 9-bit results of the folding ADC are finally obtained. The proposed encoder has an advantage of independent operation between the coarse ADC and the fine ADC,

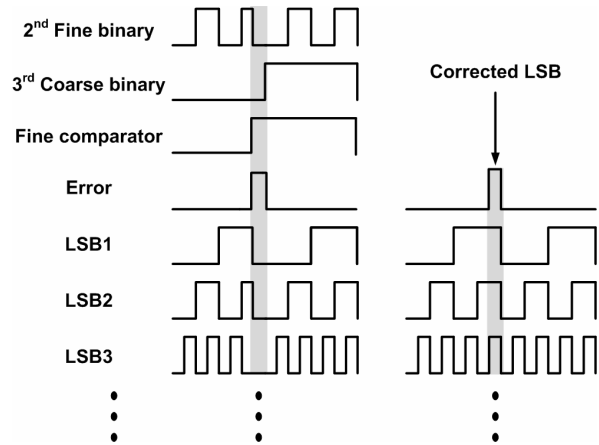


Fig. 4. Digital error correction process.

because we use an adder circuit. However, the conventional switching structure has a drawback of asynchronous delay time, because there is no adder.

3. Digital Error Correction Logic

Due to the difference of delay time between the coarse ADC and the fine ADC, a normal folding ADC with a split structure causes many critical errors. Therefore, in this paper, a digital error correction logic(DCL) to minimize digital code errors at the boundary region is discussed. Fig. 4 shows the proposed digital error correction process. First of all, DCL selects Up or Down signal in advance by the 2nd binary code of the fine ADC. It means pre-selected codes are stored. Then, the output of the XOR generated by both the 3rd binary code of the coarse ADC and the fine comparator output decides the LSB codes of the fine ADC. If the output of XOR is 1, the LSB codes are corrected into the preselected codes. If the output of XOR is 0, the LSB codes are not corrected. Therefore, it minimizes the coding errors generated by the time delay between the coarse ADC and the fine ADC.

IV. MEASURED RESULTS

Fig. 5 shows measured environments such as the chip microphotograph, testing printed circuit board, and measurement equipment. The chip has been fabricated by Samsung 45 nm CMOS technology, the core size is 2100 um x 1420 um. To measure a few GHz sampling frequency, a 1/16 down sampling decimation circuit is

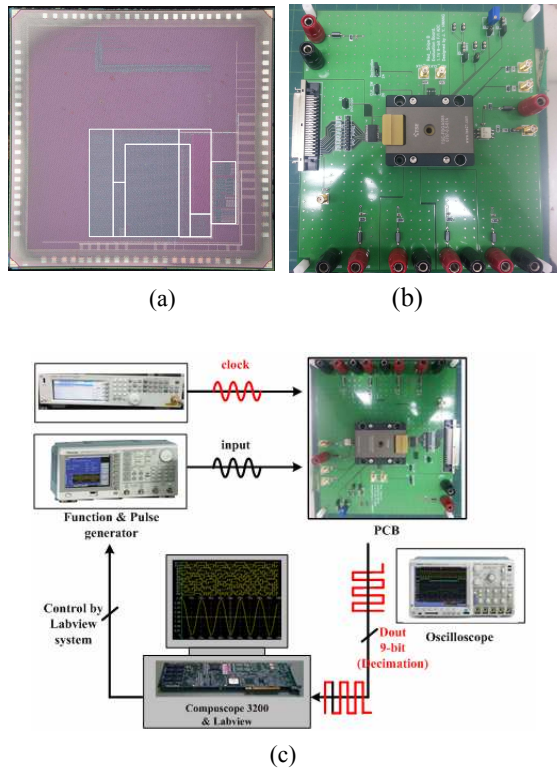


Fig. 5. Measured Environments (a) chip microphotograph, (b) testing board, (c) measurement equipment.

included. It is very helpful technique to verify the high-speed ADC. In order to verify the performance of ADC, a compuscope 3200 testing board that is able to measure SNR, DNL, INL, and other performance is used. We especially use Labview system to improve the reliability of the measurement, while we verify the characteristics of the ADC. Fig. 6 shows measured results for FFT spectrum, INL, DNL of the proposed ADC at the sampling frequency (f_s) of 1GS/s and the input frequency (f_{in}) of 6.2 MHz. The measured result of SNDR is 48.5 dB, SFDR is about 59.59 dBc. INL is within +7 LSB/-3 LSB and DNL is within +1.5 LSB/-1 LSB. Most of the ADCs have some drawbacks of linearity error, gain error, and a few errors due to device mismatching and other secondary effects. Hence, many ADCs recently have the self-calibration logic to reduce the errors [17]. But, since there is no calibration circuit in this ADC, the measured performance is not good. In case of INL, specially, the offset errors are continuously accumulated from the initial code to the final code. Thus it has a worst value of 7 LSB, and it must be reduced in a future.

Fig. 7 shows the measured SNDR vs input analog frequency at the sampling frequency of 1 GHz. The

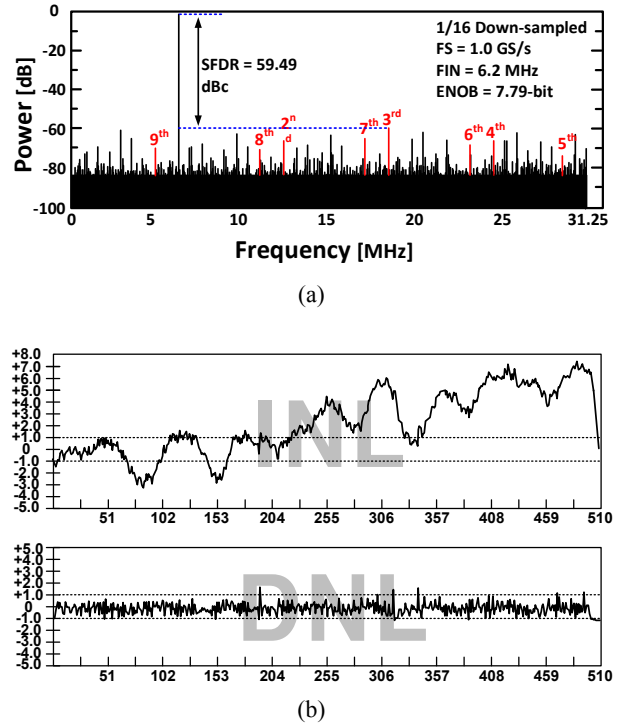


Fig. 6. Measured results (a) FFT spectrum, (b) INL and DNL.

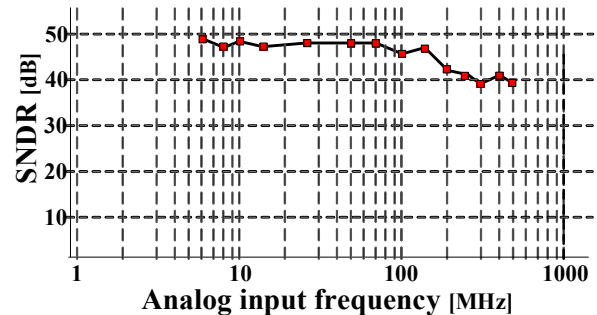


Fig. 7. Measured SNDR vs analog input frequency ($f_s=1$ GHz).

SNDR is about 45.35 dB at 150 MHz, and 40 dB at 500 MHz. In the folding structure, the effective resolution of band width (ERBW) is normally decreased, when the folding amp increases the input signal frequency. In order to solve this problem, an input stage with THA is employed in this paper. Nevertheless, each amplifier connected with cascaded structure causes a degradation of bandwidth (BW). Furthermore, parasitic capacitances are generated by metal layers, gate-drain capacitance, etc. Moreover, the high speed input signal frequency causes a rapid increase of parasitic capacitance. Therefore, the dynamic performance of ADC is degraded by the increase of the input signal frequency.

Table 2. Summary of measured results

Resolution	9-bit
Conversion Rate	1 GS/s
Power Supply	1.1V (Analog&Digital)
SNDR	45.35 dB(150 MHz@1GS/s)
SFDR	55.23 dB(150 MHz@1GS/s)
INL(LSB)	+7 LSB/-3 LSB
DNL(LSB)	+1.5 LSB/-1 LSB
Power Consumption	120 mW (ADC)
Area	2.99 mm ² (ADC)
Process	Samsung 45 nm CMOS Process

Table 3. Performance comparison table

	This work	[11]	[15]	[16]
Technology	45 nm	180 nm	90 nm	65 nm
Resolution	9 bit	10 bit	6 bit	10 bit
Conversion Rate	1 GS/s	1 GS/s	1.6 GS/s	2.6 GS/s
Power Supply	1.1V	1.8V	1.3V	1.2V
SNDR	45.35dB	56.92 dB	30.35dB	48.5 dB
ENOB	7.27 bit	9.1 bit	4.75 bit	7.76 bit
INL [LSB]	7	0.72	1.7	N/A
DNL [LSB]	1.5	0.2	0.67	N/A
Power Dissipation	120 mW	2520 mW	20.1 mW	480 mW
Chip Area	2.99 mm ²	49 mm ²	0.24 mm ²	5.1 mm ²
FOM [pJ/Conv]	0.78	4.59	0.46	0.85

V. CONCLUSIONS

In this paper, a 45 nm 9-bit 1GSPS high precision CMOS folding ADC for a high-performance multi-media equipment has been described. In order to satisfy 9-bit resolution and high conversion rate, the proposed ADC has been designed with an odd number of folding blocks. In the middle of ADC, a digital encoder using adder logic, and a digital error correction logic have been discussed. The chip had been fabricated with Samsung 45nm CMOS process. Table 2 shows the summary of measurement result and performance. Table 3 shows the comparison of this work with other ones. Even though the power consumption of the ADC is 120mW, the FOM is not much better than the others. Thus a calibration circuit must be added in the next version.

ACKNOWLEDGMENTS

This work was supported by a grant-in-aid of Samsung Thales and the MSIP(Ministry of Science, ICT & Future Planning), Korea, under the University ITRC support

program (NIPA-2014-H0301-14-1007) supervised by the NIPA(National IT Industry Promotion Agency), AIPRC.

REFERENCES

- [1] Daeyun Kim and Minkyu Song, "A 65nm 1.2V 7-bit 1GSPS Folding-Interpolation A/D Converter with a Digitally Self-Calibrated Vector Generator", IEICE Transactions on Electronics, Vol. E94-C, No.7, pp.1199-1205, July. 2011.
- [2] Chun-Ying Chen, Michael Q. Le et al., "A Low Power 6-bit Flash ADC With Reference Voltage and Common-Mode Calibration," IEEE Journal of Solid-State Circuits, Vol.44, No. 4, pp. 1041-1046, April. 2009.
- [3] Xicheng Jiang and Mau-Chung Frank Chang, "A 1-GHz Signal Bandwidth 6-bit CMOS ADC With Power-Efficient Averaging," IEEE Journal of Solid-State Circuits, Vol. 40, No. 2, pp. 532-535, Feb. 2005.
- [4] Robert C. Taft, Chris A. Menkus, et al., "A 1.8-V 1.6-GSample/s 8-b Self-Calibrating Folding ADC With 7.26 ENOB at Nyquist Frequency", IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, pp. 2107-2115, Dec. 2004.
- [5] Klaas Bult and Aaron Buchwald, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1- μm^2 ", IEEE Journal of Solid-State Circuits, Vol. 32, No. 12, pp. 1887-1895 Dec. 1997.
- [6] Alireza Razzaghi, Sai-Wang Tam, et al., "A single-channel 10b 1GS/s ADC with 1-cycle Latency using Pipelined Cascaded Folding" IEEE Bipolar/BiCMOS circuits and Technology Meeting, pp. 265-268, Oct. 2008.
- [7] Joongwon Jun, Daeyun Kim, et al., "A 10-b 500 MS/s CMOS Folding A/D Converter with a Hybrid Calibration and a Novel Digital Error Correction Logic", Journal of Semiconductor Technology and Science, Vol. 12, No.1, pp.1-9, March. 2012.
- [8] Myung-Jun Choe, Band-Sup Song, et al., "An 8-b 100-MSample/s CMOS Pipelined Folding ADC," IEEE Journal of Solid-State Circuits, Vol. 36, No. 2, pp. 184-194, Feb. 2001.
- [9] Zheng-Yu Wang, Hui Pan, et al., "A 600MSPS 8-bit Folding ADC in 0.18 μm CMOS," IEEE Symposium on VLSI Circuit Dig. Tech. Papers, pp. 424-427, June. 2004.

- [10] Kiyoshi Makigawa, Koichi Ono, et al., "A 7bit 800Msps 120mW folding and Interpolation ADC Using a Mixed-Averaging Schme," IEEE Symposium on VLSI Circuit Dig. Tech. Papers, pp. 138-139, June. 2006.
- [11] Robert C. Taft, Pier Andrea Francese, et al., "A 1.8 V 1.0 GS/s 10b Self-Calibrating Unified- Folding- Interpolating ADC With 9.1 ENOB at Nyquist Frequency," IEEE Journal of Solid-State Circuits, Vol. 44, No. 12, pp. 2107-2115, Dec. 2009.
- [12] Mingshuo Wang, Tao Lin, et al., "A 1.2 V 1.0-GS/s 8-bit Voltage-Buffer-Free Folding and interpolating ADC," IEEE International Midwest Symposium on Circuits and Systems, pp. 274-277, Aug. 2012.
- [13] Hairong Yu and Mau-Chung Frank Chang, "A 1-V 1.25-GS/S 8-Bit Self-Calibrated Flash ADC in 90-nm Digital CMOS," IEEE Transactions on Circuits and Systems II : Express Briefs, Vol. 55, No.7, pp. 668-672, July. 2008.
- [14] Hyeok-Ki Hong, Wan Kim, Sun-Jae Park, Michael Choi, Ho-Jin Park, and Seung-Tak Ryu, "A 7b 1GS/s 7.2mW Nonbinary 2b/cycle SAR ADC with Register-to-DAC Direct Control," IEEE Custom Integrated Circuits Conference(CICC), pp. 1-4, Sept. 2012.
- [15] Ehsan Zhian Tabasy, Ayman Shafik, Shan Huang, Noah Hae-Woong Yang, Sebastian Hoyos, and Samuel Palermo, "A 6-b 1.6-GS/s ADC With Redundant Cycle One-Tap Embedded DFE in 90-nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 48, No. 8, pp. 1885-1897, Aug. 2013.
- [16] Kostas Doris, Erwin Janssen, Claudio Nani, Athos Zanakopoulos, and Gerard van der Weide, "A 480mW 2.6GS/s 10b Time-Interleaved ADC With 48.5 dB SNDR up to Nyquist in 65nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 46, No. 12, pp. 2821-2833, Dec. 2011.
- [17] Seongjoo Lee, Jangwoo Lee, Mun-Kyo Lee, Sun-Phil Nah, and Minkyu Song, "An 8-b 1GS/s Fractional Folding CMOS Analog-to-Digital Converter with an Arithmetic Digital Encoding Technique," Journal of Semiconductor Technology and Science (JSTS), Vol. 13, No.5, pp.473-481, Oct. 2013.



analog circuit.

Seongjoo Lee received the B.S. degree in Semiconductor Science from Dongguk University, Seoul, Korea in 2013, where he is currently working toward the Integrated Ph. D. course in Department of Semiconductor Science. His major interest is design of CMOS



Science. His major interest is design of CMOS Analog-to-Digital Converter.

Jangwoo Lee received the B.S. degree in Semiconductor Science from Dongguk University, Seoul, Korea in 2012, where he is currently working toward the M.S. degree in Department of Semiconductor



Japan where he worked in the area of low power VLSI design. From 1995 to 1996, he was a researcher in the CMOS Analog Circuit Design Team of Samsung Electronics, Korea. Since 1997, he has been a professor at University of Dongguk, Korea. He is a member of IEEE and IEIE. His major interest is design of CMOS analog circuits, mixed-mode circuits, and low power digital circuits.

Minkyu Song received the B.S. and M.S., and Ph.D. degree in Electronics Engineering from Seoul National University, Korea in 1986, 1988 and 1993, respectively. From 1993 to 1994, he was a researcher at Asada Lab., VDEC, University of Tokyo,