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반응성 질소와 플라즈마 처리에 의한 문턱 스위칭 소자의 개선

(Improved Distribution of Threshold Switching Device by Reactive Nitrogen and Plasma Treatment)

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요 약

두 가지 N_2 프로세스(성장 중 반응성 질소 그리고 질소 플라즈마 경화)에 의해 특별히 개선된 AsGeTeS 위에 만들어진 문턱 스위칭 소자를 제시하고자 한다. 적층과 열적 안정적인 소자 구조가 가능한 두 스텝 프로세스에서의 질소의 사용은 나노급 배열 회로의 응용에서의 스위치와 메모리 소자의 집적을 가능하게 한다. 이것의 좋은 문턱 스위칭 특성에도 불구하고 AsTeGeSi 기반의 스위치는 높은 온도에서의 신뢰성 있는 저항 메모리 적용에 중요한 요소를 가진다. 이것은 보통 Te의 농도 변화에 기인한다. 그러나 chalconitride 스위치(AsTeGeSiN)은 30×30 ($㎚^2$) 셀에서 $1.1\times10^7 A/cm^2$가 넘는 높은 전류 농도를 갖는 높은 온도 안정성을 보여준다. 스위치의 반복 능력은 10^8번을 넘어선다. 더하여 AsTeGeSiN 선택 소자를 가진 TaOx 저항성 메모리를 사용한 1 스위치-1저항으로 구성된 메모리 셀을 시연하였다.

Abstract

We present on a threshold switching device based on AsGeTeSi material which is significantly improved by two N_2 processes: reactive N_2 during deposition, and N_2 plasma hardening. The introduction of N2 in the two-step processing enables a stackable and thermally stable device structure, is allowing integration of switch and memory devices for application in nano scale array circuits. Despite of its good threshold switching characteristics, AsTeGeSi-based switches have had key issues with reliability at a high temperature to apply resistive memory. This is usually due to a change in a Te concentration. However, our chalconitride switches(AsTeGeSiN) show high temperature stability as well as high current density over $1.1\times10^7 A/cm^2$ at 30×30 ($㎚^2$) celll. A cycling performance of the switch was over 10^8 times. In addition, we demonstrated a memory cell consisted of 1 switch-1 resistor (1S-1R) stack structure using a TaOx resistance memory with the AsTeGeSiN select device.

Keywords : Threshold switching device, AsTeGeSiN, Chalconitride, Resistance memory

Ⅰ. Introduction

Resistance based memories in contrast to charge storage based memories allow for superior state retention.[1~2] As devices scale, charge storage based methods must be able to reliably store only a few electrons over 10 years. In contrast, resistance based memories use more stable and durable methods of maintaining their states.

In order to achieve extreme high density beyond 1Tbit, high technologies such as 3D cell stacking, multi-level cell, and scaling down below 10 nm node can be needed. In a high density memory system, each memory devices requires a switch element to suppress sneak current paths. For example, a

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conventional switch element has been Si-based transistor or 2-terminal Si diode to obtain sufficient on-current density and reliability. However, the conventional Si-based switches are not suitable to 3D cell stacking or 10nm node technologies. Although another candidates such as the mixed-ionic-electronic- conduction[3], bidirectional varistor[4] and oxide diodes have been recently proposed as a replacement of Si-based switches. The chalcogenide material, AsTeGeSi, despite its good threshold switching characteristics, have had key issues on degradation with repeated cycling and reliability at post-processing temperatures of 500~600℃. Also, a threshold switching behavior of chalcogenide glass, which results from the trap-limited conduction (TLC) in a highly disordered structure, has been studied[5].

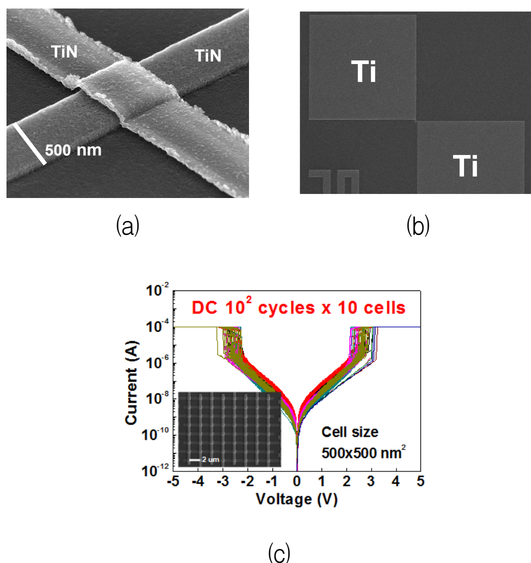

그림 1. (a) 포토리소그래피를 사용하여 TiN을 전극으로 사용한 500 ㎚ 스위치 셀 SEM 사진, (b) 전자선 리소그래피를 사용하여 Ti를 전극으로 사용한 30 ㎚ 스위치 셀 SEM 사진, (c) AsTeGeSiN 500 ㎚ 셀의 스위칭 특성

Fig. 1. (a) SEM image of our 500 nm switch cell using TiN top and bottom electrodes. Conventional photolithography was used to define the cells. (b) SEM image of our 30 nm switch cell using Ti top and bottom electrodes. Electron beam lithography was used to define the cells. (c) Typical switching characteristics of 500 nm cell AsTeGeSiN.

Fig. 1-(a) and (b) shows the SEM images of our 500×500 $㎚^2$ and 30×30 $㎚^2$ threshold switching devices respectively. The typical switching behavior AsTeGeSiN switch is shown in Fig. 1-(c), while the inset shows a crossbar array of switch devices.

Ⅱ. Fabrication of AsTeGeSiN switching devices

We fabricated TiN/AsTeGeSiN/TiN structure as bidirectional switch devices. All films were deposited by using reactive DC magnetron sputtering based on respective metal target. For the fabrication of threshold switching devices, the TiN bottom electrode was deposited by reactive sputter of a Ti target in a mixture of N_2 and Ar. Then, a 40 nm switch layer of AsGeTeSiN was deposited using reactive sputter of a AsTeGeSi target again in a mixture of N_2 and Ar gas and a N_2 plasma treatment was formed and capped with the top TiN or Ti electrode.

E-beam lithography was used to define crossbar cell structures of switch devices from 250 to 30 nm sizes. First, a two-layered electroresist(ER) fabrication process was used to create Ti bottom electrode lines (40 nm thick) on the 500 nm thick SiO_2 substrates. The two ER layers were composed of ZEP- 520A7 from ZEONREX Electronic Chemicals on top of Lift-off-Resist 1A (LOR1A) form Microchem Corp. This method was used to define a more precise cell structure in order to achieve accurate measurements and higher device yields. Top Ti deposition was performed using e-beam evaporation after pattering the bottom lines by E-beam lithography and then using a lift-off method. Device sizes from 0.5 um^2 and above were fabricated similar to E-beam samples; however, conventional project ion photo lithography was used.

Annealing conditions for the experiments presented in Fig. 2 was performed in within the sputtering chamber. First the chamber was pumped down to a base pressure of 10^{-7} Torr, and the substrate holder

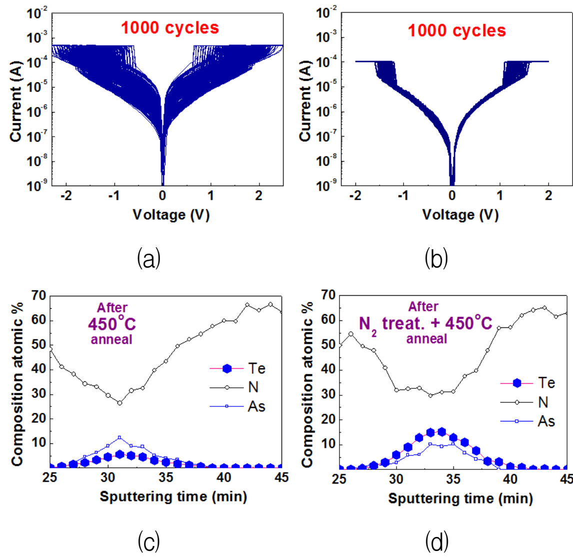

그림 2. 30×30 ㎟ 셀의 열처리 후 관찰된 열화 (a) 주기적 열처리 막 의 DC I-V, (b) 질소 플라즈마 처리 열처리 막의 DC I-V, (c) 질소 처리를 하지 않은 낮은 Te 포화도를 나타내는 막의 XPS 포화도, (d) 질소 처리를 한 높은 Te 포화도를 나타내는 막의 XPS 포화도

Fig. 2. Sample degradation observed after annealing at 30×30 ㎟ cell sizes. (a) DC I-V cycling of annealed films (b) DC I-V cycling of N_2 plasma treated and annealed films. (c) XPS concentration profiles of films showing low Te concentration for non-N_2 treated films. (d) XPS concentration profiles of films showing high Te concentration for N_2 treated films.

temperature was increased to 500℃. The samples were annealed from 15 to 30 minutes and then removed. Additionally annealing in N_2 ambient at 30 mTorr under the same temperature was performed, however, device performance for both reactive N_2 devices and pristine devices did not show any difference from those of vacuum annealed samples.

Ⅲ. N_2 Plasma Nitridation and Analysis

We analyzed the degradation behavior of AsTeGeSiN switches after annealing. The reactive N_2 sputtering and plasma hardening which together form a thin highly crosslinked glass Si_3N_4-based barrier that suppresses Te diffusion in the chalcogenide film, leading to dramatic improvement on its endurance and switching distribution. We believe that a similar treatment is applicable to any materials in which elemental diffusion limits reliability and cycle to cycle distribution. Especially, the introduction of reactive N_2 during deposition improves the thermal stability of the chalcogenide glass which allows memory node and switch device in a single device for stackable complete memory cells. In contrast to previous studies which required wire connection or another method of switching devices separately from memory nodes.

Fig. 2 shows the changes in switching behavior for (a) annealed and (b) N_2 plasma treated +annealed samples. As seen in Fig. 2-(b), the distribution of threshold voltage and current are greatly reduced for N_2 plasma treated samples. We investigated the properties of the select device and the effects of the previously mentioned plasma hardening process which led to a significant improvement in cycle to cycle switching distribution. To confirm the Te loss in non-N_2 treated samples at different annealing conditions, the depth profiles of X-ray photoelectron spectroscopy(XPS) were used to analyze the film composition. The depth profile of a pristine AsTeGeSiN layer(with reactive N_2) is shownin Fig. 2-3(c) and (d). The degradation with continuous switching was apparent as the off-state resistance was reduced by almost two orders of magnitude. The switching voltage also decreased on average while additionally having a wide distribution even between consecutive cycles. After cycling, we performed another XPS depth profile and was able to observe a significant change to the composition. The concentration of tellurium (Te) severely decreased in the non-N_2 plasma treated samples. Especially, striking was the immense diffusion of the Te layer as shown in Fig. 2-(c) from XPS results. Previous models of TS in AsTeGeSiN have proposed that Te acts as the key material for switching, because the trap sites in the deep level was converted to the shallow level in the presence of high fields.[6] The

exact effects of Te diffusion have not been considered at this time; however, it likely seems to be related to both the wide distribution and degraded device resistance properties. Prior to deposition of the top TiN electrode, another sample (Fig. 2-(d)) was prepared with our N_2 plasma hardening treatment. Highly energized N_2 atoms have been previously shown to increase the degree of crosslinking in Si_3N_4 glasses[7] which would retard diffusion across the region due to reduction of defect sites[8]. After annealing at 500 ℃, we run the N_2 plasma treated device for 1000 cycles as shown in Fig.2-(d).

To further investigate and confirm the Te loss in non-N_2 treated samples at different annealing conditions, secondary ion mass spectroscopy (SIMS) analysis was performed as shown in Fig. 3. Fig. 3-(a) shows the SIMS profiles for films deposited at different N_2 partial pressure during deposition. A comparison of the films deposited at 0% and 2% N_2 partial pressure before and after N_2 plasma treatment is shown in Fig.3-(b). We believe that a thin SiN layer and SiN bonding may be related with im provement of thermal stability of the film. The SIMS analysis reveals that N2 plasma treatment creates a thin Si_3N_4 layer on the surface of AsTeGeSiN switch material.

We also performed the modeling for off state conduction based on the trap-limited conduction

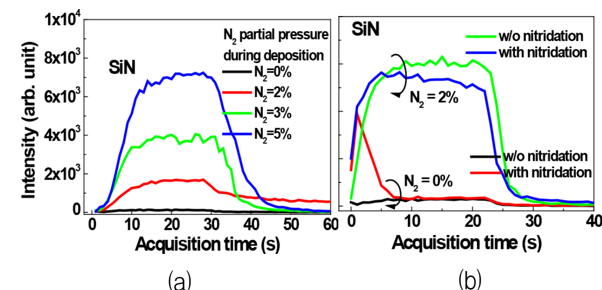

그림 3. SIMS 분석 (a) 질소 부분 압력 조건의 스퍼터링 AsGeTeSiN 막, (b) 질소 프라즈마 처리된 0 % and 2 % 막의 SIMS 변화

Fig. 3. SIMS analysis of (a) AsGeTeSiN films sputtered under differing N_2 partial pressure conditions. (b) Changes to the SIMS profile for 0 % and 2 % films after N_2 plasma treatment.

(TLC) mechanism[9~10]. From the TLC model, we employed the trap-limited conduction model to relate the off-state current with the total trap density and the average trap distance within the AsTeGeSiN deposited films and indeed the model indicated that trap density decreased from $1.5\times10^{18}/cm^3$ down to $4\times10^{17}/cm^3$ after plasma treatment and annealing. Compared with as-dep. sample, the change in trap density and distance of N_2 treated one was suppressed, which means trap density and distance are strongly related with Te loss, as mentioned above. Based on valence alternation pairs model, bonding configurations between chalcogens determine trap density and energy levels in highly disordered structure. Cycling performance of threshold switching devices were shown to be greater than 10^8 times at pulse width of 1us pulse.

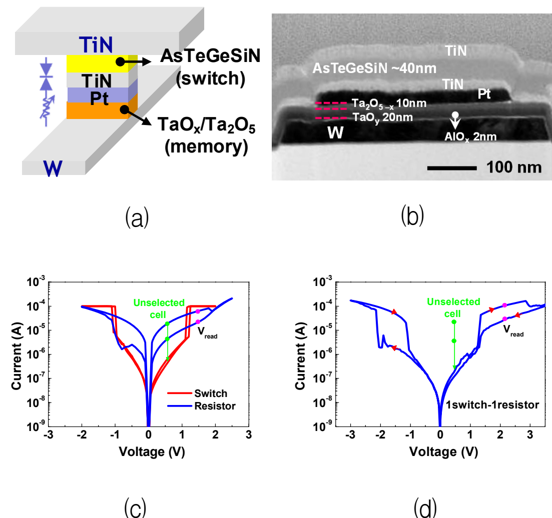

그림 4. RRAM 메모리 셀을 가진 AsGeTeSiN 스위치들의 집적. (a) 구조, (b) 소자 적층 구조의 TEM 사진 , W/Pt 전극 ReRAM 위의 TaOx, (c) 개별 스위치와 메모리 소자의 I-V 특성, (d) 스위치와 메모리 셀의 조합된 I-V 측정

Fig. 4. Integration of AsGeTeSiN switches with RRAM memory cell. (a) Structure, (b) TEM image of device stack structure. TaOx based ReRAM cell with W/Pt electrodes is below the switch with TiN electrodes. (c) I-V characteristics of the individual switch and memory elements. (d) Combined I-V measurement of the switch and memory cell.

Ⅳ. Integration

We demonstrate cell performance of 1S-1R memory cell. Fig. 4-(b) shows a cross-sectional transmission electron microscopy (TEM) image of the stacked structure that combines our memory and select device. The TaO_y/Ta_2O_{5-x} bilayer memory element has been previously demonstrated to shown on volatile high endurance up to 10^{12} and considered to be an appropriate material for the study of switch elements. The TaO_x resistive memory is used as a storage element. Detailed process condition of TaOx resistive memory can be found in journal.[2] The structure begins with the bottom W electrode onto which a thin 2 nm buffer layer is deposited by atomic layer deposition (ALD). This AlOx buffer layer is used to reduce excessive voltage d rop across the switch and memory node when they are both in the irrespective low resistance states[3]. Additionally the thin AlOx layer suppresses any chemical reaction between the W electrode and the memory node layer. Next the TaO_y(20nm) /Ta_2O_{5-x}(10nm) bilayer memory stackared deposited as a storage element. The middle electrode is a Pt/TiN double layer contacted to the appropriate sides for optimal switching. The AsTeGeSiN chalcogenide threshold switching layer is then deposited. In order to form a highly crosslinked glass Si_3N_4-based barrier using the Si within the switching material, we subsequently use a N_2 plasma hardening process on the deposited chalcogenide layer. Finally, the TiN top electrode is formed to complete the stacked device. Figure 1e shows the I-V characteristics of the combined one switch-one resistor (1S-1R) stack structure. The device performance of the individual elements is seen in Fig. 4-(c). Finally the combined 1S-1R switching behavior is confirmed in Fig. 4-(d).

표 1. 선택 소자 요약
Table 1. Summary of our select device.

Parameter	value
Max. current density	1.1×10^{7} A/cm^2 (@ 30 nm node)
Selectivity ΔI @I_{set}, I_{read} (1/2 V_{set})	10^2(@30 um), 10^3 (30 nm)
Endurance	DC: >10^3 , Pulse: >10^8 cycles
Processing temperature	200℃
High Temperature stability	< 500℃

Ⅴ. Conclusion

We summarized the performance of our AsTeGeSiN switch in Table I. By utilizing N2 plasma treatment, we were able to improve the thermal stability of AsTeGeSiN switch devices which is particularly applicable to 3-dimensional cell stacking process. We also demonstrated that the scalability with high performance extends down to at least 30 nm with competitive switching current density for high density memory application.

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