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Compensation PWM Technique for Extended Output Voltage Range in Three-Phase VSI Using Three Shunt Resistors

Seung-Min Shin*, Rae-Kwan Park* and Byoung-Kuk Lee†

Abstract – This paper proposes a compensation PWM technique for the extension of output voltage ranges in three-phase VSI applications using three shunt resistors. The proposed technique aims to solve the dead zone, which occurs in high modulation indexes. In the dead zone, two phase currents cannot be sampled correctly, so that the three-phase VSI cannot be operated up to the maximum output voltage. The dead zone is analyzed in detail, and the compensation PWM algorithm is developed. The proposed algorithm is verified by numerical analysis and experimental results.

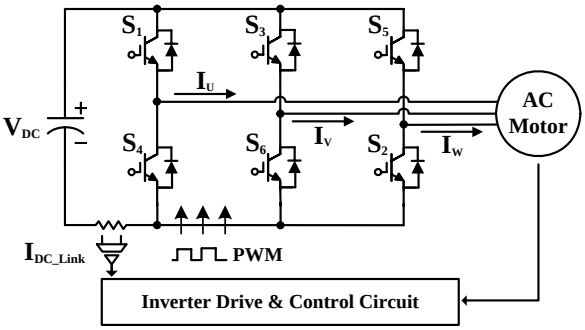
Keywords: Three phase currents sampling, Shunt resistors, Minimum required turn-on time, Three-phase voltage source inverter

1. Introduction

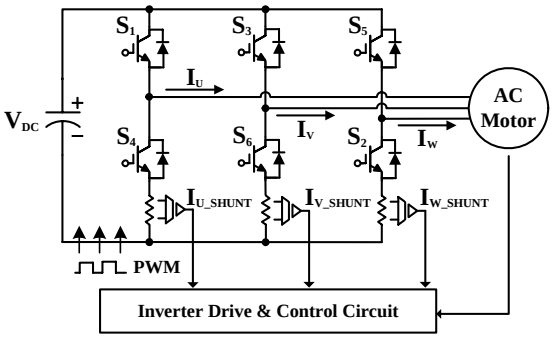
In a three-phase voltage source inverter (VSI) used for AC motor applications, the phase current should be precisely monitored and sensed as much as possible to ensure the stable operation of the VSI. In general, high-bandwidth current sensors such as a current transducer and hall-effect type current sensor are widely used to sense the phase current. However, in some cost sensitive applications, the number of sensors has been reduced and high-bandwidth sensors have been replaced by low cost ones [1, 2].

One of the alternative solutions to monitoring and sensing the phase current is to use a shunt resistor, which has the advantages of low cost and small size. However, the use of shunt resistors leads to two major problems, namely, power loss and dead zone. Implementation of shunt resistors on the main power board increases the power loss. However, the power loss from a few milliohm shunt resistor is negligible in medium power applications like home appliances. Compared to the power loss, the dead zone is a much serious problem. If the output voltage is located in the dead zone, current sampling and reconstruction become limited or impossible without a proper compensation method [3-5].

Two types of phase current sampling techniques using the shunt resistor has been presented in previous studies. One uses a single dc-link shunt resistor connected to a negative dc bus as shown in Fig. 1(a). The information of three phase currents is reconstructed in the DSP (Digital Signal Processor) by using the measured dc-link current with applied pulse width modulation (PWM) switching patterns. However, in this case, when the active switching vector is not maintained for a sufficient time, a dead zone needs to be considered [6, 7]. To solve this dead zone problem, which arises from the use of the single dc-link shunt resistor, various strategies have been proposed: adjusted pulse width modulation method [8, 9]; modified modulation method [10]; observer method [11]; and vector insertion method [12]. However, the single dc-link shunt resistor technique is limitedly used in industrial applications since the reliability of the start-up and low speed control for AC motors is not ensured. The other phase current sampling technique uses three shunt resistors, each connected



(a) Single dc-link shunt resistor



(b) Three shunt resistors

Fig. 1. Two types of phase current sampling techniques using shunt resistors

† Corresponding Author: School of Information and Communication Engineering, Sungkyunkwan University, Korea. (bkleeskku@skku.edu)
* School of Information and Communication Engineering, Sungkyunkwan University, Korea. (shinmin000@skku.edu)
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between the emitter of a power switch and the dc-link negative line as shown in Fig. 1(b). This technique is widely used in some cost sensitive home applications and vector control drives since there is no limit on the low modulation indexes for the start-up and low speed control and it can provide sufficient reliability and cost-effectiveness. However, at high modulation indexes, it also induces the dead zone when the holding time of the zero switching vector is not sufficient for measurement of reliable phase current information in the DSP [13, 14].

Phase current regulation using three shunt resistors cannot be guaranteed above about 90% of the maximum output voltage in space vector pulse width modulation (SVPWM) [15]. In this problem output voltage range, the holding time of the zero switching vector is not sufficient for current sampling in the DSP. Therefore, in this paper, the advanced PWM technique for the three shunt resistors is proposed to extend the output voltage range of the three-phase VSI. With the proposed technique, the three-phase VSI can be controlled up to the maximum output voltage in SVPWM. Moreover, the proposed technique can be implemented simply with the low-cost DSP. The proposed technique is verified by experiments measuring the phase current under various conditions.

2. Analysis of Phase Currents Sampling Using Three Shunt Resistors

2.1 General description of phase currents sampling

Unlike the hall-effect type current sensors and current transducers, the three shunt resistors are connected between the emitters of the power switches and the dc-link negative line, respectively, to share the same ground terminal, so they depend on the states of low side switches (S_4, S_6 and S_2) to measure the phase currents. There are eight switching state combinations: active switching vectors (V_1 ~ V_6) and zero switching vectors (V_0 and V_7). The sampling phase currents for each switching vector are summarized in Table 1. For the zero switching vector 111, no phase current can be sampled since no phase current flows through any of the shunt resistors. However, in the case of the zero switching vector 000, all phase currents can be sampled since three phase currents are freewheeled through a load and the low-side switches. For phase current regulation in the three-phase VSI, information about at least two phase currents is required. The unknown phase current can be calculated assuming current symmetry, i.e., $I_U + I_V + I_W = 0$. Therefore, in the cases of vectors V_1, V_3 and V_5, information about three phase currents can be obtained. However, in the case of vectors V_2, V_4 and V_6, phase current regulation is impossible since only one phase current can be sampled.

Table 1. Sampling phase currents according to switching vectors

Switching vectors	Low side switch states	Sampling phase current
V_0 (000)	S_4=ON, S_6=ON, S_2=ON	I_U, I_V, I_W
V_1 (100)	S_4=OFF, S_6=ON, S_2=ON	I_V, I_W
V_2 (110)	S_4=OFF, S_6=OFF, S_2=ON	I_W
V_3 (010)	S_4=ON, S_6=OFF, S_2=ON	I_U, I_W
V_4 (011)	S_4=ON, S_6=OFF, S_2=OFF	I_U
V_5 (001)	S_4=ON, S_6=ON, S_2=OFF	I_U, I_V
V_6 (101)	S_4=OFF, S_6=ON, S_2=OFF	I_V
V_7 (111)	S_4=OFF, S_6=OFF, S_2=OFF	No phase current can be sampled

In the PWM period ($T_S = T_k + T_{k+1} + T_0$, $k = 1 \sim 5$), there are two active switching vectors (V_k and V_{k+1}) for two active switching vector times (T_k and T_{k+1}) and two zero switching vectors (V_0 and V_7) for a zero switching vector time (T_0). For examples, in sector 2, a reference voltage vector (V^*) is calculated as

$$V^* = \frac{T_2}{T_S}V_2 + \frac{T_3}{T_S}V_3 \tag{1}$$

In the PWM period T_S, at least one of the vectors V_2, V_4 and V_6 is included, and the switching vector time is changed according to the magnitude and angle of the reference voltage vector. Therefore, in order to obtain information about three phase currents in the DSP, regardless of the switching vectors and the reference voltage vector, the current sampling point must be synchronized with the peak of a PWM carrier since vector V_0 always appears at the peak of a PWM carrier.

2.2 Limitation of phase currents sampling

For reliable phase current sampling, the turn-on times of the low-side switches should be longer than the minimum required turn-on time. Based on Fig. 2, the minimum turn-on time is determined as

$$T_{MIN} = T_{DEL} + T_{RS} + T_{AD} \tag{2}$$

T_{MIN} includes the IGBT turn-on delay time (T_{DEL}), phase

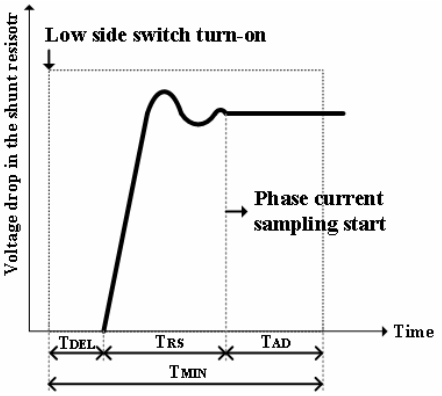


Fig. 2. Minimum required turn-on time of the low side switch

current rise and settling time (T_{RS}) and analog-to-digital conversion time (T_{AD}). T_{DEL} includes the dead time, IGBT driver signal processing time and IGBT turn-on delay time. T_{AD} is related to the extra sample and hold time, which is needed to ensure the ADC operation after the sampling has initiated. If T_{MIN} is not guaranteed, phase current sampling cannot be ensured.

The turn-on times of the low-side switches for each phase are calculated based on the active switching vector time and the zero switching vector time as shown in Fig. 3. T_{SHORT}, T_{MIDDLE} and T_{LONG} represent the turn-on times of each low-side switch. The largest phase voltage determines T_{SHORT}, the medium one determines T_{MIDDLE} and the smallest one determines T_{LONG}. These times vary according to the switching vectors used in each sector as shown in Table 2.

T_{LONG} is always longer than T_{MIN} because each phase current has a phase shift of 120 degrees. However, T_{SHORT} and T_{MIDDLE} are the limiting factors of phase current sampling since they decrease depending on the output voltage command. Accordingly, T_{SHORT} should satisfy the following condition to ensure measurement of three phase currents at the same time

$$T_{SHORT} = T_0 \geq T_{MIN} \tag{3}$$

If T_{SHORT} does not satisfy condition (3), the corresponding phase current cannot be sampled correctly. Then, T_{MIDDLE} determines whether another phase current can be sampled or not. Therefore, conditions for two phase currents sampling can be written as

$$T_{SHORT} = T_0 < T_{MIN} \tag{4}$$

$$T_{MIDDLE} = T_0 + 2T_k \geq T_{MIN} \quad k = 1,3,5 \tag{5}$$

In the conditions (4) and (5), the phase current corresponding to T_{SHORT} cannot be sampled correctly. However, the phase currents corresponding to T_{MIDDLE} and T_{LONG} can be sampled correctly. Consequently, the unknown phase current can be calculated. Nevertheless, it should be noted that if T_{SHORT} and T_{MIDDLE} are shorter than T_{MIN}, the use of the output voltage is limited since two phase currents cannot be sampled accurately; this condition is called the dead zone. Therefore, in the dead zone, the solving technique is strongly required to control and extend the output voltage range for the three-phase VSI using three shunt resistors.

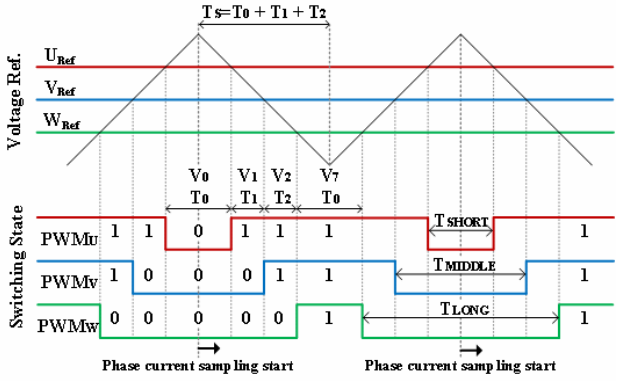


Fig. 3. Relationship between the three-phase PWM pattern and the low-side switches turn-on time in sector 1

Table 2. Limitation phase according to low-side switch turn-on time

Voltage sector	Low side switch turn-on time	Limitation phase
Sector 1	$T_{SHORT}=PWM_U=T_0$ $T_{MIDDLE}=PWM_V=T_0+2T_1$ $T_{LONG}=PWM_W=T_0+2T_1+2T_2$	PWM_U, PWM_V
Sector 2	$T_{SHORT}=PWM_V=T_0$ $T_{MIDDLE}=PWM_U=T_0+2T_3$ $T_{LONG}=PWM_W=T_0+2T_2+2T_3$	PWM_U, PWM_V
Sector 3	$T_{SHORT}=PWM_V=T_0$ $T_{MIDDLE}=PWM_W=T_0+2T_3$ $T_{LONG}=PWM_U=T_0+2T_3+2T_4$	PWM_V, PWM_W
Sector 4	$T_{SHORT}=PWM_W=T_0$ $T_{MIDDLE}=PWM_V=T_0+2T_5$ $T_{LONG}=PWM_U=T_0+2T_4+2T_5$	PWM_V, PWM_W
Sector 5	$T_{SHORT}=PWM_W=T_0$ $T_{MIDDLE}=PWM_U=T_0+2T_5$ $T_{LONG}=PWM_V=T_0+2T_5+2T_6$	PWM_U, PWM_W
Sector 6	$T_{SHORT}=PWM_U=T_0$ $T_{MIDDLE}=PWM_W=T_0+2T_1$ $T_{LONG}=PWM_V=T_0+2T_6+2T_1$	PWM_U, PWM_W

3. Proposed Compensation PWM Technique

In order to reliably use a three-phase VSI using three shunt resistors up to the maximum output voltage vector, three phase currents need to be classified as a measurable phase current or an immeasurable phase current.

3.1 Dead zone analysis

In the PWM period T_S, T_0 is determined by the highest phase voltage command. As shown in Fig. 4, if T_0 does not

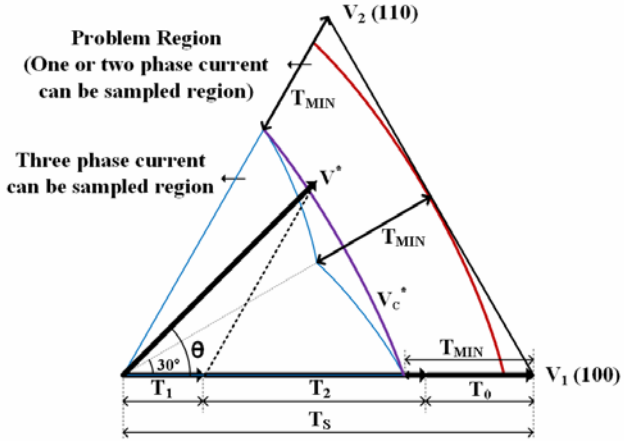


Fig. 4. Problem region in sector 1 in which three phase current sampling is not possible

satisfy condition (3), the phase current corresponding to the highest voltage phase command cannot be sampled correctly. The criterion of the reference voltage vector for three phase currents sampling can be calculated as

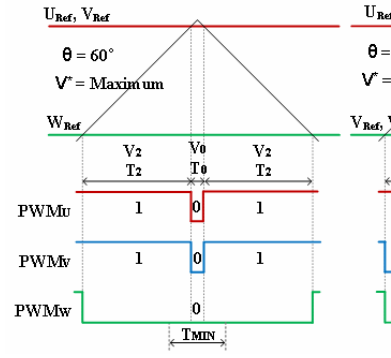
$$V_C^* = \frac{2}{3} V_{DC}(1 - 2T_{MIN} f_{sw}) \quad (6)$$

where V_{DC} is the dc-link voltage and the f_{sw} is the switching frequency in the three-phase VSI. Furthermore, in this problem region, two phase currents sampling region and only one phase current sampling region exist together according to the magnitude and angle of the reference voltage vector. Especially, the only one phase current sampling region, which is the dead zone, is affected by the holding times of vectors V_2, V_4 and V_6.

Fig. 5 shows the three phase PWM patterns at the maximum output voltage vector for the reference voltage vector angle of 0° and 60°. In the case of Fig. 5(b), the turn-on times of the low-side switches are obtained by using T_0 and T_1. The highest phase voltage command does not satisfy condition (3). However, the two phase currents corresponding to T_{MIDDLE} and T_{LONG} can be sampled. In contrast, when θ approaches 60 degrees, T_1 is decreased and T_2 is increased. If condition (5) is not satisfied according to the increase of T_2, the information about the two phase currents corresponding to T_{SHORT} and T_{MIDDLE} cannot be sampled as shown in Fig. 5(a). Therefore, a dead zone is generated when the reference voltage vector centers the marked region in Fig. 6, and it is also generated around V_4 and V_6 same as V_2.

3.2 Classification of each phase

In each PWM cycle, a criterion, regardless of the magnitude and angle of the reference voltage vector, is needed to determine whether conditions (3) and (5) are satisfied or not. This criterion can be obtained from the magnitude of the phase voltage, which is compared with the PWM carrier to generate the PWM pattern. If the magnitude of the phase voltage is large, the turn-on times of the low-side switches are short and if it is small, the turn-on times of low-side switches are long, therefore, the magnitude of the phase voltage for T_{MIN} can be determined. Consequentially, after the magnitude of the phase voltage for T_{MIN} is determined, phase currents can be classified as either measureable or immeasurable by comparison with each phase voltage. The criterion phase voltage for T_{MIN} can be determined as



(a) PWM pattern in θ=60° (b) PWM pattern in θ=0°

Fig. 5. Relationship between the angle of the reference voltage vector and the three phase PWM pattern at the maximum output voltage vector

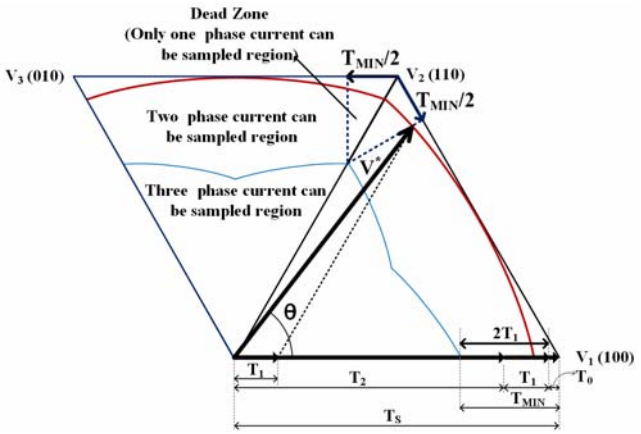
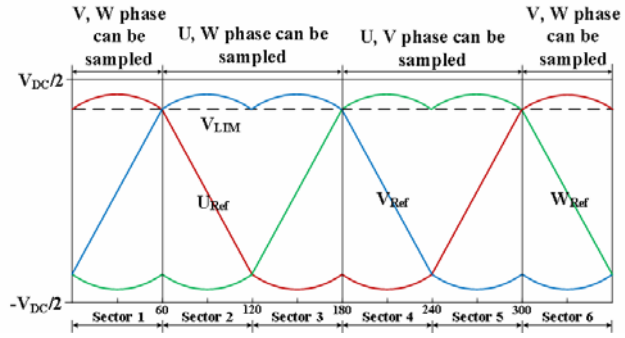
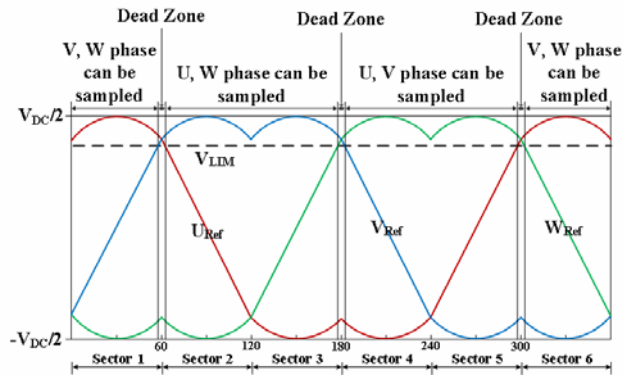


Fig. 6. Classification of unusable reference voltage vector due to the dead zone



(a) Two phase measurable regions



(b) Two or one phase measurable regions

Fig. 7. Classification of each phase voltage in SVPWM

$$V_{LIM} = \frac{V_{DC}}{2} - T_{MIN} f_{sw} V_{DC} \quad (7)$$

When all phase voltages are smaller than V_{LIM}, all phase currents can be sampled. However, when the largest phase voltage is greater than V_{LIM}, condition (3) is not satisfied as shown in Fig. 7(a). In this case, the phase current can be classified as immeasurable using Eq. (7). Furthermore, the dead zone is generated as shown in Fig. 7(b) when the magnitude of the reference voltage vector is bigger than the value of Eq. (6). If one of the three phase voltages is bigger than V_{LIM}, the immeasurable phase current can be calculated in the same way as in the Fig. 7(a) case. However, if two of the three phase voltages are bigger than V_{LIM}, all phase voltages need to be reconstructed to obtain a longer time than T_{MIN}.

3.3 Implementation of compensation PWM technique

The compensation PWM technique is implemented through four processes as shown in Fig. 8. The phase separator process compares each phase voltage with V_{LIM} in order to classify three phase voltages into the measurable phase current and the immeasurable phase current. The phase compensator process reconstructs all phase voltages to measure at least two phase currents when two of the three phase voltages are bigger than V_{LIM}. The next process is the current sampling. When all phase voltages are smaller than V_{LIM}, three phase current sampling is carried out. However, when one or two phase voltages are bigger than V_{LIM}, two phase current sampling is carried out. The current calculator process calculates the unknown phase current information at the end.

Three operation modes are integrated in the compensation PWM technique. The first mode is operated when all phase currents can be sampled directly. Second mode is operated when two phase currents can be sampled. Third mode is operated in the dead zone.

3.3.1 Mode 1

When all phase voltages are smaller than V_{LIM}, three phase currents can be sampled directly using the three shunt resistors. This mode is operated in the phase separator process and the current sampling process.

3.3.2 Mode 2

When one of the three phase voltages are bigger than V_{LIM}, the immeasurable phase current must be calculated so that it can be classified in the phase separator. In the current calculator, the immeasurable phase current is calculated using the measurable phase current obtained from the current sampling process.

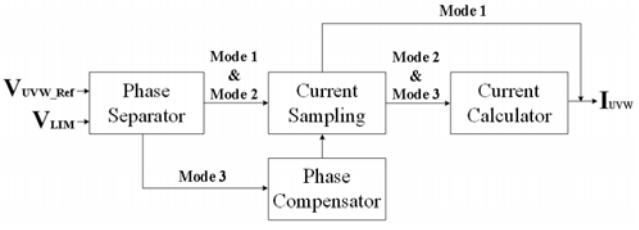


Fig. 8. Compensation PWM technique process

3.3.3 Mode 3

When two of the three phase voltages are bigger than V_{LIM}, all voltages need the reconstruction to sample two phase currents as shown in Fig. 9. Two immeasurable phase currents are classified in the phase separator. In the phase compensator, first, the middle magnitude phase voltage (V_{MIDDLE}) between two immeasurable phases (V_{IM_1ph}, V_{IM_2ph}) is determined as follows

$$V_{IM\_1ph} > V_{IM\_2ph}, V_{MIDDLE} = V_{IM\_2ph} \quad (8)$$

$$V_{IM\_1ph} < V_{IM\_2ph}, V_{MIDDLE} = V_{IM\_1ph} \quad (9)$$

Then, the minimum rate of voltage change to guarantee T_{MIN} in V_{MIDDLE} is calculated as

$$V_{DIF} = V_{MIDDLE} - V_{LIM} \quad (10)$$

If V_{MIDDLE} is reduced by V_{DIF}, its immeasurable phase is changed to the measurable phase. Voltage reconstruction is performed as follows to guarantee T_{MIN} in two phases without change of the line-to-line voltage

$$V_{SHORT\_DIF} = V_{SHORT} - V_{DIF} < V_{LIM} \quad (11)$$

$$V_{MIDDLE\_DIF} = V_{MIDDLE} - V_{DIF} = V_{LIM} \quad (12)$$

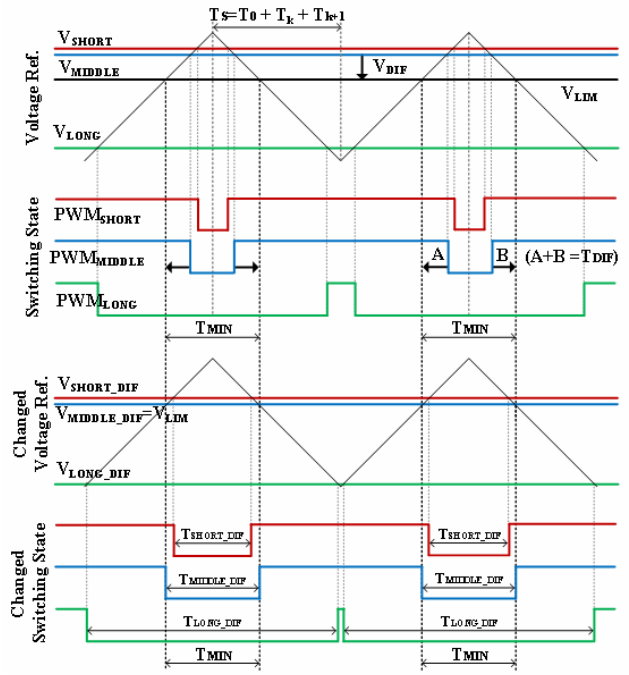


Fig. 9. Modified reference voltages and switching states for two phase currents sampling in mode 3

$$V_{LONG\_DIF} = V_{LONG} - V_{DIF} > V_{LIM} \quad (13)$$

where V_{SHORT} is the biggest phase voltage, V_{MIDDLE} is medium one and V_{LONG} is the smallest one. Using the phase voltage reconstruction as Eqs. (11, 12) and (13), the turn-on times of the low-side switches becomes longer since the reconstructed reference voltage becomes smaller than the reference voltage. V_{SHORT} is changed to V_{SHORT_DIF}, but nevertheless the phase current corresponding to V_{SHORT_DIF} cannot be still sampled. However, V_{MIDDLE} is reconstructed to V_{MIDDLE_DIF} which guarantees T_{MIN} for the phase current sampling. The phase current corresponding to V_{LONG} can be sampled without the voltage reconstruction since the turn-on times of the low-side switches corresponding to V_{LONG} is always longer than T_{MIN}. Thus, the voltage change for phase current sampling is minimized by setting V_{MIDDLE} on the criterion of the voltage reconstruction. Moreover, all phase voltages are reconstructed to sample two phase currents without change of the line-to-line voltage. The turn-on times of the low-side switches is changed as follows during the voltage reconstruction.

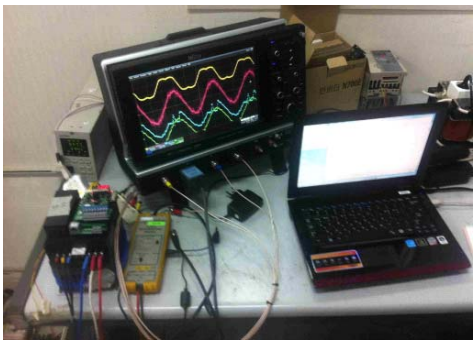
$$T_{SHORT\_DIF} = T_0 + T_{DIF} < T_{MIN} \quad (14)$$

$$T_{MIDDLE\_DIF} = T_0 + T_k + T_{DIF} = T_{MIN} \quad (15)$$

$$T_{LONG\_DIF} = T_0 + T_k + T_{k+1} + T_{DIF} > T_{MIN} \quad (16)$$

where T_{DIF} is added to the turn-on times of the low-side switches through the voltage change. Therefore, since two phase currents corresponding to V_{MIDDLE} and V_{LONG} can be sampled, the remaining phase current corresponding to V_{SHORT} can be calculated using these phase currents in the current calculator.

(a) Induction motor dynamo set



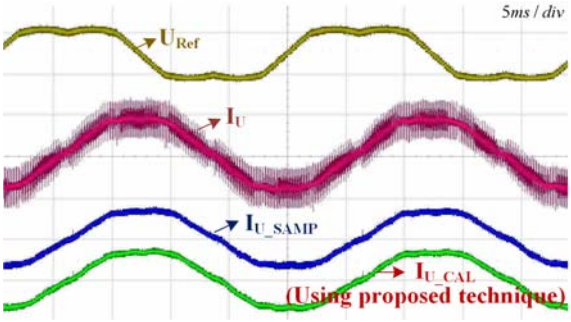
(b) Measurement equipment

Fig. 10. Experimental test-bed

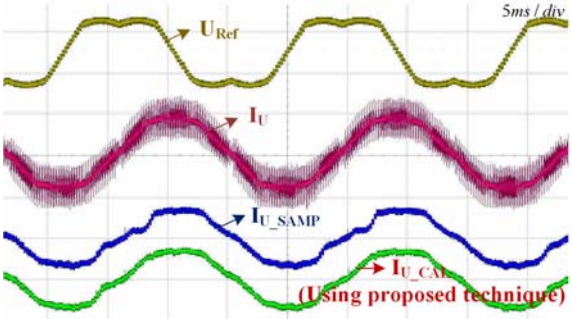
4. Experimental Results

Fig. 10 shows the entire experimental system including the proposed technique to monitor phase currents. To validate the feasibility of the proposed compensation PWM technique, a VSI using three shunt resistors based on Freescale DSP 56F803 was implemented. V23990-P546-A28 module of Vincotech was chosen for the inverter. The shunt resistor of 10mΩ was employed to sense the phase current. The internal variables inside the DSP were monitored through a 12-bit serial digital-to-analog converter (DAC). The other parameters used in this experiment were as follows: VDC is 310V; TMIN is 23usec; f_{sw} is 5kHz. An experiment was performed in V/F control with an induction motor.

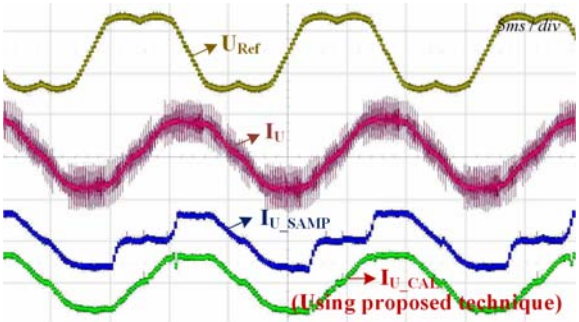
Fig. 11 shows the reconstruction current waveforms



(a) No load test at MI = 0.66



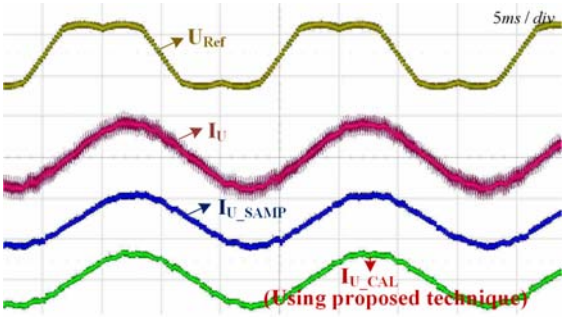
(b) No load test at MI = 0.93



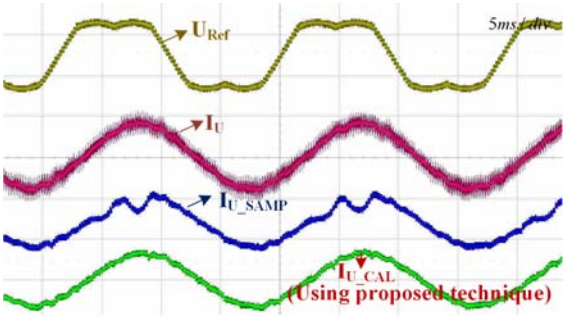
(c) No load test at MI = 1

Fig. 11. Comparison of compensation PWM technique test according to MI at no load (U_{Ref}: 10V/div; I_U: 10A/div; I_{U_SAMP} and I_{U_CAL}: 5V/div)

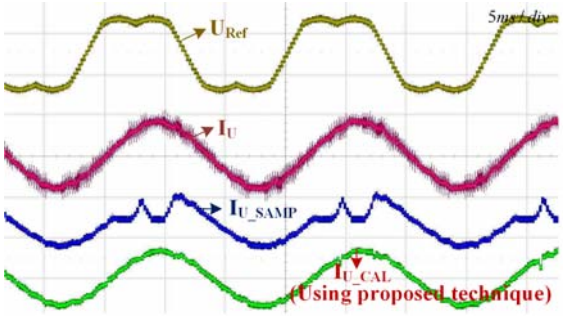
without and with the proposed compensation PWM technique under no load. I_{U_SAMP} and I_{U_CAL} are DAC signals which are sampled by using the ADC in the DSP. I_{U_SAMP} is sampled without the compensation PWM technique and I_{U_CAL} is sampled with the compensation PWM technique. I_U is the U phase output current, which is measured using a current probe. Before the application of the compensation PWM technique, I_{U_SAMP} had an extremely distorted waveform in high MI. Especially, when θ is varied between about -60° and 60°, it could not be sampled accurately, as predicted in Sector 3. When MI is 0.66, the phase current information can be sampled correctly since the turn-on times of the low-side switches is longer than T_{MIN} as shown in Fig. 11(a). In contrast, when MI is bigger than 0.93, I_{U_SAMP} was extremely distorted as shown Figs. 11(b) and (C). When MI is higher than before, the distortion of the ADC signal is getting worse since the region where the phase voltage is bigger than V_{LIM} is increased. However, regardless of the MI, I_{U_CAL} has a nearly similar waveform as I_U. Fig. 12 shows the reconstruction current waveform when the three-phase VSI is controlled at full load. When MI is 0.66, the phase current information can be sampled correctly as shown Fig. 12(a). However, same as Figs. 11(b) and (c), when MI is bigger than 0.93, I_{U_SAMP} is extremely distorted as shown Figs. 12(b) and (C). The difference is that the immeasurable region is shifted since a current phase angle is shifted according to load status. Nevertheless, I_{U_CAL} also has a nearly similar waveform as I_U regardless of MI.



(a) Full load test at MI = 0.66



(b) Full load test at MI = 0.93



(c) Full load test at MI = 1

Fig. 12. Comparison of compensation PWM technique test according to MI at full load (U_{Ref}: 10V/div; I_U: 20A/div; I_{U_SAMP} and I_{U_CAL}: 10V/div)

5. Conclusion

A three-phase VSI using three shunt resistors cannot be used until the maximum output voltage has been analyzed. From the analysis, three phase currents sampling region, two phase currents sampling region and one phase current sampling region were identified. This paper proposed the compensation PWM technique to use the whole output voltage range of the three-phase VSI using three shunt resistors. The proposed technique classifies the measurable phase current and the immeasurable phase current based on a criterion phase voltage. Therefore, the minimum rate of voltage change to guarantee the minimum required turn-on time of the low-side switch can be calculated. In the dead zone, voltage reconstruction is performed to guarantee T_{MIN} in two phases without change of the line-to-line voltage. As a result, the voltage utilization of the three-phase VSI can be improved from low-performance V/F drives to high-performance vector control drives. The validity of the proposed technique has been supported by experimental results.

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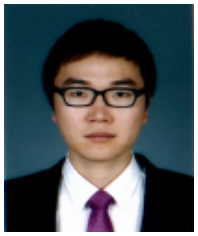

Seung-Min Shin He received his B.S. and M.S. degrees in Electrical Engineering from Sungkyunkwan University, Suwon, Korea, in 2009 and 2011, respectively. Since 2009, he has studied for Ph.D. degree in electrical Engineering at Sungkyunkwan University. His research interests are electric vehicle drives, power electronics and advanced motor drive systems.

Rae-Kwan Park He received the B.S. and the M.S. degrees in Electrical Engineering from Hanyang University, Seoul, Korea, in 1992 and 1994, respectively. Since 2010, he has worked for his Ph. D. degree in Electrical Engineering at Sungkyunkwan University. His research interests include electric motor drives, electrical machines, high/low power DC-DC converter for PHEV/EV and advanced motor drive systems.

Byoung-Kuk Lee He received the B.S. and the M.S. degrees from Hanyang University, Seoul, Korea, in 1994 and 1996, respectively and the Ph.D. degree from Texas A&M University, College Station, TX, in 2001, all in electrical engineering. From 2003 to 2005, he has been a Senior Researcher at Power Electronics Group, Korea Electrotechnology Research Institute (KERI), Changwon, Korea. From 2006 Dr. Lee joins at School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea. His research interests include charger for electric vehicles, hybrid renewable energy systems, dc distribution systems for home appliances, power conditioning systems for fuel cells and photovoltaic, modeling and simulation, and power electronics. Prof. Lee is a recipient of Outstanding Scientists of the 21st Century from IBC and listed on 2008 Ed. of Who's Who in America. Prof. Lee is an Associate Editor in the IEEE Transactions on Industrial Electronics and Power Electronics. He was the General Chair for IEEE Vehicular Power and Propulsion Conference (VPPC) in 2012.